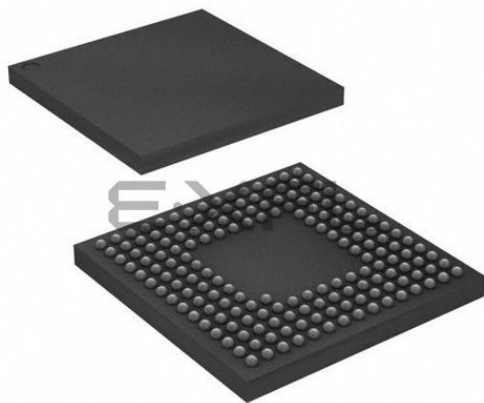




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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	148
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	177-TFLGA
Supplier Device Package	177-TFLGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5630dddlc-u0

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part number.

Table 1.3 List of Products (1/2)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX630 (D version)	R5F56307CDFN	PLQP0080KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307DDFN	PLQP0080KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307CDFP	PLQP0100KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307DDFP	PLQP0100KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307CDLA	PTLG0100KA-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307DDLA	PTLG0100KA-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308CDFN	PLQP0080KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308DDFN	PLQP0080KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308CDFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308DDFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308CDLA	PTLG0100KA-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308DDLA	PTLG0100KA-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDFP*1	PLQP0100KB-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDFP*1	PLQP0100KB-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDFB*1	PLQP0144KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDFB*1	PLQP0144KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDLK*1	PTLG0145KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDLK*1	PTLG0145KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDFC	PLQP0176KB-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDFC	PLQP0176KB-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDBG	PLBG0176GA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDBG	PLBG0176GA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDLC	PTLG0177KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDLC	PTLG0177KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDFP*1	PLQP0100KB-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDFP*1	PLQP0100KB-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDFB*1	PLQP0144KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDFB*1	PLQP0144KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDLK*1	PTLG0145KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDLK*1	PTLG0145KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDFC	PLQP0176KB-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDFC	PLQP0176KB-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDBG	PLBG0176GA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDBG	PLBG0176GA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDLC	PTLG0177KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDLK	PTLG0177KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DCDFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DDDFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DCDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DDDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DCDLK	PTLG0145KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C

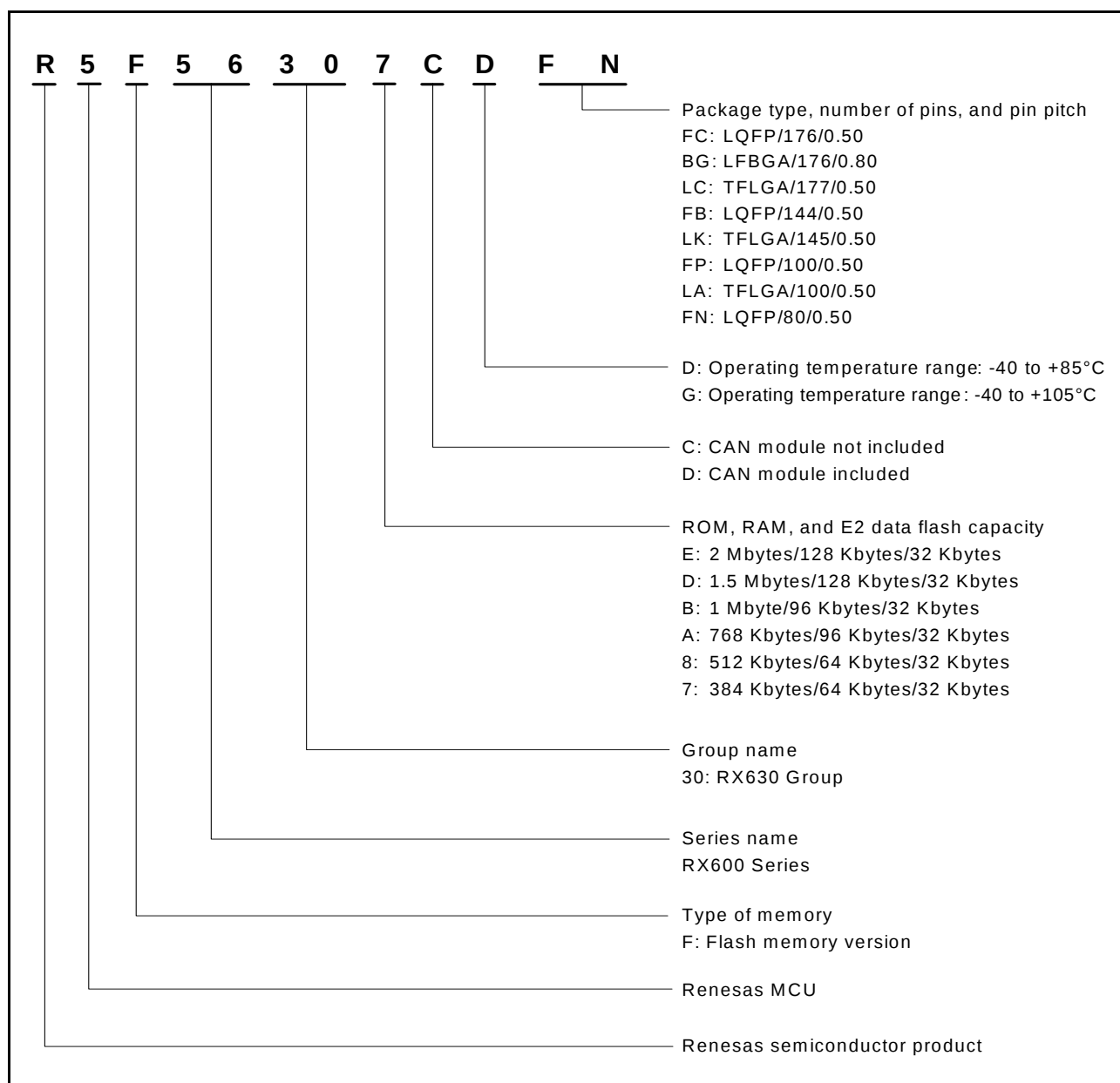


Figure 1.1 How to Read the Product Part Number

RX630 Group
PTLG0100KA-A (100-Pin TFLGA)
(Top View)

	A	B	C	D	E	F	G	H	J	K	
10	PE2	PE3	PE4	PA0	PA3	VSS	VCC	PB7	PC1	PC2	10
9	PE1	PD7	PE5	PA1	PA5	PA7	PB1	PB6	PC0	PC3	9
8	PE0	PD6	PD5	PE7	PA4	PB0	PB4	PC6	PC4	PC5	8
7	PD4	PD3	PD2	PE6	PA6	PB2	PB5	PC7	P50	P51	7
6	PD0	PD1	P47	P46	PA2	PB3	P52	P54	VCC_ USB	USB0_ DP	6
5	P43	P44	P42	P45	P41	P12	P53	P55	VSS_ USB	USB0_ DM	5
4	VREFL0	P40	VREFH0	VBATT	P34	P32	P27	P15	P13	P14	4
3	P07	AVCC0	PJ3	MD	RES#	P35	P30	P16	P17	P20	3
2	VREFH	AVSS0	VREFL	XCOUT	VSS	VCC	P31	P25	P21	P22	2
1	P05	EMLE	VCL	XCIN	XTAL	EXTAL	P33	P26	P24	P23	1
	A	B	C	D	E	F	G	H	J	K	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pins and Pin Functions (145-Pin TFLGA).

Figure 1.8 Pin Assignment (100-Pin TFLGA)

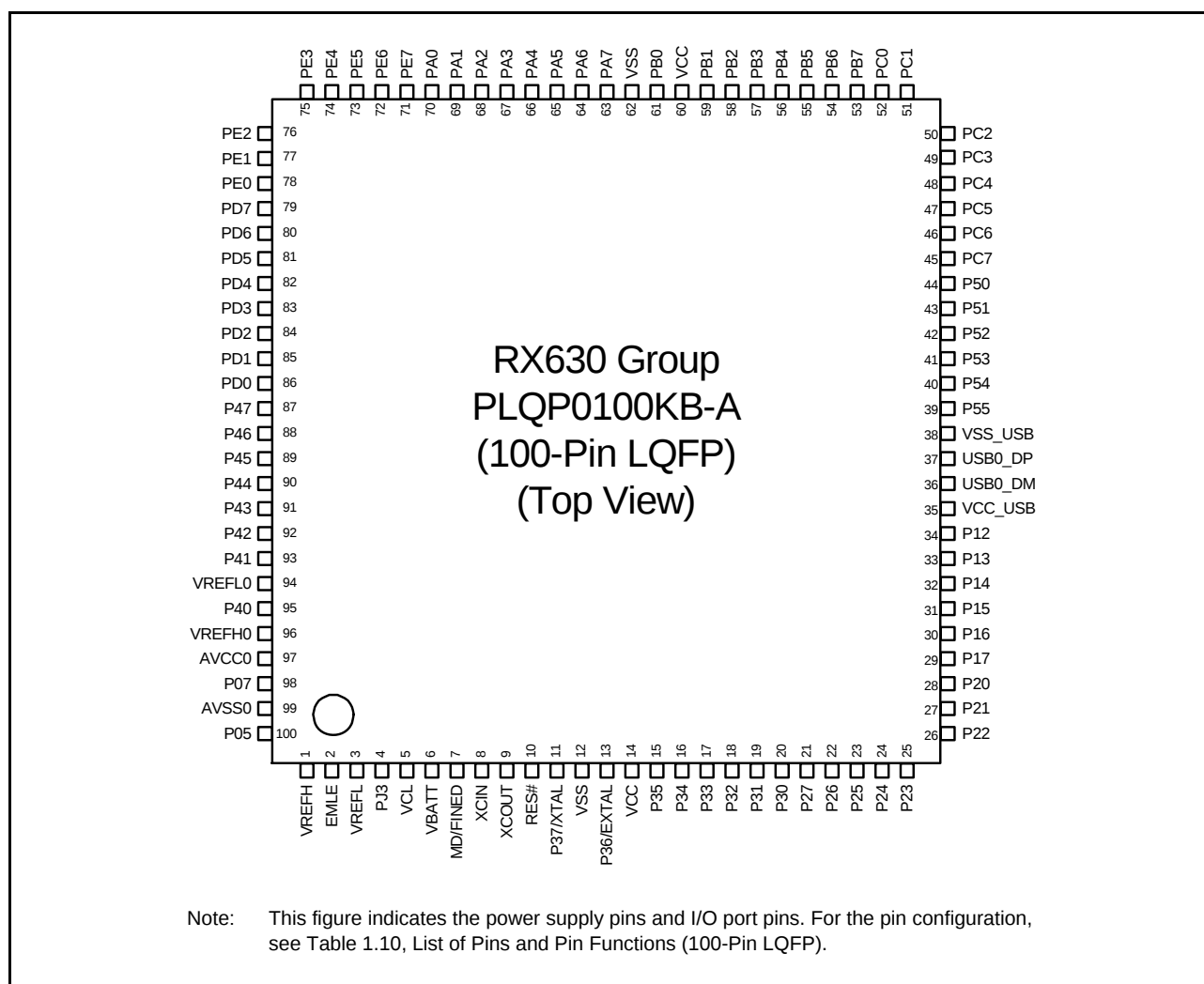


Figure 1.9 Pin Assignment (100-Pin LQFP)

Table 1.5 List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (2/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
C13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	SSLB0		AN2
C14		PK4			RXD4/SMISO4/SSCL4		
C15		P70			SCK4		
D1		P01		TMCI0	RXD6/SMISO6/SSCL6	IRQ9	AN019
D2		P02		TMCI1	SCK6	IRQ10	AN020
D3		P03				IRQ11	DA0
D4		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
D5		P44				IRQ12-DS	AN004
D6		P93	A19/D19		CTS7#/RTS7#/SS7#		AN017
D7		P95	A21/D21				
D8		PK1					
D9		PD5	D5[A5/D5]	MTIC5W/POE2#	SSLC1	IRQ5	AN013
D10		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
D11		P61	CS1#		CTS9#/RTS9#/SS9#		
D12		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	RSPCKB	IRQ5	AN3
D13		PK5			TXD4/SMOSI4/SSDA4		
D14		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
D15		P65	CS5#				
E1		PJ5					
E2	EMLE						
E3		PF5				IRQ4	
E4	VSS						
E5*1	NC						
E12		PE6	D14[A14/D14]	TIOCA11	CTS4#/RTS4#/SS4#/ MOSIB	IRQ6	AN4
E13	TRDATA0	PG2	D26				
E14	TRDATA1	PG3	D27				
E15		P67	CS7#		CRX2*2	IRQ15	
F1	VBATT						
F2	VCL						
F3		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
F4	BSCANP						
F12		P66	CS6#		CTX2*2		
F13	TRSYNC#	PG4	D28				
F14		PA0	A0/BC0#	MTIOC4A/TIOCA0/PO16	SSLA1		
F15	VSS						
G1	XCIN						
G2	XCOUT						
G3	MD FINED						
G4	TRST#	PF4					
G12	TRCLK	PG5	D29				
G13	TRDATA2	PG6	D30				
G14		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2	IRQ11	
G15	VCC						

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (1/4)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
A1	AVSS0						
A2		P07				IRQ15	ADTRG0#
A3		P40				IRQ8-DS	AN000
A4		P42				IRQ10-DS	AN002
A5		P45				IRQ13-DS	AN005
A6		P90	A16		TXD7/SMOSI7/SSDA7		AN014
A7		P92	A18		RXD7/SMISO7/SSCL7		AN016
A8		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010
A9		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
A10		PK3			RXD9/SMISO9/SSCL9		
A11		P62	CS2#				
A12		PE1	D9[A9/D9]	MTIOC4C/TIOCD9/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/RSPCKB		ANEX1
A13		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/PO26/ POE8#	CTS12#/RTS12#/SS12#/ MISOB		AN1
B1	VREFH						
B2	AVCC0						
B3		P05				IRQ13	DA1
B4	VREFL0						
B5		P43				IRQ11-DS	AN003
B6		P47				IRQ15-DS	AN007
B7		P91	A17		SCK7		AN015
B8		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
B9		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
B10		PK2			TXD9/SMOSI9/SSDA9		
B11		P61	CS1#		CTS9#/RTS9#/SS9#		
B12		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/PO23	RXD12/SMISO12/ SSCL12/RXDX12/SSLB3/ MOSIB	IRQ7-DS	AN0
B13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	SSLB0		AN2
C1	VREFL						
C2		P02		TMCI1	SCK6	IRQ10	AN020
C3	VREFH0						
C4		P41				IRQ9-DS	AN001
C5		P46				IRQ14-DS	AN006
C6	VSS						
C7		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
C8		PD3	D3[A3/D3]	TIOCB8/TCLKH/POE8#	RSPCKC	IRQ3	AN011
C9		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
C10		P63	CS3#				
C11		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0
C12		P70			SCK4		
C13		PK4			RXD4/SMISO4/SSCL4		
D1		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
D2		PF5				IRQ4	
D3		P03				IRQ11	DA0
D4		P01		TMCI0	RXD6/SMISO6/SSCL6	IRQ9	AN019

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (1/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
1	AVSS0						
2		P05				IRQ13	DA1
3	VREFH						
4		P03				IRQ11	DA0
5	VREFL						
6		P02		TMCI1	SCK6	IRQ10	AN020
7		P01		TMCI0	RXD6/SMISO6/SSCL6	IRQ9	AN019
8		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
9		PF5				IRQ4	
10	EMLE						
11		PJ5					
12	VSS						
13		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
14	VCL						
15	VBATT						
16	MD/FINED						
17	XCIN						
18	XCOUT						
19	RES#						
20	XTAL	P37					
21	VSS						
22	EXTAL	P36					
23	VCC						
24		P35				NMI	
25	TRST#	P34		MTIOC0A/TMCI3/PO12/ POE2#	SCK6/SCK0	IRQ4	
26		P33		MTIOC0D/TIOC0D/ TMRI3/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0	IRQ3-DS	
27		P32		MTIOC0C/TIOCC0/TMO3/ PO10/RTCCOUT/RTCCIC2	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0	IRQ2-DS	
28	TMS	P31		MTIOC4D/TMCI2/PO9/ RTCCIC1	CTS1#/RTS1#/SS1#/ SSLB0	IRQ1-DS	
29	TDI	P30		MTIOC4B/TMRI3/PO8/ RTCCIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB	IRQ0-DS	
30	TCK/FINEC	P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB		
31	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
32		P25	CS5#	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3		ADTRG0#
33		P24	CS4#	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3		
34		P23		MTIOC3D/MTCLKD/ TIOC03/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3		
35		P22		MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0		
36		P21		MTIOC1B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/SSCL0/ SCL1	IRQ9	
37		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/SSDA0/ SDA1	IRQ8	

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (4/4)

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
108		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/PO26/ POE8#	CTS12#/RTS12#/SS12#/ MISOB		AN1
109		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/PO23	RXD12/SMISO12/ SSCL12/RDX12/SSLB3/ MOSIB	IRQ7-DS	AN0
110		PE1	D9[A9/D9]	MTIOC4C/TIOCD9/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/RSPCKB		ANEX1
111		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0
112		P64	CS4#				
113		P63	CS3#				
114		P62	CS2#				
115		P61	CS1#		CTS9#/RTS9#/SS9#		
116		PK3			RXD9/SMISO9/SSCL9		
117		P60	CS0#		SCK9		
118		PK2			TXD9/SMOSI9/SSDA9		
119		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
120		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
121		PD5	D5[A5/D5]	MTIC5W/POE2#	SSLC1	IRQ5	AN013
122		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
123		PD3	D3[A3/D3]	TIOCB8/TCLKH/POE8#	RSPCKC	IRQ3	AN011
124		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010
125		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
126		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
127		P93	A19		CTS7#/RTS7#/SS7#		AN017
128		P92	A18		RXD7/SMISO7/SSCL7		AN016
129		P91	A17		SCK7		AN015
130	VSS						
131		P90	A16		TXD7/SMOSI7/SSDA7		AN014
132	VCC						
133		P47				IRQ15-DS	AN007
134		P46				IRQ14-DS	AN006
135		P45				IRQ13-DS	AN005
136		P44				IRQ12-DS	AN004
137		P43				IRQ11-DS	AN003
138		P42				IRQ10-DS	AN002
139		P41				IRQ9-DS	AN001
140	VREFLO						
141		P40				IRQ8-DS	AN000
142	VREFH0						
143	AVCC0						
144		P07				IRQ15	ADTRG0#

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 MB/1.5 MB

Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (2/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
33		P13		MTIOC0B/TIOCA5/TMO3/ PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
34		P12		TMC11	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
35	VCC_USB						
36					USB0_DM		
37					USB0_DP		
38	VSS_USB						
39		P55	WAIT#	MTIOC4D/TMO3	CRX1	IRQ10	
40		P54	ALE	MTIOC4B/TMC11	CTS2#/RTS2#/SS2#/ CTX1		
41	BCLK	P53*2					
42		P52	RD#		RXD2/SMISO2/SSCL2/ SSLB3		
43		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
44		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
45		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA	IRQ14	
46		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMC12/PO30	RXD8/SMISO8/SSCL8/ MOSIA	IRQ13	
47		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TMRI2/PO29	SCK8/RSPCKA		
48		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMC11/PO25/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0		
49		PC3	A19	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ IETXD		
50		PC2	A18	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/IERXD		
51		PC1	A17	MTIOC3A/TCLKD/PO18	SCK5/SSLA2	IRQ12	
52		PC0	A16	MTIOC3C/TCLKC/PO17	CTS5#/RTS5#/SS5#/ SSLA1	IRQ14	
53		PB7	A15	MTIOC3B/TIOCB5/PO31	TXD9/SMOSI9/SSDA9		
54		PB6	A14	MTIOC3D/TIOCA5/PO30	RXD9/SMISO9/SSCL9		
55		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	SCK9		
56		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/SS9#		
57		PB3	A11	MTIOC0A/MTIOC4A/ TIOC3D/TCLKD/TMO0/ PO27/POE3#	SCK6		
58		PB2	A10	TIOCC3/TCLKC/PO26	CTS6#/RTS6#/SS6#		
59		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25	TXD6/SMOSI6/SSDA6	IRQ4-DS	
60	VCC						
61		PB0	A8	MTIC5W/TIOCA3/PO24	RXD6/SMISO6/SSCL6/ RSPCKA	IRQ12	
62	VSS						
63		PA7	A7	TIOCB2/PO23	MISOA		
64		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMC13/PO22/ POE2#	CTS5#/RTS5#/SS5#/ MOSIA		
65		PA5	A5	TIOCB1/PO21	RSPCKA		
66		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS	

Table 4.1 List of I/O Registers (Address Order) (7/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 70C7h	ICU	Interrupt request register 199	IR199	8	8	2 ICLK		ICUb
0008 70C8h	ICU	Interrupt request register 200	IR200	8	8	2 ICLK		
0008 70C9h	ICU	Interrupt request register 201	IR201	8	8	2 ICLK		
0008 70D6h	ICU	Interrupt request register 214	IR214	8	8	2 ICLK		
0008 70D7h	ICU	Interrupt request register 215	IR215	8	8	2 ICLK		
0008 70D8h	ICU	Interrupt request register 216	IR216	8	8	2 ICLK		
0008 70D9h	ICU	Interrupt request register 217	IR217	8	8	2 ICLK		
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8	2 ICLK		
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8	2 ICLK		
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8	2 ICLK		
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8	2 ICLK		
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8	2 ICLK		
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8	2 ICLK		
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8	2 ICLK		
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8	2 ICLK		
0008 70E2h	ICU	Interrupt request register 226	IR226	8	8	2 ICLK		
0008 70E3h	ICU	Interrupt request register 227	IR227	8	8	2 ICLK		
0008 70E4h	ICU	Interrupt request register 228	IR228	8	8	2 ICLK		
0008 70E5h	ICU	Interrupt request register 229	IR229	8	8	2 ICLK		
0008 70E6h	ICU	Interrupt request register 230	IR230	8	8	2 ICLK		
0008 70E7h	ICU	Interrupt request register 231	IR231	8	8	2 ICLK		
0008 70E8h	ICU	Interrupt request register 232	IR232	8	8	2 ICLK		
0008 70E9h	ICU	Interrupt request register 233	IR233	8	8	2 ICLK		
0008 70EAh	ICU	Interrupt request register 234	IR234	8	8	2 ICLK		
0008 70EBh	ICU	Interrupt request register 235	IR235	8	8	2 ICLK		
0008 70ECh	ICU	Interrupt request register 236	IR236	8	8	2 ICLK		
0008 70EDh	ICU	Interrupt request register 237	IR237	8	8	2 ICLK		
0008 70EEh	ICU	Interrupt request register 238	IR238	8	8	2 ICLK		
0008 70EFh	ICU	Interrupt request register 239	IR239	8	8	2 ICLK		
0008 70F0h	ICU	Interrupt request register 240	IR240	8	8	2 ICLK		
0008 70F1h	ICU	Interrupt request register 241	IR241	8	8	2 ICLK		
0008 70F2h	ICU	Interrupt request register 242	IR242	8	8	2 ICLK		
0008 70F3h	ICU	Interrupt request register 243	IR243	8	8	2 ICLK		
0008 70F4h	ICU	Interrupt request register 244	IR244	8	8	2 ICLK		
0008 70F5h	ICU	Interrupt request register 245	IR245	8	8	2 ICLK		
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8	2 ICLK		
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8	2 ICLK		
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8	2 ICLK		
0008 70F9h	ICU	Interrupt request register 249	IR249	8	8	2 ICLK		
0008 70FAh	ICU	Interrupt request register 250	IR250	8	8	2 ICLK		
0008 70FBh	ICU	Interrupt request register 251	IR251	8	8	2 ICLK		
0008 70FCh	ICU	Interrupt request register 252	IR252	8	8	2 ICLK		
0008 70FDh	ICU	Interrupt request register 253	IR253	8	8	2 ICLK		
0008 711Bh	ICU	DTC activation enable register 027	DTCE027	8	8	2 ICLK		
0008 711Ch	ICU	DTC activation enable register 028	DTCE028	8	8	2 ICLK		
0008 711Dh	ICU	DTC activation enable register 029	DTCE029	8	8	2 ICLK		
0008 711Eh	ICU	DTC activation enable register 030	DTCE030	8	8	2 ICLK		
0008 711Fh	ICU	DTC activation enable register 031	DTCE031	8	8	2 ICLK		
0008 7121h	ICU	DTC activation enable register 033	DTCE033	8	8	2 ICLK		
0008 7122h	ICU	DTC activation enable register 034	DTCE034	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (8/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7127h	ICU	DTC activation enable register 039	DTCE039	8	8	2 ICLK		ICUb
0008 7128h	ICU	DTC activation enable register 040	DTCE040	8	8	2 ICLK		
0008 712Ah	ICU	DTC activation enable register 042	DTCE042	8	8	2 ICLK		
0008 712Bh	ICU	DTC activation enable register 043	DTCE043	8	8	2 ICLK		
0008 712Dh	ICU	DTC activation enable register 045	DTCE045	8	8	2 ICLK		
0008 712Eh	ICU	DTC activation enable register 046	DTCE046	8	8	2 ICLK		
0008 7140h	ICU	DTC activation enable register 064	DTCE064	8	8	2 ICLK		
0008 7141h	ICU	DTC activation enable register 065	DTCE065	8	8	2 ICLK		
0008 7142h	ICU	DTC activation enable register 066	DTCE066	8	8	2 ICLK		
0008 7143h	ICU	DTC activation enable register 067	DTCE067	8	8	2 ICLK		
0008 7144h	ICU	DTC activation enable register 068	DTCE068	8	8	2 ICLK		
0008 7145h	ICU	DTC activation enable register 069	DTCE069	8	8	2 ICLK		
0008 7146h	ICU	DTC activation enable register 070	DTCE070	8	8	2 ICLK		
0008 7147h	ICU	DTC activation enable register 071	DTCE071	8	8	2 ICLK		
0008 7148h	ICU	DTC activation enable register 072	DTCE072	8	8	2 ICLK		
0008 7149h	ICU	DTC activation enable register 073	DTCE073	8	8	2 ICLK		
0008 714Ah	ICU	DTC activation enable register 074	DTCE074	8	8	2 ICLK		
0008 714Bh	ICU	DTC activation enable register 075	DTCE075	8	8	2 ICLK		
0008 714Ch	ICU	DTC activation enable register 076	DTCE076	8	8	2 ICLK		
0008 714Dh	ICU	DTC activation enable register 077	DTCE077	8	8	2 ICLK		
0008 714Eh	ICU	DTC activation enable register 078	DTCE078	8	8	2 ICLK		
0008 714Fh	ICU	DTC activation enable register 079	DTCE079	8	8	2 ICLK		
0008 7162h	ICU	DTC activation enable register 098	DTCE098	8	8	2 ICLK		
0008 7166h	ICU	DTC activation enable register 102	DTCE102	8	8	2 ICLK		
0008 717Eh	ICU	DTC activation enable register 126	DTCE126	8	8	2 ICLK		
0008 717Fh	ICU	DTC activation enable register 127	DTCE127	8	8	2 ICLK		
0008 7180h	ICU	DTC activation enable register 128	DTCE128	8	8	2 ICLK		
0008 7181h	ICU	DTC activation enable register 129	DTCE129	8	8	2 ICLK		
0008 7182h	ICU	DTC activation enable register 130	DTCE130	8	8	2 ICLK		
0008 7183h	ICU	DTC activation enable register 131	DTCE131	8	8	2 ICLK		
0008 7184h	ICU	DTC activation enable register 132	DTCE132	8	8	2 ICLK		
0008 7185h	ICU	DTC activation enable register 133	DTCE133	8	8	2 ICLK		
0008 7186h	ICU	DTC activation enable register 134	DTCE134	8	8	2 ICLK		
0008 7187h	ICU	DTC activation enable register 135	DTCE135	8	8	2 ICLK		
0008 7188h	ICU	DTC activation enable register 136	DTCE136	8	8	2 ICLK		
0008 7189h	ICU	DTC activation enable register 137	DTCE137	8	8	2 ICLK		
0008 718Ah	ICU	DTC activation enable register 138	DTCE138	8	8	2 ICLK		
0008 718Bh	ICU	DTC activation enable register 139	DTCE139	8	8	2 ICLK		
0008 718Ch	ICU	DTC activation enable register 140	DTCE140	8	8	2 ICLK		
0008 718Dh	ICU	DTC activation enable register 141	DTCE141	8	8	2 ICLK		
0008 718Eh	ICU	DTC activation enable register 142	DTCE142	8	8	2 ICLK		
0008 718Fh	ICU	DTC activation enable register 143	DTCE143	8	8	2 ICLK		
0008 7190h	ICU	DTC activation enable register 144	DTCE144	8	8	2 ICLK		
0008 7191h	ICU	DTC activation enable register 145	DTCE145	8	8	2 ICLK		
0008 7194h	ICU	DTC activation enable register 148	DTCE148	8	8	2 ICLK		
0008 7195h	ICU	DTC activation enable register 149	DTCE149	8	8	2 ICLK		
0008 7196h	ICU	DTC activation enable register 150	DTCE150	8	8	2 ICLK		
0008 7197h	ICU	DTC activation enable register 151	DTCE151	8	8	2 ICLK		
0008 7198h	ICU	DTC activation enable register 152	DTCE152	8	8	2 ICLK		
0008 7199h	ICU	DTC activation enable register 153	DTCE153	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (18/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8327h	RIIC1	I ² C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK	RIIC
0008 8328h	RIIC1	I ² C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8329h	RIIC1	I ² C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 832Ah	RIIC1	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 832Ah	RIIC1	Timeout Internal Counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK	
0008 832Bh	RIIC1	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 832Bh	RIIC1	Timeout Internal Counter U	TMOCNTU	8	8	2, 3 PCLKB	2 ICLK	
0008 832Ch	RIIC1	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 832Dh	RIIC1	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 832Eh	RIIC1	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	
0008 832Fh	RIIC1	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	
0008 8330h	RIIC1	I ² C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	
0008 8331h	RIIC1	I ² C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8332h	RIIC1	I ² C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	
0008 8333h	RIIC1	I ² C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	
0008 8340h	RIIC2	I ² C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8341h	RIIC2	I ² C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8342h	RIIC2	I ² C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8343h	RIIC2	I ² C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8344h	RIIC2	I ² C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 8345h	RIIC2	I ² C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK	
0008 8346h	RIIC2	I ² C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK	
0008 8347h	RIIC2	I ² C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8348h	RIIC2	I ² C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8349h	RIIC2	I ² C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 834Ah	RIIC2	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 834Bh	RIIC2	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 834Ch	RIIC2	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 834Dh	RIIC2	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 834Eh	RIIC2	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	
0008 834Fh	RIIC2	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	
0008 8350h	RIIC2	I ² C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	
0008 8351h	RIIC2	I ² C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8352h	RIIC2	I ² C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	
0008 8353h	RIIC2	I ² C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	
0008 8360h	RIIC3	I ² C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8361h	RIIC3	I ² C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8362h	RIIC3	I ² C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8363h	RIIC3	I ² C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8364h	RIIC3	I ² C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 8365h	RIIC3	I ² C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK	
0008 8366h	RIIC3	I ² C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK	
0008 8367h	RIIC3	I ² C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8368h	RIIC3	I ² C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8369h	RIIC3	I ² C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 836Ah	RIIC3	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 836Bh	RIIC3	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 836Ch	RIIC3	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 836Dh	RIIC3	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 836Eh	RIIC3	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (21/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8632h	MTU	Timer buffer transfer set register	TBTER	8	8	2, 3 PCLKB	2 ICLK	MTU2a
0008 8634h	MTU	Timer dead time enable register	TDER	8	8	2, 3 PCLKB	2 ICLK	
0008 8636h	MTU	Timer output level buffer register	TOLBR	8	8	2, 3 PCLKB	2 ICLK	
0008 8638h	MTU3	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK	
0008 8639h	MTU4	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK	
0008 8640h	MTU4	Timer A/D converter start request control register	TADCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8644h	MTU4	Timer A/D converter start request cycle set register A	TADCORA	16	16	2, 3 PCLKB	2 ICLK	
0008 8646h	MTU4	Timer A/D converter start request cycle set register B	TADCORB	16	16	2, 3 PCLKB	2 ICLK	
0008 8648h	MTU4	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16	2, 3 PCLKB	2 ICLK	
0008 864Ah	MTU4	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8660h	MTU	Timer waveform control register	TWCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8680h	MTU	Timer start register	TSTR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8681h	MTU	Timer synchronous register	TSYR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8684h	MTU	Timer read/write enable register	TRWER	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8690h	MTU0	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8691h	MTU1	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8692h	MTU2	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8693h	MTU3	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8694h	MTU4	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8695h	MTU5	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8700h	MTU0	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8701h	MTU0	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8702h	MTU0	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8703h	MTU0	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8704h	MTU0	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8705h	MTU0	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8706h	MTU0	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8708h	MTU0	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 870Ah	MTU0	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 870Ch	MTU0	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 870Eh	MTU0	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 8720h	MTU0	Timer general register E	TGRE	16	16	2, 3 PCLKB	2 ICLK	
0008 8722h	MTU0	Timer general register F	TGRF	16	16	2, 3 PCLKB	2 ICLK	
0008 8724h	MTU0	Timer interrupt enable register 2	TIER2	8	8	2, 3 PCLKB	2 ICLK	
0008 8726h	MTU0	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK	
0008 8780h	MTU1	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8781h	MTU1	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8782h	MTU1	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 8784h	MTU1	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8785h	MTU1	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8786h	MTU1	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8788h	MTU1	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 878Ah	MTU1	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8790h	MTU1	Timer input capture control register	TICCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8800h	MTU2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8801h	MTU2	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8802h	MTU2	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (36/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0009 0853h	CAN0	Mailbox search mode register	MSMR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 0854h	CAN0	Time stamp register	TSR	16	16	2, 3 PCLKB	2 ICLK	
0009 0856h	CAN0	Acceptance filter support register	AFSR	16	16	2, 3 PCLKB	2 ICLK	
0009 0858h	CAN0	Test control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0009 1200h to 0009 13FFh	CAN1	Mailbox registers 0 to 31	MB0 to 31	128	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 1400h to 0009 141Fh	CAN1	Mask register 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 1420h	CAN1	FIFO received ID compare register 0	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 1424h	CAN1	FIFO received ID compare register 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 1428h	CAN1	Mask invalid register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 142Ch	CAN1	Mailbox interrupt enable register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 1820h to 0009 183Fh	CAN1	Message control registers 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK	
0009 1840h	CAN1	Control register	CTLR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 1842h	CAN1	Status register	STR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 1844h	CAN1	Bit configuration register	BCR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 1848h	CAN1	Receive FIFO control register	RFCR	8	8	2, 3 PCLKB	2 ICLK	
0009 1849h	CAN1	Receive FIFO pointer control register	RFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 184Ah	CAN1	Transmit FIFO control register	TFCR	8	8	2, 3 PCLKB	2 ICLK	
0009 184Bh	CAN1	Transmit FIFO pointer control register	TFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 184Ch	CAN1	Error interrupt enable register	EIER	8	8	2, 3 PCLKB	2 ICLK	
0009 184Dh	CAN1	Error interrupt factor judge register	EIFR	8	8	2, 3 PCLKB	2 ICLK	
0009 184Eh	CAN1	Receive error count register	RECR	8	8	2, 3 PCLKB	2 ICLK	
0009 184Fh	CAN1	Transmit error count register	TECR	8	8	2, 3 PCLKB	2 ICLK	
0009 1850h	CAN1	Error code store register	ECSR	8	8	2, 3 PCLKB	2 ICLK	
0009 1851h	CAN1	Channel search support register	CSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 1852h	CAN1	Mailbox search status register	MSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 1853h	CAN1	Mailbox search mode register	MSMR	8	8	2, 3 PCLKB	2 ICLK	
0009 1854h	CAN1	Time stamp register	TSR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 1856h	CAN1	Acceptance filter support register	AFSR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 1858h	CAN1	Test control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0009 2200h to 0009 23FFh	CAN2	Mailbox registers 0 to 31	MB0 to 31	128	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 2400h to 0009 241Fh	CAN2	Mask register 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 2420h	CAN2	FIFO received ID compare register 0	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 2424h	CAN2	FIFO received ID compare register 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 2428h	CAN2	Mask invalid register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 242Ch	CAN2	Mailbox interrupt enable register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 2820h to 0009 283Fh	CAN2	Message control registers 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK	
0009 2820h to 0009 283Fh	CAN2	Message control registers 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK	
0009 2840h	CAN2	Control register	CTLR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 2842h	CAN2	Status register	STR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 2844h	CAN2	Bit configuration register	BCR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (37/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0009 2848h	CAN2	Receive FIFO control register	RFCCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2849h	CAN2	Receive FIFO pointer control register	RFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Ah	CAN2	Transmit FIFO control register	TFCCR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Bh	CAN2	Transmit FIFO pointer control register	TFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Ch	CAN2	Error interrupt enable register	EIER	8	8	2, 3 PCLKB	2 ICLK	
0009 284Dh	CAN2	Error interrupt factor judge register	EIFR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Eh	CAN2	Receive error count register	RECR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Fh	CAN2	Transmit error count register	TECR	8	8	2, 3 PCLKB	2 ICLK	
0009 2850h	CAN2	Error code store register	ECSR	8	8	2, 3 PCLKB	2 ICLK	
0009 2851h	CAN2	Channel search support register	CSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 2852h	CAN2	Mailbox search status register	MSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 2853h	CAN2	Mailbox search mode register	MSMR	8	8	2, 3 PCLKB	2 ICLK	
0009 2854h	CAN2	Time stamp register	TSR	16	16	2, 3 PCLKB	2 ICLK	
0009 2856h	CAN2	Acceptance filter support register	AFSR	16	16	2, 3 PCLKB	2 ICLK	
0009 2858h	CAN2	Test control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
000A 0000h	USB0	System configuration control register	SYSCFG	16	16	3, 4 PCLKB	2, 3 ICLK	USBa
000A 0004h	USB0	System configuration status register 0	SYSSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*8	
000A 0008h	USB0	Device state control register 0	DVSTCTR0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*8	
000A 0014h	USB0	CFIFO port register	CFIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK	
000A 0018h	USB0	D0FIFO port register	D0FIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK	
000A 001Ch	USB0	D1FIFO port register	D1FIFO	16	8, 16	3, 4 PCLKB	2, 3 ICLK	
000A 0020h	USB0	CFIFO port select register	CFIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK	
000A 0022h	USB0	CFIFO port control register	CFIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK	
000A 0028h	USB0	D0FIFO port select register	D0FIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK	
000A 002Ah	USB0	D0FIFO port control register	D0FIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK	
000A 002Ch	USB0	D1FIFO port select register	D1FIFOSEL	16	16	3, 4 PCLKB	2, 3 ICLK	
000A 002Eh	USB0	D1FIFO port control register	D1FIFOCTR	16	16	3, 4 PCLKB	2, 3 ICLK	
000A 0030h	USB0	Interrupt enable register 0	INTENB0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*8	
000A 0036h	USB0	BRDY interrupt status register	BRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*8	
000A 0038h	USB0	NRDY interrupt status register	NRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*8	

Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, T_a = T_{opr}

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Supply current*1	High-speed operating mode	Max.*2		I _{CC} *3	—	—	100	mA	ICLK = 100 MHz PCLKB = 50 MHz FCLK = 50 MHz BCLK = 50 MHz	
		Normal	Peripheral function: clock signal supplied*4		—	52	—			
			Peripheral function: clock signal stopped*4		—	40	—			
		Sleep mode			—	25	60			
		All-module-clock-stop mode (reference value)			—	20	30			
		Increased by BGO operation*5			—	15	—			
	Low-speed operating mode 1*6				—	4	—			ICLK = 1 MHz ICLK = 32.768 kHz
	Low-speed operating mode 2				—	1	—			
	Software standby mode				—	0.2	6			
	Deep software standby mode	Power supplied to RAM and USB resume detecting unit			—	22	200	μA		
		Power not supplied to RAM and USB resume detecting unit	Power-on reset circuit and low-power function enabled consumption function disabled		—	21	60			
			Power-on reset circuit and low-power function enabled consumption function enabled		—	6.2	28			
		Increased by RTC operation			—	3	—			
		RTC operation when VCC is off			—	1.7	—		V _{BATT} = 2.3 V	
						—	3.3	—	V _{BATT} = 3.3 V	
Analog power supply current*7	During 12-bit A/D conversion (including temperature sensor)			I _{AVCC0}	—	2.3	3.2	mA		
	During 10-bit A/D conversion			I _{VREFH} *7	—	1.0	1.65			
	During D/A conversion (per unit)				—	0.7	1.0			
	Waiting for A/D, D/A conversion (all units)*8			—	—	25	35		μA	
	A/D, D/A converter in standby mode (all units)*8				—	0.1	4.0		μA	
Reference power supply current	During 12-bit A/D conversion			I _{VREFH0}	—	0.6	0.7	mA		
	Waiting for 12-bit A/D conversion (per unit)				—	0.5	0.6			
	12-bit A/D converter in standby mode (per unit)				—	0.1	2.0		μA	
RAM standby voltage				V _{RAM}	2.7	—	—	V		
VCC rising gradient				SrVCC	8.4	—	20000	μs/V		
VCC falling gradient*8				SfVCC	8.4	—	—	μs/V		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.

Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK:PCLK:BCLK:BCLK pin = 8:4:4:2)

I_{CC} Max. = 0.87 × f + 13 (max. operation in high-speed operating mode)

I_{CC} Typ. = 0.35 × f + 5 (normal operation in high-speed operating mode)

I_{CC} Typ. = 1.0 × f + 3 (low-speed operating mode 1)

I_{CC} Max. = 0.48 × f + 12 (sleep mode)

Note 4. This does not include the BGO operation.

Note 5. This is the increase for programming or erasure of the ROM or flash memory for data storage during program execution.

Note 6. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

Note 7. The current values for 10-bit A/D converter and 10-bit D/A converter are included in the current from the VREFH pin.

Note 8. The values are the sum of I_{AVCC0} and I_{VREFH}.

5.3 AC Characteristics

Table 5.7 Operation Frequency Value (High-Speed Operating Mode)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

	Item	Symbol	Min.	Typ.	Max.	Unit
Operation frequency	System clock (ICLK)	f	—	—	100	MHz
	Peripheral module clock (PCLKB)		—*1	—	50	
	FlashIF clock (FCLK)		—*2	—	50	
	External bus clock (BCLK)		—	—	50	
	BCLK pin output		—	—	25	
	USB clock (UCLK)		—	—	48	
	IEBUS clock (IECLK)		—	—	44.03	

Note 1. The PCLKB must run at a frequency of at least 24 MHz if the USB is in use.

Note 2. The FCLK must run at a frequency of at least 4 MHz when changing the ROM or E2 DataFlash memory contents.

Table 5.8 Operation Frequency Value (Low-Speed Operating Mode 1)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

	Item	Symbol	Min.	Typ.	Max.	Unit
Operation frequency	System clock (ICLK)	f	—	—	1	MHz
	Peripheral module clock (PCLKB)		—	—	1	
	FlashIF clock (FCLK)		—	—	1	
	External bus clock (BCLK)		—	—	1	
	BCLK pin output		—	—	1	
	USB clock (UCLK)		—	—	1	
	IEBUS clock (IECLK)		—	—	1	

Table 5.9 Operation Frequency Value (Low-Speed Operating Mode 2)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

	Item	Symbol	Min.	Typ.	Max.	Unit
Operation frequency	System clock (ICLK)	f	32	—	143.75	kHz
	Peripheral module clock (PCLKB)		—	—	143.75	
	FlashIF clock (FCLK)		32	—	143.75	
	External bus clock (BCLK)		—	—	143.75	
	BCLK pin output		—	—	143.75	
	USB clock (UCLK)		—	—	143.75	
	IEBUS clock (IECLK)		—	—	143.75	

5.3.2 Clock Timing

Table 5.11 Clock Timing (Except for Sub-Clock Related)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, T_a = T_{opr}

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time		t _{Bcyc}	40	—	—	ns	Figure 5.3
BCLK pin output high pulse width		t _{CH}	15	—	—	ns	
BCLK pin output low pulse width		t _{CL}	15	—	—	ns	
BCLK pin output rising time		t _{Cr}	—	—	5	ns	
BCLK pin output falling time		t _{Cf}	—	—	5	ns	
EXTAL external clock input cycle time		t _{EXcyc}	50	—	—	ns	Figure 5.4
EXTAL external clock input high pulse width		t _{EXH}	20	—	—	ns	
EXTAL external clock input low pulse width		t _{EXL}	20	—	—	ns	
EXTAL external clock rising time		t _{EXr}	—	—	5	ns	
EXTAL external clock falling time		t _{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1		t _{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency		f _{MAIN}	4	—	16	MHz	
Main clock oscillation stabilization time (crystal)		t _{MAINOSC}	—	—	—*3	ms	Figure 5.5
Main clock oscillation stabilization wait time (crystal)		t _{MAINOSCWT}	—	—	—*4	ms	
LOCO and IWDTCCLK clock cycle time		t _{cyc}	6.96	8	9.4	μs	
LOCO and IWDTCCLK clock oscillation frequency		f _{LOCO}	106.25	125	143.75	kHz	
LOCO and IWDTCCLK clock oscillation stabilization wait time		t _{LOCOWT}	—	—	20	μs	Figure 5.6
HOCO clock oscillator oscillation frequency		f _{HOCO}	45	50	55	MHz	
HOCO clock oscillation stabilization wait time 1*2		t _{HOCOWT1}	—	—	1.8	ms	Figure 5.7
HOCO clock oscillation stabilization wait time 2		t _{HOCOWT2}	—	—	2.0	ms	Figure 5.8
HOCO clock power supply settling time		t _{HOCOP}	—	—	1	ms	Figure 5.9
PLL circuit oscillation frequency		f _{PLL}	104	—	200	MHz	
PLL clock oscillation stabilization time	PLL operation started after main clock oscillation has settled	t _{PLL1}	—	—	500	μs	Figure 5.10
PLL clock oscillation stabilization wait		t _{PLLWT1}	—	—	—*5	ms	
PLL clock oscillation stabilization time	PLL operation started before main clock oscillation has settled	t _{PLL2}	—	—	t _{MAINOSC} + t _{PLL1}	ms	Figure 5.11
PLL clock oscillation stabilization wait		t _{PLLWT2}	—	—	—*5	ms	

Note 1. This is the time until the clock is used after setting P36 and P37 as inputs, and then clearing the main clock oscillator stop bit (MOSCCR.MOSTP) to 0 (selecting operation).

Note 2. This is the time until the frequency of oscillation by the HOCO (f_{HOCO}) reaches the range for guaranteed operation. after release from the reset state.

Note 3. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 4. The number of cycles n selected by the value of the MOSCWTCR.MSTS[4:0] bits determines the main-clock oscillation stabilization waiting time in accord with the formula below.

$$t_{\text{MAINOSCWT}} = t_{\text{MAINOSC}} + \frac{n + 16384}{f_{\text{MAIN}}}$$

Note 5. The number of cycles n selected by the value of the PLLWTCR.PSTS[4:0] bits determines the PLL-clock oscillation stabilization waiting time in accord with the formula below.

$$t_{\text{PLLWT1}} = t_{\text{PLL1}} + \frac{n + 131072}{f_{\text{PLL}}}$$

$$t_{\text{PLLWT2}} = t_{\text{PLL2}} + \frac{n + 131072}{f_{\text{PLL}}} = t_{\text{MAINOSC}} + t_{\text{PLL1}} + \frac{n + 131072}{f_{\text{PLL}}}$$

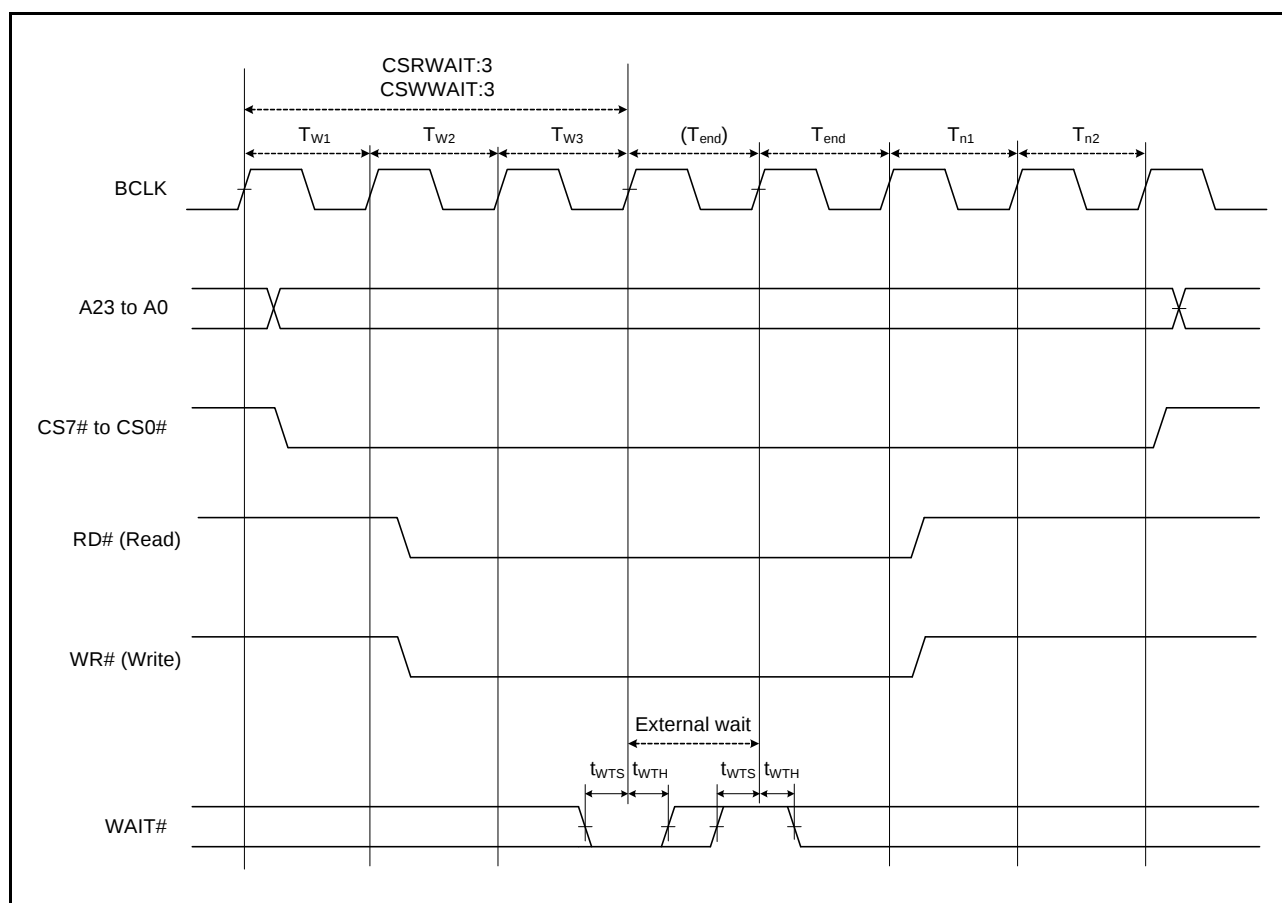


Figure 5.23 External Bus Timing/External Wait Control

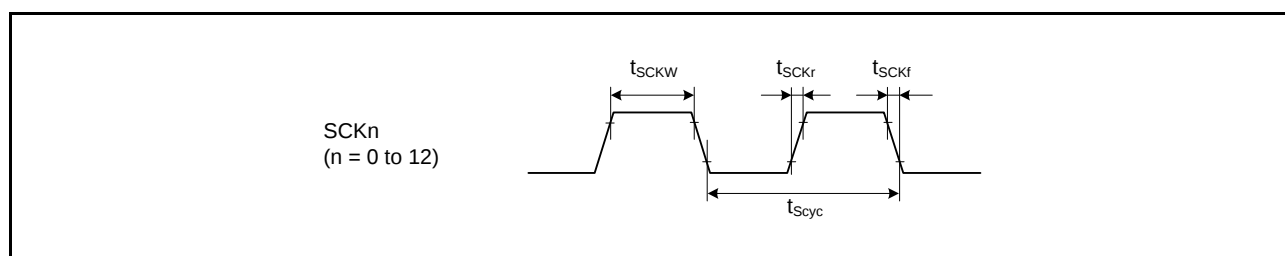


Figure 5.29 SCK Clock Input Timing

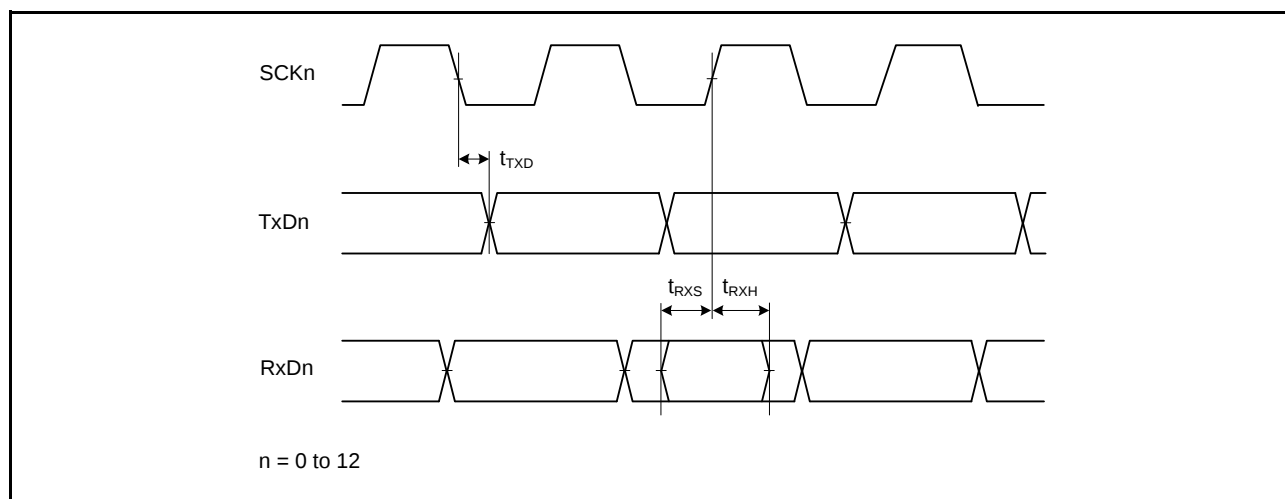


Figure 5.30 SCI Input/Output Timing: Clock Synchronous Mode

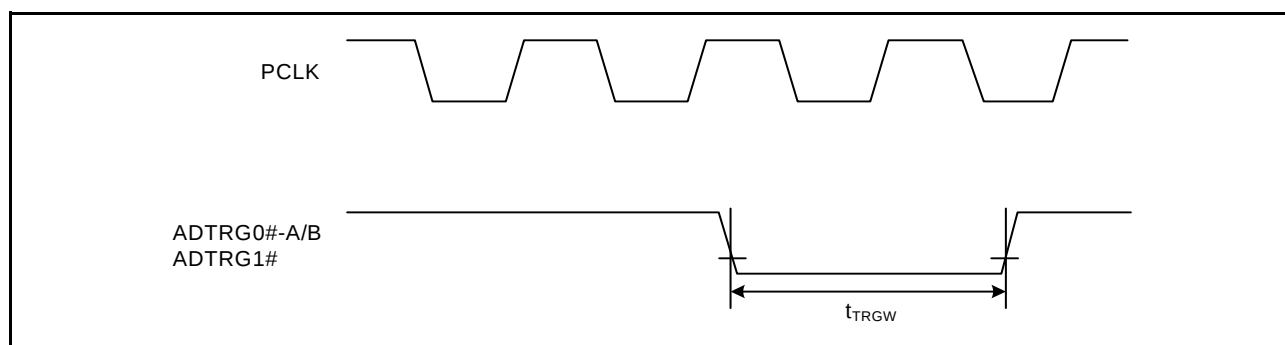


Figure 5.31 A/D Converter External Trigger Input Timing