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Details

Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	117
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5630ecdfb-v0

1.5 Pin Assignments

Figure 1.3 to Figure 1.10 show the pin assignments. Table 1.5 to Table 1.11 show the lists of pins and pin functions.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R								
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	PL0	PL1	PC1	15							
14	PE1	PE0	PK4	PE7	PG3	PA0	PA1	PA2	PA7	PK7	PB1	PB5	P73	P75	P74	14							
13	P63	P64	PE4	PK5	PG2	PG4	PG6	PA3	PK6	P71	PB3	PB7	PC0	PC2	P76	13							
12	P60	PK3	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12							
11	PD6	PG1	PK2	P61	RX630 Group PTLG0177KA-A (177-Pin TFLGA) (Upper perspective view)							P81	P82	PC6	VCC	11							
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10							
9	PK0	P96	PD3	PD5								P50	P51	P52	P84	9							
8	P94	PD1	PD2	PK1								P53	PL2	PL3	PL4	8							
7	VSS	P92	PD0	P95								P54	P55	VSS_ USB	USB0_ DP	7							
6	VCC	P91	P90	P93								P56	P57	VCC_ USB	USB0_ DM	6							
5	P46	P47	P45	P44	NC								P13	P12	P10	P11	5						
4	P42	P41	P43	P00	VSS								BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P85	4
3	VREFL0	P40	VREFH0	P03	PF5								PJ3	MD	RES#	P34	PF2	PF0	P24	P22	P87	P16	3
2	AVCC0	P07	VREFH	P02	EMLE								VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2
1	AVSS0	P05	VREFL	P01	PJ5								VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	PH5	PH4	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R								
Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).																							

Figure 1.3 Pin Assignment (177-Pin TFLGA)

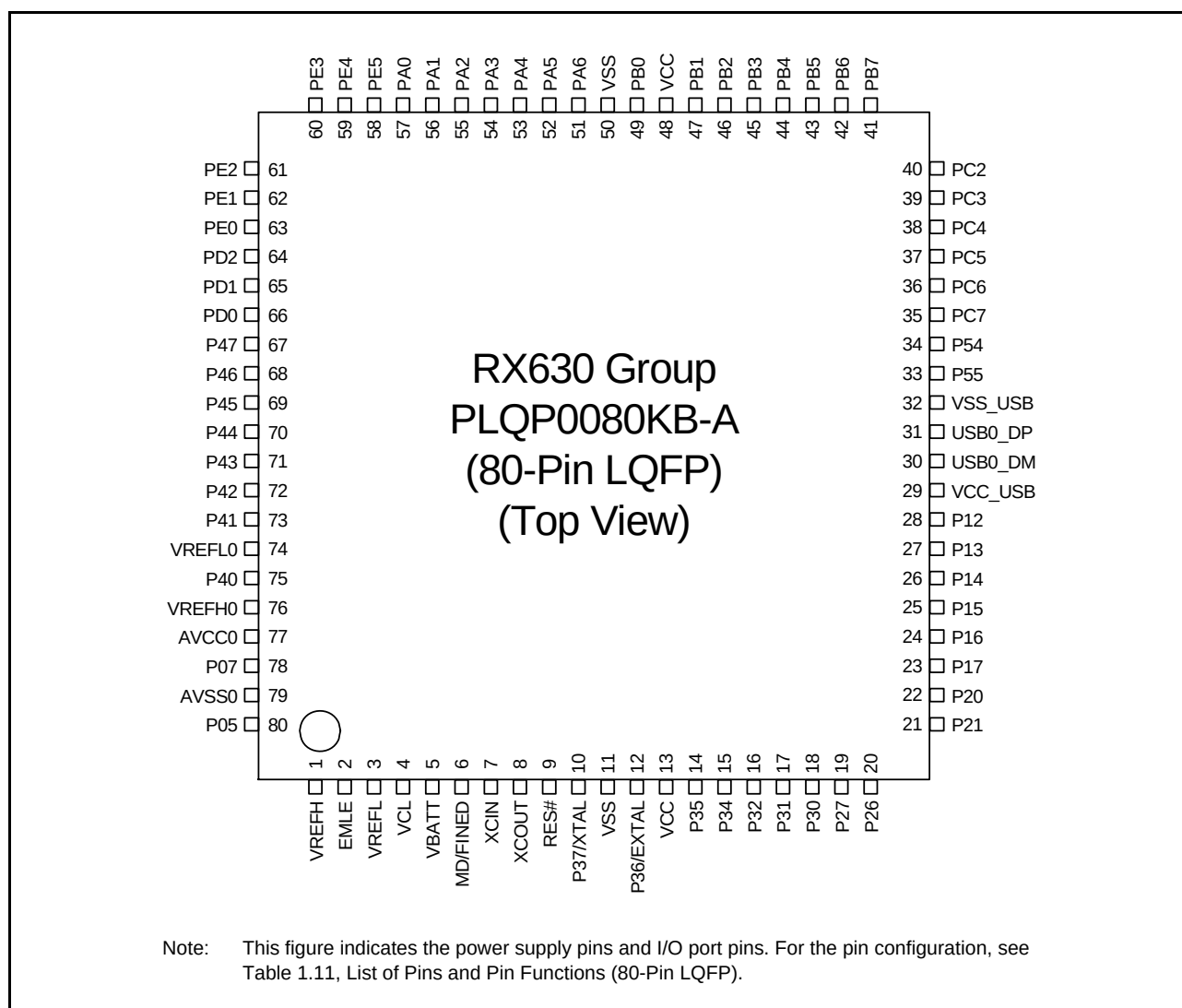


Figure 1.10 Pin Assignment (80-Pin LQFP)

Table 1.5 List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (3/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
H1	XTAL	P37					
H2	VSS						
H3	RES#						
H4		P35				NMI	
H12		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS	
H13		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/SSCL5	IRQ6-DS	
H14		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
H15	TRDATA3	PG7	D31				
J1	EXTAL	P36					
J2	VCC						
J3		P34		MTIOC0A/TMCI3/PO12/ POE2#	SCK6/SCK0	IRQ4	
J4	TMS	PF3					
J12		PA5	A5	TIOCB1/PO21	RSPCKA		
J13		PK6					
J14		PA7	A7	TIOCB2/PO23	MISOA		
J15		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	CTS5#/RTS5#/SS5#/ MOSIA		
K1		P33		MTIOC0D/TIOC0D/ TMRI3/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0	IRQ3-DS	
K2		P32		MTIOC0C/TIOCC0/ TMO3/PO10/RTCOUT/ RTCIC2	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0	IRQ2-DS	
K3	TDI	PF2			RXD1/SMISO1/SSCL1		
K4	TCK/FINEC	PF1			SCK1		
K12		PB2	A10	TIOCC3/TCLKC/PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#		
K13		P71	CS1#				
K14		PK7					
K15		PB0	A8	MTIC5W/TIOCA3/PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA	IRQ12	
L1		P31		MTIOC4D/TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0	IRQ1-DS	
L2		P30		MTIOC4B/TMRI3/PO8/ RTCIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB	IRQ0-DS	
L3	TDO	PF0			TXD1/SMOSI1/SSDA1		
L4		P25	CS5#	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3		ADTRG0#
L12		PB6	A14	MTIOC3D/TIOCA5/PO30	RXD9/SMISO9/SSCL9		
L13		PB3	A11	MTIOC0A/MTIOC4A/ TIOC0D/TCLKD/TMO0/ PO27/POE3#	SCK4/SCK6		
L14		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6	IRQ4-DS	
L15		P72	CS2#				
M1		P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB		
M2		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (3/4)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
H13		PA7	A7	TIOCB2/PO23	MISOA		
J1	TRST#	P34		MTIOC0A/TMCI3/PO12/ POE2#	SCK6/SCK0	IRQ4	
J2		P33		MTIOC0D/TIOC0D/ TMR13/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0	IRQ3-DS	
J3		P32		MTIOC0C/TIOCC0/TMO3/ PO10/RTICOUT/RTICIC2	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0	IRQ2-DS	
J4	TDI	P30		MTIOC4B/TMR13/PO8/ RTICIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB	IRQ0-DS	
J10		PB3	A11	MTIOC0A/MTIOC4A/ TIOC03/TCLKD/TMO0/ PO27/POE3#	SCK4/SCK6		
J11		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/SS9#		
J12		PB2	A10	TIOCC3/TCLKC/PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#		
J13		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6	IRQ4-DS	
K1	TCK/FINEC	P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB		
K2	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
K3	TMS	P31		MTIOC4D/TMCI2/PO9/ RTICIC1	CTS1#/RTS1#/SS1#/ SSLB0	IRQ1-DS	
K4		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS	IRQ5	
K5	TRDATA2	P54	ALE	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#/ CTX1		
K6		P53*2	BCLK				
K7		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
K8	VCC						
K9	TRDATA0	P80		MTIOC3B/PO26	SCK10		
K10		P76	CS6#	PO22	RXD11/SMISO11/SSCL11		
K11		PB7	A15	MTIOC3B/TIOCB5/PO31	TXD9/SMOSI9/SSDA9		
K12		PB6	A14	MTIOC3D/TIOCA5/PO30	RXD9/SMISO9/SSCL9		
K13		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE1#	SCK9		
L1		P25	CS5#	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3		ADTRG0#
L2		P23		MTIOC3D/MTCLKD/ TIOC03/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3		
L3		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTICOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS	IRQ6	ADTRG0#
L4		P24	CS4#	MTIOC4A/MTCLKA/ TIOCB4/TMR11/PO4	SCK3		
L5		P13		MTIOC0B/TIOCA5/TMO3/ PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
L6		P56		MTIOC3C/TIOCA1			
L7		P52	RD#		RXD2/SMISO2/SSCL2/ SSLB3		
L8	TRCLK	P83		MTIOC4C	CTS10#/RTS10#/SS10#		

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (4/4)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
L9		PC5	A21/CS2#/WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/ PO29	SCK8/RSPCKA		
L10		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TIOCC6/TCLKE/TMC11/ PO25/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0		
L11		PC2	A18	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/IERXD		
L12		P73	CS3#	PO16			
L13		PL0					
M1		P22		MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0		
M2		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/ IETXD	IRQ7	ADTRG#
M3		P86		TIOCA0			
M4		P12		TMC11	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
M5	VCC_USB						
M6	VSS_USB						
M7		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
M8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TIOCA6/TMC12/PO30	RXD8/SMISO8/SSCL8/ MOSIA	IRQ13	
M9	TRDATA1	P81		MTIOC3D/PO27	RXD10/SMISO10/SSCL10		
M10		P77	CS7#	PO23	TXD11/SMOSI11/SSDA11		
M11		PC0	A16	MTIOC3C/TCLKC/PO17	CTS5#/RTS5#/SS5#/ SSLA1/SCL3	IRQ14	
M12		PC1	A17	MTIOC3A/TCLKD/PO18	SCK5/SSLA2/SDA3	IRQ12	
M13		PL1					
N1		P21		MTIOC1B/TIOCA3/ TMC10/PO1	RXD0/SMISO0/SSCL0/ SCL1	IRQ9	
N2		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/SSDA0/ SDA1	IRQ8	
N3		P87		TIOCA2			
N4		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE	IRQ4	
N5					USB0_DM		
N6					USB0_DP		
N7	TRDATA3	P55	WAIT#	MTIOC4D/TMO3	CRX1	IRQ10	
N8	VSS						
N9		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA	IRQ14	
N10	TRSYNC#	P82		MTIOC4A/PO28	TXD10/SMOSI10/SSDA10		
N11		PC3	A19	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ IETXD		
N12		P75	CS5#	PO20	SCK11		
N13		P74	CS4#	PO19	CTS11#/RTS11#/SS11#		

Note 1. Enabled only for the ROM capacity: 2 MB/1.5 MB

Note 2. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (1/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
1	VREFH						
2	EMLE						
3	VREFL						
4		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
5	VCL						
6	VBATT						
7	MD/FINED						
8	XCIN						
9	XCOUT						
10	RES#						
11	XTAL	P37					
12	VSS						
13	EXTAL	P36					
14	VCC						
15		P35				NMI	
16	TRST#	P34		MTIOC0A/TMCi3/PO12/ POE2#	SCK6/SCK0	IRQ4	
17		P33		MTIOC0D/TIOC0D/ TMRI3/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0*1	IRQ3-DS	
18		P32		MTIOC0C/TIOCC0/TMO3/ PO10/RTCOU7/RTIC2	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0*1	IRQ2-DS	
19	TMS	P31		MTIOC4D/TMCi2/PO9/ RTIC1	CTS1#/RTS1#/SS1#/ SSLB0	IRQ1-DS	
20	TDI	P30		MTIOC4B/TMRI3/PO8/ RTIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB	IRQ0-DS	
21	TCK/FINEC	P27	CS7#	MTIOC2B/TMCi3/PO7	SCK1/RSPCKB		
22	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
23		P25	CS5#	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3		ADTRG0#
24		P24	CS4#	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3		
25		P23		MTIOC3D/MTCLKD/ TIOC03/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3		
26		P22		MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0		
27		P21		MTIOC1B/TIOCA3/ TMCi0/PO1	RXD0/SMISO0/SSCL0	IRQ9	
28		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/SSDA0	IRQ8	
29		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/ IETXD	IRQ7	ADTRG#
30		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOU7	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/ MOSIA/SCL2-DS/IEXD/ USB0_VBUS	IRQ6	ADTRG0#
31		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCi2/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS	IRQ5	
32		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE	IRQ4	

Table 4.1 List of I/O Registers (Address Order) (8/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7127h	ICU	DTC activation enable register 039	DTCER039	8	8	2 ICLK		ICUb
0008 7128h	ICU	DTC activation enable register 040	DTCER040	8	8	2 ICLK		
0008 712Ah	ICU	DTC activation enable register 042	DTCER042	8	8	2 ICLK		
0008 712Bh	ICU	DTC activation enable register 043	DTCER043	8	8	2 ICLK		
0008 712Dh	ICU	DTC activation enable register 045	DTCER045	8	8	2 ICLK		
0008 712Eh	ICU	DTC activation enable register 046	DTCER046	8	8	2 ICLK		
0008 7140h	ICU	DTC activation enable register 064	DTCER064	8	8	2 ICLK		
0008 7141h	ICU	DTC activation enable register 065	DTCER065	8	8	2 ICLK		
0008 7142h	ICU	DTC activation enable register 066	DTCER066	8	8	2 ICLK		
0008 7143h	ICU	DTC activation enable register 067	DTCER067	8	8	2 ICLK		
0008 7144h	ICU	DTC activation enable register 068	DTCER068	8	8	2 ICLK		
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8	2 ICLK		
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8	2 ICLK		
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8	2 ICLK		
0008 7148h	ICU	DTC activation enable register 072	DTCER072	8	8	2 ICLK		
0008 7149h	ICU	DTC activation enable register 073	DTCER073	8	8	2 ICLK		
0008 714Ah	ICU	DTC activation enable register 074	DTCER074	8	8	2 ICLK		
0008 714Bh	ICU	DTC activation enable register 075	DTCER075	8	8	2 ICLK		
0008 714Ch	ICU	DTC activation enable register 076	DTCER076	8	8	2 ICLK		
0008 714Dh	ICU	DTC activation enable register 077	DTCER077	8	8	2 ICLK		
0008 714Eh	ICU	DTC activation enable register 078	DTCER078	8	8	2 ICLK		
0008 714Fh	ICU	DTC activation enable register 079	DTCER079	8	8	2 ICLK		
0008 7162h	ICU	DTC activation enable register 098	DTCER098	8	8	2 ICLK		
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8	2 ICLK		
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8	2 ICLK		
0008 717Fh	ICU	DTC activation enable register 127	DTCER127	8	8	2 ICLK		
0008 7180h	ICU	DTC activation enable register 128	DTCER128	8	8	2 ICLK		
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8	2 ICLK		
0008 7182h	ICU	DTC activation enable register 130	DTCER130	8	8	2 ICLK		
0008 7183h	ICU	DTC activation enable register 131	DTCER131	8	8	2 ICLK		
0008 7184h	ICU	DTC activation enable register 132	DTCER132	8	8	2 ICLK		
0008 7185h	ICU	DTC activation enable register 133	DTCER133	8	8	2 ICLK		
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8	2 ICLK		
0008 7187h	ICU	DTC activation enable register 135	DTCER135	8	8	2 ICLK		
0008 7188h	ICU	DTC activation enable register 136	DTCER136	8	8	2 ICLK		
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8	2 ICLK		
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8	2 ICLK		
0008 718Bh	ICU	DTC activation enable register 139	DTCER139	8	8	2 ICLK		
0008 718Ch	ICU	DTC activation enable register 140	DTCER140	8	8	2 ICLK		
0008 718Dh	ICU	DTC activation enable register 141	DTCER141	8	8	2 ICLK		
0008 718Eh	ICU	DTC activation enable register 142	DTCER142	8	8	2 ICLK		
0008 718Fh	ICU	DTC activation enable register 143	DTCER143	8	8	2 ICLK		
0008 7190h	ICU	DTC activation enable register 144	DTCER144	8	8	2 ICLK		
0008 7191h	ICU	DTC activation enable register 145	DTCER145	8	8	2 ICLK		
0008 7194h	ICU	DTC activation enable register 148	DTCER148	8	8	2 ICLK		
0008 7195h	ICU	DTC activation enable register 149	DTCER149	8	8	2 ICLK		
0008 7196h	ICU	DTC activation enable register 150	DTCER150	8	8	2 ICLK		
0008 7197h	ICU	DTC activation enable register 151	DTCER151	8	8	2 ICLK		
0008 7198h	ICU	DTC activation enable register 152	DTCER152	8	8	2 ICLK		
0008 7199h	ICU	DTC activation enable register 153	DTCER153	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (13/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8	2 ICLK		ICUb
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8	2 ICLK		
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8	2 ICLK		
0008 7508h	ICU	IRQ control register 8	IRQCR8	8	8	2 ICLK		
0008 7509h	ICU	IRQ control register 9	IRQCR9	8	8	2 ICLK		
0008 750Ah	ICU	IRQ control register 10	IRQCR10	8	8	2 ICLK		
0008 750Bh	ICU	IRQ control register 11	IRQCR11	8	8	2 ICLK		
0008 750Ch	ICU	IRQ control register 12	IRQCR12	8	8	2 ICLK		
0008 750Dh	ICU	IRQ control register 13	IRQCR13	8	8	2 ICLK		
0008 750Eh	ICU	IRQ control register 14	IRQCR14	8	8	2 ICLK		
0008 750Fh	ICU	IRQ control register 15	IRQCR15	8	8	2 ICLK		
0008 7510h	ICU	IRQ pin digital filter enable register 0	IRQFLTE0	8	8	2 ICLK		
0008 7511h	ICU	IRQ pin digital filter enable register 1	IRQFLTE1	8	8	2 ICLK		
0008 7514h	ICU	IRQ pin digital filter setting register 0	IRQFLTC0	8	8	2 ICLK		
0008 7516h	ICU	IRQ pin digital filter setting register 1	IRQFLTC1	8	8	2 ICLK		
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 ICLK		
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 ICLK		
0008 7582h	ICU	Non-maskable interrupt status clear register	NMICLR	8	8	2 ICLK		
0008 7583h	ICU	NMI pin interrupt control register	NMICR	8	8	2 ICLK		
0008 7590h	ICU	NMI pin digital filter enable register	NMIFLTE	8	8	2 ICLK		
0008 7594h	ICU	NMI pin digital filter setting register	NMIFLTC	8	8	2 ICLK		
0008 8000h	CMT	Compare match timer start register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8010h	CMT	Compare match timer start register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK	
0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8020h	WDT	WDT refresh register	WDTRR	8	8	2, 3 PCLKB	2 ICLK	WDTa
0008 8022h	WDT	WDT control register	WDTCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8024h	WDT	WDT status register	WDTSR	16	16	2, 3 PCLKB	2 ICLK	
0008 8026h	WDT	WDT reset control register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8030h	IWDT	IWDT refresh register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK	IWDTa
0008 8032h	IWDT	IWDT control register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8034h	IWDT	IWDT status register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK	
0008 8036h	IWDT	IWDT reset control register	IWDTRCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8038h	IWDT	IWDT count stop control register	IWDTCSTPR	8	8	2, 3 PCLKB	2 ICLK	
0008 80C0h	DA	D/A data register 0	DADR0	16	16	2, 3 PCLKB	2 ICLK	DAa
0008 80C2h	DA	D/A data register 1	DADR1	16	16	2, 3 PCLKB	2 ICLK	
0008 80C4h	DA	D/A control register	DACR	8	8	2, 3 PCLKB	2 ICLK	
0008 80C5h	DA	DADRm format select register	DADPR	8	8	2, 3 PCLKB	2 ICLK	
0008 80C6h	DA	D/A A/D synchronous start control register	DAADSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8100h	TPUA	Timer start register	TSTR	8	8	2, 3 PCLKB	2 ICLK	TPUa

Table 4.1 List of I/O Registers (Address Order) (16/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 81B4h	TPU9	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 81B5h	TPU9	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B6h	TPU9	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81B8h	TPU9	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81BAh	TPU9	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81BCh	TPU9	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 81BEh	TPU9	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 81C0h	TPU10	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C1h	TPU10	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C2h	TPU10	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C4h	TPU10	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81C5h	TPU10	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C6h	TPU10	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81C8h	TPU10	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81CAh	TPU10	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81D0h	TPU11	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D1h	TPU11	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D2h	TPU11	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D4h	TPU11	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81D5h	TPU11	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D6h	TPU11	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	PPG
0008 81D8h	TPU11	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81DAh	TPU11	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81E6h	PPG0	PPG output control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81E7h	PPG0	PPG output mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 81E8h	PPG0	Next data enable register H	NDERH	8	8	2, 3 PCLKB	2 ICLK	
0008 81E9h	PPG0	Next data enable register L	NDERL	8	8	2, 3 PCLKB	2 ICLK	
0008 81EAh	PPG0	Output data register H	PODRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81EBh	PPG0	Output data register L	PODRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81ECh*1	PPG0	Next data register H	NDRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81EDh*2	PPG0	Next data register L	NDRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81EEh*1	PPG0	Next data register H	NDRH2	8	8	2, 3 PCLKB	2 ICLK	
0008 81EFh*2	PPG0	Next data register L	NDRL2	8	8	2, 3 PCLKB	2 ICLK	
0008 81F0h	PPG1	PPG trigger select register	PTRSLR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F6h	PPG1	PPG output control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F7h	PPG1	PPG output mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F8h	PPG1	Next data enable register H	NDERH	8	8	2, 3 PCLKB	2 ICLK	
0008 81F9h	PPG1	Next data enable register L	NDERL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FAh	PPG1	Output data register H	PODRH	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 81FBh	PPG1	Output data register L	PODRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FCh*3	PPG1	Next data register H	NDRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81FDh*4	PPG1	Next data register L	NDRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FEh*3	PPG1	Next data register H	NDRH2	8	8	2, 3 PCLKB	2 ICLK	
0008 81FFh*4	PPG1	Next data register L	NDRL2	8	8	2, 3 PCLKB	2 ICLK	
0008 8200h	TMR0	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8201h	TMR1	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8202h	TMR0	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8203h	TMR1	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8204h	TMR0	Time constant register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8205h	TMR1	Time constant register A	TCORA	8	8*5	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (26/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A10Bh	SCI8	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId
0008 A10Ch	SCI8	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A10Dh	SCI8	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A120h	SCI9	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A121h	SCI9	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A122h	SCI9	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A123h	SCI9	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A124h	SCI9	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A125h	SCI9	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A126h	SCI9	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A127h	SCI9	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A128h	SCI9	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A129h	SCI9	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A12Ah	SCI9	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A12Bh	SCI9	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A12Ch	SCI9	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A12Dh	SCI9	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A140h	SCI10	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A141h	SCI10	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A142h	SCI10	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A143h	SCI10	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A144h	SCI10	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A145h	SCI10	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A146h	SCI10	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A147h	SCI10	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A148h	SCI10	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A149h	SCI10	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	IEB
0008 A14Ah	SCI10	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A14Bh	SCI10	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A14Ch	SCI10	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A14Dh	SCI10	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A160h	SCI11	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A161h	SCI11	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A162h	SCI11	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A163h	SCI11	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A164h	SCI11	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A165h	SCI11	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A166h	SCI11	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A167h	SCI11	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A168h	SCI11	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A169h	SCI11	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A16Ah	SCI11	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A16Bh	SCI11	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A16Ch	SCI11	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A16Dh	SCI11	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A800h	IEB	IEBus control register	IECTR	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 A801h	IEB	IEBus command register	IECMR	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 A802h	IEB	IEBus master control register	IEMCR	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 A803h	IEB	IEBus master unit address register 1	IEAR1	8	8	3, 4 PCLKB	2, 3 ICLK	
0008 A804h	IEB	IEBus master unit address register 2	IEAR2	8	8	3, 4 PCLKB	2, 3 ICLK	

Table 4.1 List of I/O Registers (Address Order) (30/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C08Eh	PORT7	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C08Fh	PORT7	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C090h	PORT8	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C091h	PORT8	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C092h	PORT9	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C093h	PORT9	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C094h	PORTA	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C095h	PORTA	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C096h	PORTB	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C097h	PORTB	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C098h	PORTC	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C099h	PORTC	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Ah	PORTD	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Bh	PORTD	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Ch	PORTE	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Dh	PORTE	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Eh	PORTF	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Fh	PORTF	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A0h	PORTG	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A1h	PORTG	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A3h	PORTH	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A4h	PORTJ	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A5h	PORTJ	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A6h	PORTK	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A7h	PORTK	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A8h	PORTL	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A9h	PORTL	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0C0h	PORT0	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C1h	PORT1	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C2h	PORT2	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C3h	PORT3	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C4h	PORT4	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C5h	PORT5	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C6h	PORT6	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C7h	PORT7	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C8h	PORT8	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C9h	PORT9	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CAh	PORTA	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CBh	PORTB	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CCh	PORTC	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CDh	PORTD	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CEh	PORTE	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CFh	PORTF	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0D0h	PORTG	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0D1h	PORTH	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0D2h	PORTJ	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0D3h	PORTK	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0D4h	PORTL	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E0h	PORT0	Driving ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E2h	PORT2	Driving ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (33/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C1A4h	MPC	PC4 pin function control register	PC4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A5h	MPC	PC5 pin function control register	PC5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A6h	MPC	PC6 pin function control register	PC6PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A7h	MPC	PC7 pin function control register	PC7PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A8h	MPC	PD0 pin function control register	PD0PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A9h	MPC	PD1 pin function control register	PD1PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1AAh	MPC	PD2 pin function control register	PD2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1ABh	MPC	PD3 pin function control register	PD3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1ACh	MPC	PD4 pin function control register	PD4PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1ADh	MPC	PD5 pin function control register	PD5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1AEh	MPC	PD6 pin function control register	PD6PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1AFh	MPC	PD7 pin function control register	PD7PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B0h	MPC	PE0 pin function control register	PE0PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B1h	MPC	PE1 pin function control register	PE1PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B2h	MPC	PE2 pin function control register	PE2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B3h	MPC	PE3 pin function control register	PE3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B4h	MPC	PE4 pin function control register	PE4PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B5h	MPC	PE5 pin function control register	PE5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B6h	MPC	PE6 pin function control register	PE6PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B7h	MPC	PE7 pin function control register	PE7PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B8h	MPC	PF0 pin function control register	PF0PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B9h	MPC	PF1 pin function control register	PF1PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1BAh	MPC	PF2 pin function control register	PF2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1BDh	MPC	PF5 pin function control register	PF5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1D3h	MPC	PJ3 pin function control register	PJ3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1DAh	MPC	PK2 pin function control register	PK2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1DBh	MPC	PK3 pin function control register	PK3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1DCh	MPC	PK4 pin function control register	PK4PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1DDh	MPC	PK5 pin function control register	PK5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C280h	SYSTEM	Deep standby control register	DPSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C282h	SYSTEM	Deep standby interrupt enable register 0	DPSIER0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C283h	SYSTEM	Deep standby interrupt enable register 1	DPSIER1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C284h	SYSTEM	Deep standby interrupt enable register 2	DPSIER2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C285h	SYSTEM	Deep standby interrupt enable register 3	DPSIER3	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C286h	SYSTEM	Deep standby interrupt flag register 0	DPSIFR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C287h	SYSTEM	Deep standby interrupt flag register 1	DPSIFR1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C288h	SYSTEM	Deep standby interrupt flag register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C289h	SYSTEM	Deep standby interrupt flag register 3	DPSIFR3	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Ah	SYSTEM	Deep standby interrupt edge register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Bh	SYSTEM	Deep standby interrupt edge register 1	DPSIEGR1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Ch	SYSTEM	Deep standby interrupt edge register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Dh	SYSTEM	Deep standby interrupt edge register 3	DPSIEGR3	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C290h	SYSTEM	Reset status register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK	Resets
0008 C291h	SYSTEM	Reset status register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C293h	SYSTEM	Main clock oscillator forced oscillation control register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit
0008 C294h	SYSTEM	High-speed on-chip oscillator power supply control register	HOCOPCR	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C296h	FLASH	Flash write erase protection register	FWEPROR	8	8	4, 5 PCLKB	2, 3 ICLK	ROM

Table 4.1 List of I/O Registers (Address Order) (35/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C42Ah	RTC	Frequency register H	RFRH	16	16	2, 3 PCLKB	2 ICLK	RTCa
0008 C42Ch	RTC	Frequency register L	RFRL	16	16	2, 3 PCLKB	2 ICLK	
0008 C42Eh	RTC	Time error adjustment register	RADJ	8	8	2, 3 PCLKB	2 ICLK	
0008 C440h	RTC	Time capture control register 0	RTCCR0	8	8	2, 3 PCLKB	2 ICLK	
0008 C442h	RTC	Time capture control register 1	RTCCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 C444h	RTC	Time capture control register 2	RTCCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 C452h	RTC	Second capture register 0	RSECCP0	8	8	2, 3 PCLKB	2 ICLK	
0008 C454h	RTC	Minute capture register 0	RMINCP0	8	8	2, 3 PCLKB	2 ICLK	
0008 C456h	RTC	Hour capture register 0	RHRCP0	8	8	2, 3 PCLKB	2 ICLK	
0008 C45Ah	RTC	Date capture register 0	RDAYCP0	8	8	2, 3 PCLKB	2 ICLK	
0008 C45Ch	RTC	Month capture register 0	RMONCP0	8	8	2, 3 PCLKB	2 ICLK	
0008 C462h	RTC	Second capture register 1	RSECCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C464h	RTC	Minute capture register 1	RMINCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C466h	RTC	Hour capture register 1	RHRCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C46Ah	RTC	Date capture register 1	RDAYCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C46Ch	RTC	Month capture register 1	RMONCP1	8	8	2, 3 PCLKB	2 ICLK	
0008 C472h	RTC	Second capture register 2	RSECCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C474h	RTC	Minute capture register 2	RMINCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C476h	RTC	Hour capture register 2	RHRCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C47Ah	RTC	Date capture register 2	RDAYCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C47Ch	RTC	Month capture register 2	RMONCP2	8	8	2, 3 PCLKB	2 ICLK	
0008 C500h	TEMPS	Temperature sensor control register	TSCR	8	8	2, 3 PCLKB	2 ICLK	Temperature Sensor
0008 C880h	SYSTEM	Counter-clock extension register 1	SCK1	8	8	2, 3 PCLKB	2 ICLK	MCK
0008 C890h	SYSTEM	Counter-clock extension register 2	SCK2	8	8	2, 3 PCLKB	2 ICLK	
0009 0200h to 0009 03FFh	CAN0	Mailbox registers 0 to 31	MB0 to 31	128	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 0400h to 0009 041Fh	CAN0	Mask registers 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0420h	CAN0	FIFO received ID compare register 0	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0424h	CAN0	FIFO received ID compare register 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0428h	CAN0	Mask invalid register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 042Ch	CAN0	Mailbox interrupt enable register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0820h to 0009 083Fh	CAN0	Message control registers 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK	
0009 0840h	CAN0	Control register	CTLR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 0842h	CAN0	Status register	STR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 0844h	CAN0	Bit configuration register	BCR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 0848h	CAN0	Receive FIFO control register	RFCR	8	8	2, 3 PCLKB	2 ICLK	
0009 0849h	CAN0	Receive FIFO pointer control register	RFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Ah	CAN0	Transmit FIFO control register	TFCR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Bh	CAN0	Transmit FIFO pointer control register	TFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Ch	CAN0	Error interrupt enable register	EIER	8	8	2, 3 PCLKB	2 ICLK	
0009 084Dh	CAN0	Error interrupt factor judge register	EIFR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Eh	CAN0	Receive error count register	RECR	8	8	2, 3 PCLKB	2 ICLK	
0009 084Fh	CAN0	Transmit error count register	TECR	8	8	2, 3 PCLKB	2 ICLK	
0009 0850h	CAN0	Error code store register	ECSR	8	8	2, 3 PCLKB	2 ICLK	
0009 0851h	CAN0	Channel search support register	CSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 0852h	CAN0	Mailbox search status register	MSSR	8	8	2, 3 PCLKB	2 ICLK	

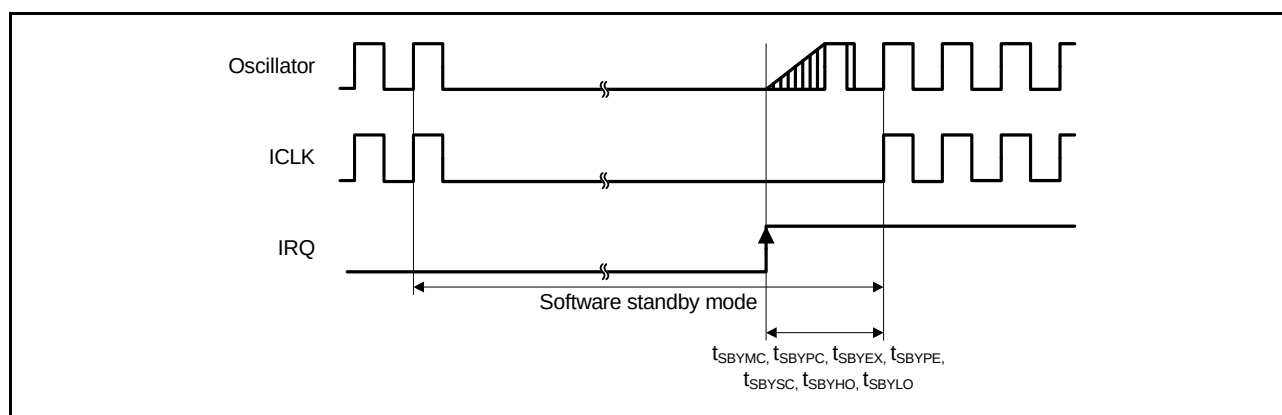


Figure 5.13 Software Standby Mode Cancellation Timing

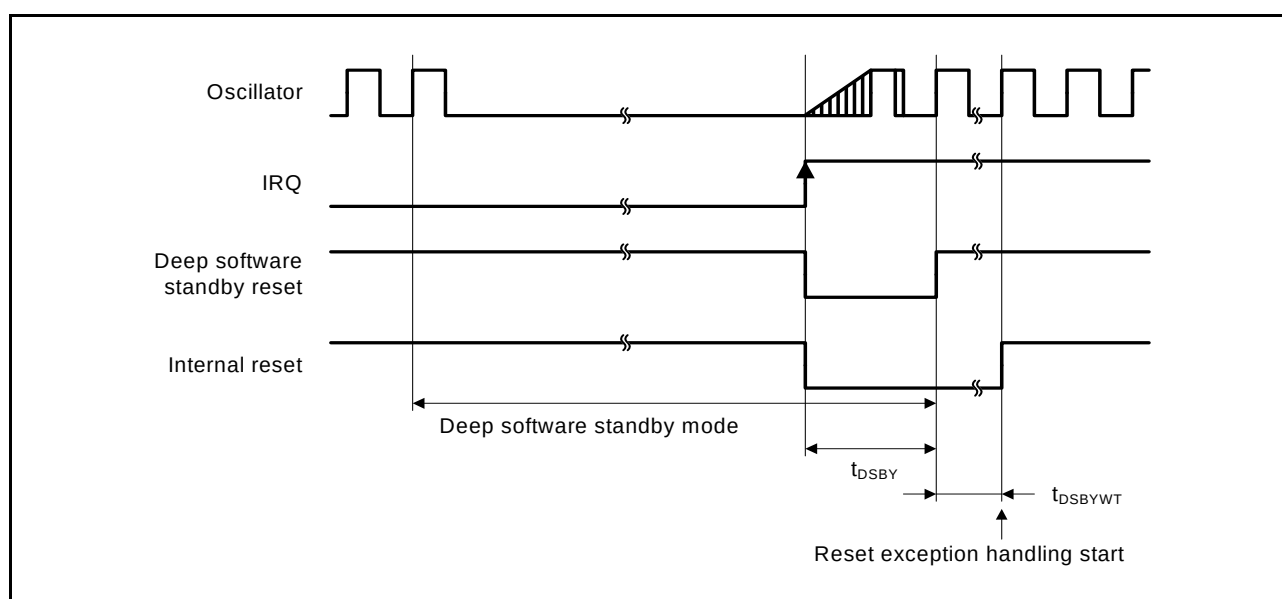


Figure 5.14 Deep Software Standby Mode Cancellation Timing

5.3.4 Control Signal Timing

Table 5.14 Control Signal Timing

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	$t_c (PCLK) \times 2 \leq 200$ ns Figure 5.15
		$t_c (PCLK) \times 2$				$t_c (PCLK) \times 2 > 200$ ns Figure 5.15
IRQ pulse width	t_{IRQW}	200	—	—	ns	$t_c (PCLK) \times 2 \leq 200$ ns Figure 5.16
		$t_c (PCLK) \times 2$				$t_c (PCLK) \times 2 > 200$ ns Figure 5.16

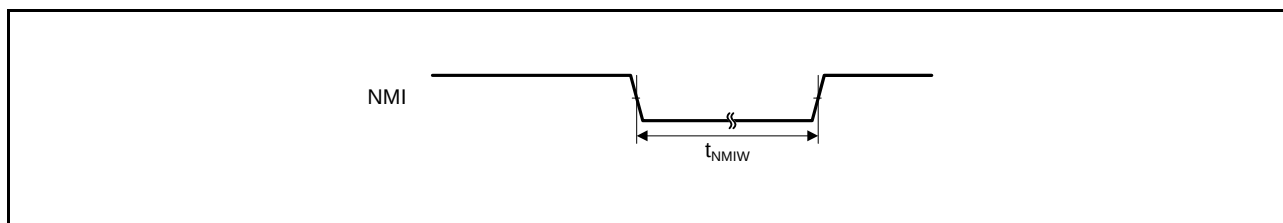


Figure 5.15 NMI Interrupt Input Timing

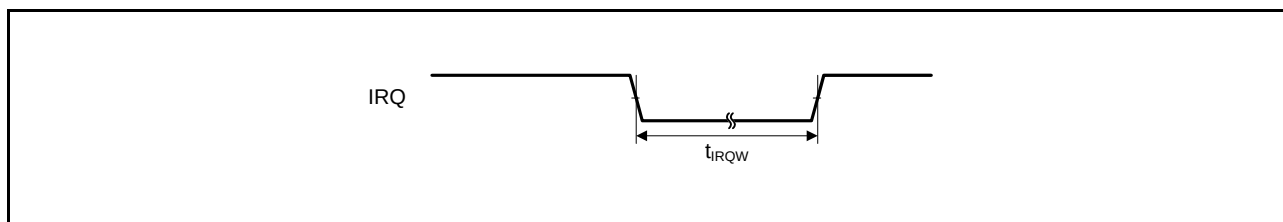


Figure 5.16 IRQ Interrupt Input Timing

5.3.5 Bus Timing

Table 5.15 Bus Timing

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V,
 $ICLK = 8$ to 100 MHz, $BCLK = 8$ to 50 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = VCC \times 0.5$, $V_{OL} = VCC \times 0.5$, $I_{OH} = -1.0$ mA, $I_{OL} = 1.0$ mA, $C = 30$ pF
 High drive output is selected by the drive capacity control register.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	20	ns	Figure 5.17 to Figure 5.22
Byte control delay time	t_{BCD}	—	20	ns	
CS# delay time	t_{CSD}	—	20	ns	
ALE delay time	t_{ALED}	—	20	ns	
RD# delay time	t_{RSD}	—	20	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	20	ns	
Write data delay time	t_{WDD}	—	20	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 5.23
WAIT# hold time	t_{WTH}	0	—	ns	

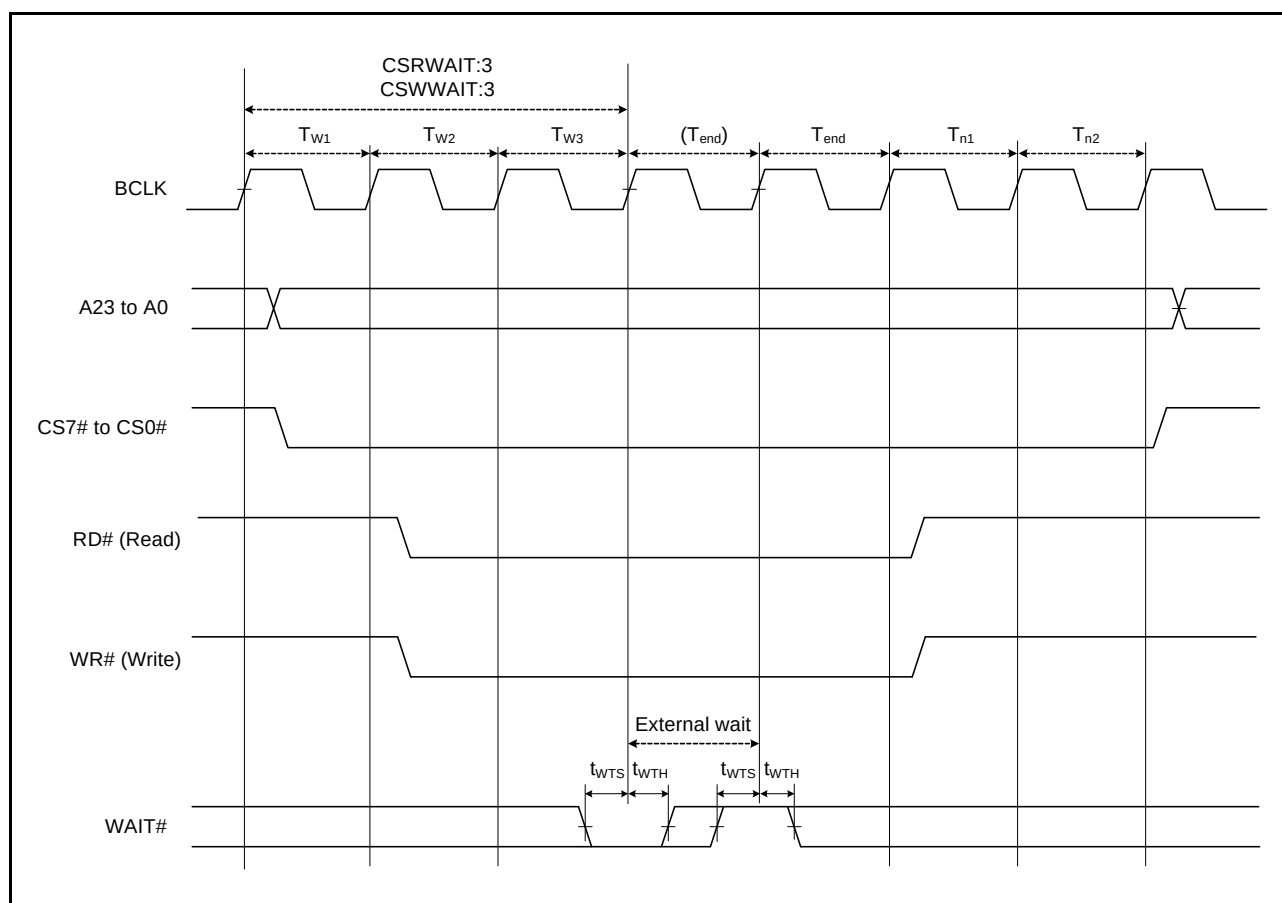


Figure 5.23 External Bus Timing/External Wait Control

Table 5.19 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0

VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

PCLK = 8 to 50 MHz

 $T_a = T_{opr}$

High drive output is selected by the drive capacity control register.

Item		Symb ol	Min.*1,*2	Max.	Unit	Test Conditions
RIIC (Standard-mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 1300$	—	ns	Figure 5.37
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 600$	—	ns	
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc} : RIIC internal reference clock (IIC ϕ) Cycle

Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 2. C_b is the total capacitance of the bus lines.

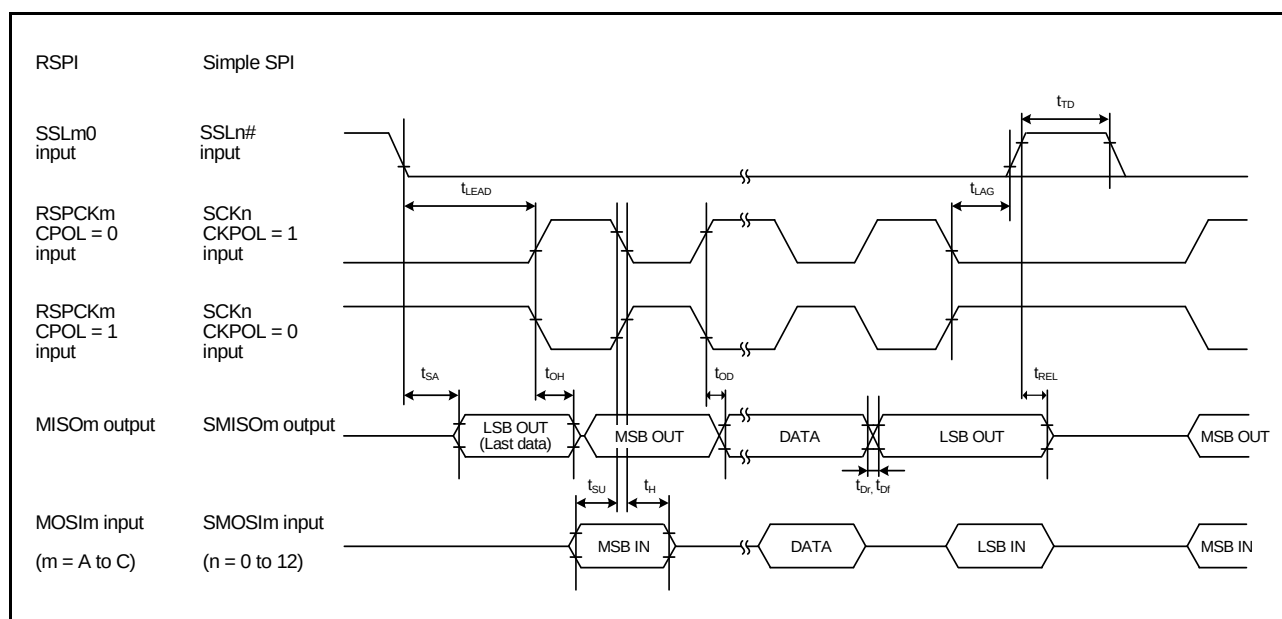


Figure 5.36 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

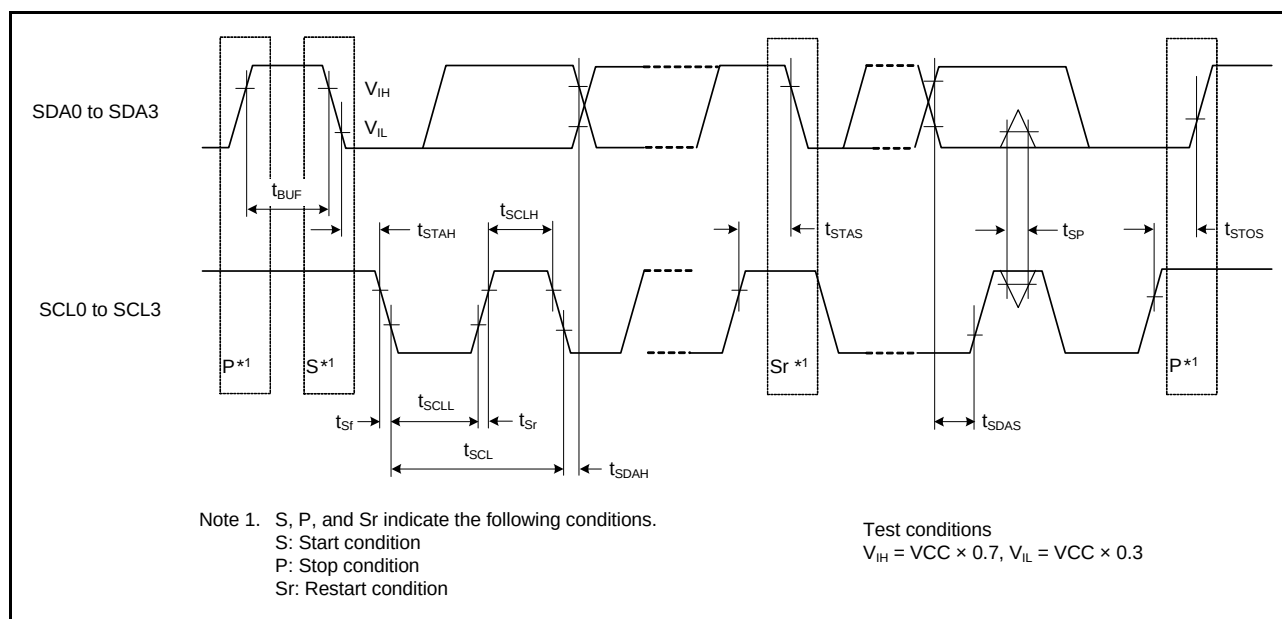


Figure 5.37 IIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

Table 5.23 12-Bit A/D Conversion CharacteristicsConditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$ $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V $PCLK = 8$ to 50 MHz $T_a = T_{opr}$

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			12	12	12	Bit	
Conversion time*1 (Operation at PCLK = 50 MHz)	AN0 to AN7	Permissible signal source impedance (max.) = 1.0 kΩ	1.0 (0.4)*2	—	—	μs	Sampling in 20 states
	Other channels	Permissible signal source impedance (max.) = 1.0 kΩ, AVCC ≥ 3.0 V	2.0 (1.4)*2	—	—	μs	Sampling in 70 states
		Permissible signal source impedance (max.) = 1.0 kΩ, AVCC ≥ 2.7 V	5.6 (5.0)*2	—	—	μs	Sampling in 250 states
Analog input capacitance			—	—	30	pF	
Offset error			—	±2.0	±7.5	LSB	
Full-scale error			—	±2.0	±7.5	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	±2.5	±8.0	LSB	
DNL differential nonlinearity error			—	±2.0	±4.0	LSB	
INL integral nonlinearity error			—	±2.0	±4.0	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.24 A/D Internal Reference Voltage CharacteristicsConditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$ $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V $PCLK = 8$ to 50 MHz $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
A/D Internal reference voltage	1.45	1.50	1.55	V	

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