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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	117
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5630eddfb-v0

Table 1.1 Outline of Specifications (5/5)

Classification	Module/Function	Description
10-bit A/D converter (ADb)		• 1 unit (1 unit × 8 channels) • 10-bit resolution • Conversion time: 1.0 μs per channel (in operation with PCLK at 50 MHz) • Operating mode - Scan mode (single scan mode or continuous scan mode) - External amplifier connection mode • Sample-and-hold function • Three ways to start A/D conversion - Conversion can be started by software, a conversion start trigger from a timer (MTU, TPU, or TMR), or an external trigger signal.
D/A converter (DAa)		• 2 channels • 10-bit resolution • Output voltage: 0 V to VREFH
Temperature sensor		• 1 channel • Precision: ± 1 °C • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter.
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
Unique ID		A 16-byte device-specific ID (only for the G version)
Operating frequency		Up to 100 MHz
Power supply voltage		VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0, Vbatt = 2.3 to 3.6 V
Operating temperature		D version: -40 to +85°C, G version: -40 to +105°C*1
Package		177-pin TFLGA (PTLG0177KA-A) (in planning) 176-pin LFBGA (PLBG0176GA-A) (in planning) 176-pin LQFP (PLQP0176KB-A) 145-pin TFLGA (PTLG0145KA-A) (in planning) 144-pin LQFP (PLQP0144KA-A) 100-pin TFLGA (PTLG0100KA-A) (in planning) 100-pin LQFP (PLQP0100KB-A) 80-pin LQFP (PLQP0080KB-A) (in planning)
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

Note 1. Please contact us if you are using a G version.

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part number.

Table 1.3 List of Products (1/2)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX630 (D version)	R5F56307CDFN	PLQP0080KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307DDFN	PLQP0080KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307CDFP	PLQP0100KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307DDFP	PLQP0100KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307CDLA	PTLG0100KA-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56307DDLA	PTLG0100KA-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308CDFN	PLQP0080KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308DDFN	PLQP0080KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308CDFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308DDFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308CDLA	PTLG0100KA-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56308DDLA	PTLG0100KA-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDFP*1	PLQP0100KB-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDFP*1	PLQP0100KB-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDFB*1	PLQP0144KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDFB*1	PLQP0144KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDLK*1	PTLG0145KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDLK*1	PTLG0145KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDFC	PLQP0176KB-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDFC	PLQP0176KB-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDBG	PLBG0176GA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDBG	PLBG0176GA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ACDLC	PTLG0177KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630ADDLC	PTLG0177KA-A	768 Kbytes	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDFP*1	PLQP0100KB-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDFP*1	PLQP0100KB-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDFB*1	PLQP0144KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDFB*1	PLQP0144KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDLK*1	PTLG0145KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDLK*1	PTLG0145KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDFC	PLQP0176KB-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDFC	PLQP0176KB-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDBG	PLBG0176GA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDBG	PLBG0176GA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BCDLC	PTLG0177KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630BDDLK	PTLG0177KA-A	1 Mbyte	96 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DCDFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DDDFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DCDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DDDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5630DCDLK	PTLG0145KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C

Table 1.4 Pin Functions (3/5)

Classifications	Pin Name	I/O	Description
16-bit timer pulse unit	TIOCA0, TIOCB0 TIOCC0, TIOCD0	I/O	The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins
	TIOCA1, TIOCB1	I/O	The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins
	TIOCA2, TIOCB2	I/O	The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins
	TIOCA3, TIOCB3 TIOCC3, TIOCD3	I/O	The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins
	TIOCA4, TIOCB4	I/O	The TGRA4 and TGRB4 input capture input/output compare output/ PWM output pins
	TIOCA5, TIOCB5	I/O	The TGRA5 and TGRB5 input capture input/output compare output/ PWM output pins
	TCLKA, TCLKB TCLKC, TCLKD	Input	Input pins for external clock signals
	TIOCA6, TIOCB6, TIOCC6, TIOCD6	I/O	The TGRA6 to TGRD6 input capture input/output compare output/ PWM output pins
	TIOCA7, TIOCB7	I/O	The TGRA7 and TGRB7 input capture input/output compare output/ PWM output pins
	TIOCA8, TIOCB8	I/O	The TGRA8 and TGRB8 input capture input/output compare output/ PWM output pins
	TIOCA9, TIOCB9, TIOCC9, TIOCD9	I/O	The TGRA9 to TGRD9 input capture input/output compare output/ PWM output pins
	TIOCA10, TIOCB10	I/O	The TGRA10 and TGRB10 input capture input/output compare output/PWM output pins
	TIOCA11, TIOCB11	I/O	The TGRA11 and TGRB11 input capture input/output compare output/PWM output pins
	TCLKE, TCLKF, TCLKG, TCLKH	Input	Input pins for external clock signals
Programmable pulse generator	PO0 to PO31	Output	Output pins for the pulse signals
8-bit timer	TMO0 to TMO3	Output	Compare match output pins
	TMCI0 to TMCI3	Input	Input pins for external clocks to be input to the counter
	TMRI0 to TMRI3	Input	Input pins for the counter reset
Serial communications interface (SCIC)	• Asynchronous mode/clock synchronous mode		
	SCK0 to SCK11	I/O	Input/output pins for the clock
	RXD0 to RXD11	Input	Input pins for received data
	TXD0 to TXD11	Output	Output pins for transmitted data
	CTS0# to CTS11#	Input	Input pins for controlling the start of transmission and reception
	RTS0# to RTS11#	Output	Output pins for controlling the start of transmission and reception
	• Simple I ² C mode		
	SSCL0 to SSCL11	I/O	Input/output pins for the I ² C clock
	SSDA0 to SSDA11	I/O	Input/output pins for the I ² C data
	• Simple SPI mode		
	SCK0 to SCK11	I/O	Input/output pins for the clock
	SMISO0 to SMISO11	I/O	Input/output pins for slave transmission of data
	SMOSI0 to SMOSI11	I/O	Input/output pins for master transmission of data
	SS0# to SS11#	Input	Chip-select input pins

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (1/4)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
A1	AVSS0						
A2		P07				IRQ15	ADTRG0#
A3		P40				IRQ8-DS	AN000
A4		P42				IRQ10-DS	AN002
A5		P45				IRQ13-DS	AN005
A6		P90	A16		TXD7/SMOSI7/SSDA7		AN014
A7		P92	A18		RXD7/SMISO7/SSCL7		AN016
A8		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010
A9		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
A10		PK3			RXD9/SMISO9/SSCL9		
A11		P62	CS2#				
A12		PE1	D9[A9/D9]	MTIOC4C/TIOCD9/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/RSPCKB		ANEX1
A13		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/PO26/ POE8#	CTS12#/RTS12#/SS12#/ MISOB		AN1
B1	VREFH						
B2	AVCC0						
B3		P05				IRQ13	DA1
B4	VREFL0						
B5		P43				IRQ11-DS	AN003
B6		P47				IRQ15-DS	AN007
B7		P91	A17		SCK7		AN015
B8		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
B9		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
B10		PK2			TXD9/SMOSI9/SSDA9		
B11		P61	CS1#		CTS9#/RTS9#/SS9#		
B12		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/PO23	RXD12/SMISO12/ SSCL12/RXDX12/SSLB3/ MOSIB	IRQ7-DS	AN0
B13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	SSLB0		AN2
C1	VREFL						
C2		P02		TMCI1	SCK6	IRQ10	AN020
C3	VREFH0						
C4		P41				IRQ9-DS	AN001
C5		P46				IRQ14-DS	AN006
C6	VSS						
C7		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
C8		PD3	D3[A3/D3]	TIOCB8/TCLKH/POE8#	RSPCKC	IRQ3	AN011
C9		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
C10		P63	CS3#				
C11		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0
C12		P70			SCK4		
C13		PK4			RXD4/SMISO4/SSCL4		
D1		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
D2		PF5				IRQ4	
D3		P03				IRQ11	DA0
D4		P01		TMCI0	RXD6/SMISO6/SSCL6	IRQ9	AN019

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (2/3)

Pin Number 100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
E4	TRST#	P34		MTIOC0A/TMC13/PO12/ POE2#	SCK6/SCK0	IRQ4	
E5		P41				IRQ9-DS	AN001
E6		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
E7		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMC13/PO22/ POE2#	CTS5#/RTS5#/SS5#/ MOSIA		
E8		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS	
E9		PA5	A5	TIOCB1/PO21	RSPCKA		
E10		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/SSCL5	IRQ6-DS	
F1	EXTAL	P36					
F2	VCC						
F3		P35				NMI	
F4		P32		MTIOC0C/TIOCC0/ TMO3/PO10/RTCOUT/ RTCIC2	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0*1	IRQ2-DS	
F5		P12		TMC11	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
F6		PB3	A11	MTIOC0A/MTIOC4A/ TIOC0D3/TCLKD/TMO0/ PO27/POE3#	SCK6		
F7		PB2	A10	TIOCC3/TCLKC/PO26	CTS6#/RTS6#/SS6#		
F8		PB0	A8	MTIC5W/TIOCA3/PO24	RXD6/SMISO6/SSCL6/ RSPCKA	IRQ12	
F9		PA7	A7	TIOCB2/PO23	MISOA		
F10	VSS						
G1		P33		MTIOC0D/TIOC0D/TMRI3 PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0*1	IRQ3-DS	
G2	TMS	P31		MTIOC4D/TMC12/PO9/ RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0	IRQ1-DS	
G3	TDI	P30		MTIOC4B/TMRI3/PO8/ RTCIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB	IRQ0-DS	
G4	TCK/FINEC	P27	CS7#	MTIOC2B/TMC13/ PO7	SCK1/RSPCKB		
G5		P53*2	BCLK				
G6		P52	RD#		RXD2/SMISO2/SSCL2/ SSLB3		
G7		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	SCK9		
G8		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/SS9#		
G9		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25	TXD6/SMOSI6/SSDA6	IRQ4-DS	
G10	VCC						
H1	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
H2		P25	CS5#	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3		ADTRG0#
H3		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/ MOSIA/SCL2-DS/IERXD/ USB_VBUS	IRQ6	ADTRG0#

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (3/3)

Pin Number 100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
H4		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMC12/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS	IRQ5	
H5		P55	WAIT#	MTIOC4D/TMO3	CRX1	IRQ10	
H6		P54	ALE	MTIOC4B/TMC11	CTS2#/RTS2#/SS2#/ CTX1		
H7		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA	IRQ14	
H8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMC12/PO30	RXD8/SMOSI8/SSCL8/ MOSIA	IRQ13	
H9		PB6	A14	MTIOC3D/TIOCA5/PO30	RXD9/SMOSI9/SSCL9		
H10		PB7	A15	MTIOC3B/TIOCB5/PO31	TXD9/SMOSI9/SSDA9		
J1		P24	CS4#	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3		
J2		P21		MTIOC1B/TIOCA3/ TMC10/PO1	RXD0/SMISO0/SSCL0	IRQ9	
J3		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/ IETXD	IRQ7	ADTRG#
J4		P13		MTIOC0B/TIOCA5/TMO3/ PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
J5	VSS_USB						
J6	VCC_USB						
J7		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
J8		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMC11/PO25/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0		
J9		PC0	A16	MTIOC3C/TCLKC/PO17	CTS5#/RTS5#/SS5#/ SSLA1	IRQ14	
J10		PC1	A17	MTIOC3A/TCLKD/PO18	SCK5/SSLA2	IRQ12	
K1		P23		MTIOC3D/MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3		
K2		P22		MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0		
K3		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/SSDA0	IRQ8	
K4		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE	IRQ4	
K5					USB0_DM		
K6					USB0_DP		
K7		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
K8		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TMRI2/PO29	SCK8/RSPCKA		
K9		PC3	A19	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ IETXD		
K10		PC2	A18	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/IERXD		

Note 1. Enabled only for the ROM capacity of 768 Kbytes or more

Note 2. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (3/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
67		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/SSCL5	IRQ6-DS	
68		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
69		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2	IRQ11	
70		PA0	A0/BC0#	MTIOC4A/TIOCA0/PO16	SSLA1		
71		PE7	D15[A15/D15]		MISOB	IRQ7	AN5
72		PE6	D14[A14/D14]		MOSIB	IRQ6	AN4
73		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B	RSPCKB	IRQ5	AN3
74		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ PO28	SSLB0		AN2
75		PE3	D11[A11/D11]	MTIOC4B/PO26/POE8#	CTS12#/RTS12#/SS12#/ MISOB		AN1
76		PE2	D10[A10/D10]	MTIOC4A/PO23	RXD12/SMISO12/ SSCL12/RXDX12/SSLB3/ MOSIB	IRQ7-DS	AN0
77		PE1	D9[A9/D9]	MTIOC4C/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/RSPCKB		ANEX1
78		PE0	D8[A8/D8]		SCK12/SSLB1		ANEX0
79		PD7	D7[A7/D7]	MTIC5U/POE0#		IRQ7	AN7
80		PD6	D6[A6/D6]	MTIC5V/POE1#		IRQ6	AN6
81		PD5	D5[A5/D5]	MTIC5W/POE2#		IRQ5	AN013
82		PD4	D4[A4/D4]	POE3#		IRQ4	AN012
83		PD3	D3[A3/D3]	POE8#		IRQ3	AN011
84		PD2	D2[A2/D2]	MTIOC4D	CRX0*1	IRQ2	AN010
85		PD1	D1[A1/D1]	MTIOC4B	CTX0*1	IRQ1	AN009
86		PD0	D0[A0/D0]			IRQ0	AN008
87		P47				IRQ15-DS	AN007
88		P46				IRQ14-DS	AN006
89		P45				IRQ13-DS	AN005
90		P44				IRQ12-DS	AN004
91		P43				IRQ11-DS	AN003
92		P42				IRQ10-DS	AN002
93		P41				IRQ9-DS	AN001
94	VREFL0						
95		P40				IRQ8-DS	AN000
96	VREFH0						
97	AVCC0						
98		P07				IRQ15	ADTRG0#
99	AVSS0						
100		P05				IRQ13	DA1

Note 1. Enabled only for the ROM capacity of 768 Kbytes or more

Note 2. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 1.11 List of Pins and Pin Functions (80-Pin LQFP) (3/3)

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
73		P41			IRQ9-DS	AN001
74	VREFL0					
75		P40			IRQ8-DS	AN000
76	VREFH0					
77	AVCC0					
78		P07			IRQ15	ADTRG0#
79	AVSS0					
80		P05			IRQ13	DA1

Table 4.1 List of I/O Registers (Address Order) (2/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 2014h	DMAC0	DMA address mode register	DMAMD	16	16	2 ICLK		DMACA
0008 2018h	DMAC0	DMA offset register	DMOFR	32	32	2 ICLK		
0008 201Ch	DMAC0	DMA transfer enable register	DMCNT	8	8	2 ICLK		
0008 201Dh	DMAC0	DMA software start register	DMREQ	8	8	2 ICLK		
0008 201Eh	DMAC0	DMA status register	DMSTS	8	8	2 ICLK		
0008 201Fh	DMAC0	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 2040h	DMAC1	DMA source address register	DMSAR	32	32	2 ICLK		
0008 2044h	DMAC1	DMA destination address register	DMDAR	32	32	2 ICLK		
0008 2048h	DMAC1	DMA transfer count register	DMCRA	32	32	2 ICLK		
0008 204Ch	DMAC1	DMA block transfer count register	DMCRB	16	16	2 ICLK		
0008 2050h	DMAC1	DMA transfer mode register	DMTMD	16	16	2 ICLK		
0008 2053h	DMAC1	DMA interrupt setting register	DMINT	8	8	2 ICLK		
0008 2054h	DMAC1	DMA address mode register	DMAMD	16	16	2 ICLK		
0008 205Ch	DMAC1	DMA transfer enable register	DMCNT	8	8	2 ICLK		
0008 205Dh	DMAC1	DMA software start register	DMREQ	8	8	2 ICLK		
0008 205Eh	DMAC1	DMA status register	DMSTS	8	8	2 ICLK		
0008 205Fh	DMAC1	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 2080h	DMAC2	DMA source address register	DMSAR	32	32	2 ICLK		
0008 2084h	DMAC2	DMA destination address register	DMDAR	32	32	2 ICLK		
0008 2088h	DMAC2	DMA transfer count register	DMCRA	32	32	2 ICLK		
0008 208Ch	DMAC2	DMA block transfer count register	DMCRB	16	16	2 ICLK		
0008 2090h	DMAC2	DMA transfer mode register	DMTMD	16	16	2 ICLK		
0008 2093h	DMAC2	DMA interrupt setting register	DMINT	8	8	2 ICLK		
0008 2094h	DMAC2	DMA address mode register	DMAMD	16	16	2 ICLK		
0008 209Ch	DMAC2	DMA transfer enable register	DMCNT	8	8	2 ICLK		
0008 209Dh	DMAC2	DMA software start register	DMREQ	8	8	2 ICLK		
0008 209Eh	DMAC2	DMA status register	DMSTS	8	8	2 ICLK		
0008 209Fh	DMAC2	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 20C0h	DMAC3	DMA source address register	DMSAR	32	32	2 ICLK		
0008 20C4h	DMAC3	DMA destination address register	DMDAR	32	32	2 ICLK		
0008 20C8h	DMAC3	DMA transfer count register	DMCRA	32	32	2 ICLK		
0008 20CCh	DMAC3	DMA block transfer count register	DMCRB	16	16	2 ICLK		
0008 20D0h	DMAC3	DMA transfer mode register	DMTMD	16	16	2 ICLK		
0008 20D3h	DMAC3	DMA interrupt setting register	DMINT	8	8	2 ICLK		
0008 20D4h	DMAC3	DMA address mode register	DMAMD	16	16	2 ICLK		
0008 20DCh	DMAC3	DMA transfer enable register	DMCNT	8	8	2 ICLK		
0008 20DDh	DMAC3	DMA software start register	DMREQ	8	8	2 ICLK		
0008 20DEh	DMAC3	DMA status register	DMSTS	8	8	2 ICLK		
0008 20DFh	DMAC3	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 2200h	DMAC	DMA module activation register	DMAST	8	8	2 ICLK		
0008 2400h	DTC	DTC control register	DTCCR	8	8	2 ICLK		
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32	2 ICLK		
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8	2 ICLK		
0008 240Ch	DTC	DTC module start register	DTCST	8	8	2 ICLK		
0008 240Eh	DTC	DTC status register	DTCSTS	16	16	2 ICLK		
0008 3002h	BSC	CS0 mode register	CS0MOD	16	16	1, 2 BCLK		
0008 3004h	BSC	CS0 wait control register 1	CS0WCR1	32	32	1, 2 BCLK		
0008 3008h	BSC	CS0 wait control register 2	CS0WCR2	32	32	1, 2 BCLK		
0008 3012h	BSC	CS1 mode register	CS1MOD	16	16	1, 2 BCLK		
0008 3014h	BSC	CS1 wait control register 1	CS1WCR1	32	32	1, 2 BCLK		

Table 4.1 List of I/O Registers (Address Order) (3/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 3018h	BSC	CS1 wait control register 2	CS1WCR2	32	32	1, 2 BCLK		Buses
0008 3022h	BSC	CS2 mode register	CS2MOD	16	16	1, 2 BCLK		
0008 3024h	BSC	CS2 wait control register 1	CS2WCR1	32	32	1, 2 BCLK		
0008 3028h	BSC	CS2 wait control register 2	CS2WCR2	32	32	1, 2 BCLK		
0008 3032h	BSC	CS3 mode register	CS3MOD	16	16	1, 2 BCLK		
0008 3034h	BSC	CS3 wait control register 1	CS3WCR1	32	32	1, 2 BCLK		
0008 3038h	BSC	CS3 wait control register 2	CS3WCR2	32	32	1, 2 BCLK		
0008 3042h	BSC	CS4 mode register	CS4MOD	16	16	1, 2 BCLK		
0008 3044h	BSC	CS4 wait control register 1	CS4WCR1	32	32	1, 2 BCLK		
0008 3048h	BSC	CS4 wait control register 2	CS4WCR2	32	32	1, 2 BCLK		
0008 3052h	BSC	CS5 mode register	CS5MOD	16	16	1, 2 BCLK		
0008 3054h	BSC	CS5 wait control register 1	CS5WCR1	32	32	1, 2 BCLK		
0008 3058h	BSC	CS5 wait control register 2	CS5WCR2	32	32	1, 2 BCLK		
0008 3062h	BSC	CS6 mode register	CS6MOD	16	16	1, 2 BCLK		
0008 3064h	BSC	CS6 wait control register 1	CS6WCR1	32	32	1, 2 BCLK		
0008 3068h	BSC	CS6 wait control register 2	CS6WCR2	32	32	1, 2 BCLK		
0008 3072h	BSC	CS7 mode register	CS7MOD	16	16	1, 2 BCLK		
0008 3074h	BSC	CS7 wait control register 1	CS7WCR1	32	32	1, 2 BCLK		
0008 3078h	BSC	CS7 wait control register 2	CS7WCR2	32	32	1, 2 BCLK		
0008 3802h	BSC	CS0 control register	CS0CR	16	16	1, 2 BCLK		
0008 380Ah	BSC	CS0 recovery cycle register	CS0REC	16	16	1, 2 BCLK		
0008 3812h	BSC	CS1 control register	CS1CR	16	16	1, 2 BCLK		
0008 381Ah	BSC	CS1 recovery cycle register	CS1REC	16	16	1, 2 BCLK		
0008 3822h	BSC	CS2 control register	CS2CR	16	16	1, 2 BCLK		
0008 382Ah	BSC	CS2 recovery cycle register	CS2REC	16	16	1, 2 BCLK		
0008 3832h	BSC	CS3 control register	CS3CR	16	16	1, 2 BCLK		
0008 383Ah	BSC	CS3 recovery cycle register	CS3REC	16	16	1, 2 BCLK		
0008 3842h	BSC	CS4 control register	CS4CR	16	16	1, 2 BCLK		
0008 384Ah	BSC	CS4 recovery cycle register	CS4REC	16	16	1, 2 BCLK		
0008 3852h	BSC	CS5 control register	CS5CR	16	16	1, 2 BCLK		
0008 385Ah	BSC	CS5 recovery cycle register	CS5REC	16	16	1, 2 BCLK		
0008 3862h	BSC	CS6 control register	CS6CR	16	16	1, 2 BCLK		
0008 386Ah	BSC	CS6 recovery cycle register	CS6REC	16	16	1, 2 BCLK		
0008 3872h	BSC	CS7 control register	CS7CR	16	16	1, 2 BCLK		
0008 387Ah	BSC	CS7 recovery cycle register	CS7REC	16	16	1, 2 BCLK		
0008 3880h	BSC	CS recovery cycle insertion enable register	CSRECEN	16	16	1, 2 BCLK		
0008 6400h	MPU	Region-0 start page number register	RSPAGE0	32	32	1ICLK		MPU
0008 6404h	MPU	Region-0 end page number register	REPAGE0	32	32	1ICLK		
0008 6408h	MPU	Region-1 start page number register	RSPAGE1	32	32	1ICLK		
0008 640Ch	MPU	Region-1 end page number register	REPAGE1	32	32	1ICLK		
0008 6410h	MPU	Region-2 start page number register	RSPAGE2	32	32	1ICLK		
0008 6414h	MPU	Region-2 end page number register	REPAGE2	32	32	1ICLK		
0008 6418h	MPU	Region-3 start page number register	RSPAGE3	32	32	1ICLK		
0008 641Ch	MPU	Region-3 end page number register	REPAGE3	32	32	1ICLK		
0008 6420h	MPU	Region-4 start page number register	RSPAGE4	32	32	1ICLK		
0008 6424h	MPU	Region-4 end page number register	REPAGE4	32	32	1ICLK		
0008 6428h	MPU	Region-5 start page number register	RSPAGE5	32	32	1ICLK		
0008 642Ch	MPU	Region-5 end page number register	REPAGE5	32	32	1ICLK		
0008 6430h	MPU	Region-6 start page number register	RSPAGE6	32	32	1ICLK		
0008 6434h	MPU	Region-6 end page number register	REPAGE6	32	32	1ICLK		

Table 4.1 List of I/O Registers (Address Order) (14/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8101h	TPUA	Timer synchronous register	TSYR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8108h	TPU0	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8109h	TPU1	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 810Ah	TPU2	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 810Bh	TPU3	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 810Ch	TPU4	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 810Dh	TPU5	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8110h	TPU0	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8111h	TPU0	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8112h	TPU0	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8113h	TPU0	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8114h	TPU0	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8115h	TPU0	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8116h	TPU0	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8118h	TPU0	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 811Ah	TPU0	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 811Ch	TPU0	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 811Eh	TPU0	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 8120h	TPU1	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8121h	TPU1	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8122h	TPU1	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 8124h	TPU1	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8125h	TPU1	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8126h	TPU1	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8128h	TPU1	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 812Ah	TPU1	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8130h	TPU2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8131h	TPU2	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8132h	TPU2	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 8134h	TPU2	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8135h	TPU2	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8136h	TPU2	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8138h	TPU2	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 813Ah	TPU2	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8140h	TPU3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8141h	TPU3	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8142h	TPU3	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8143h	TPU3	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8144h	TPU3	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8145h	TPU3	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8146h	TPU3	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8148h	TPU3	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 814Ah	TPU3	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 814Ch	TPU3	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 814Eh	TPU3	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 8150h	TPU4	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8151h	TPU4	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8152h	TPU4	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 8154h	TPU4	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8155h	TPU4	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (15/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8156h	TPU4	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8158h	TPU4	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 815Ah	TPU4	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8160h	TPU5	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8161h	TPU5	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8162h	TPU5	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 8164h	TPU5	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8165h	TPU5	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8166h	TPU5	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8168h	TPU5	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 816Ah	TPU5	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8170h	TPUB	Timer start register	TSTR	8	8	2, 3 PCLKB	2 ICLK	
0008 8171h	TPUB	Timer synchronous register	TSYR	8	8	2, 3 PCLKB	2 ICLK	
0008 8178h	TPU6	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8179h	TPU7	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 817Ah	TPU8	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 817Bh	TPU9	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 817Ch	TPU10	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 817Dh	TPU11	Noise filter control register	NFCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8180h	TPU6	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8181h	TPU6	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8182h	TPU6	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8183h	TPU6	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8184h	TPU6	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8185h	TPU6	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8186h	TPU6	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8188h	TPU6	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 818Ah	TPU6	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 818Ch	TPU6	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 818Eh	TPU6	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 8190h	TPU7	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8191h	TPU7	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8192h	TPU7	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 8194h	TPU7	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8195h	TPU7	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8196h	TPU7	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8198h	TPU7	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 819Ah	TPU7	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81A0h	TPU8	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81A1h	TPU8	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81A2h	TPU8	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 81A4h	TPU8	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81A5h	TPU8	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81A6h	TPU8	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81A8h	TPU8	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81AAh	TPU8	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81B0h	TPU9	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B1h	TPU9	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B2h	TPU9	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 81B3h	TPU9	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (16/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 81B4h	TPU9	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 81B5h	TPU9	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B6h	TPU9	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81B8h	TPU9	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81BAh	TPU9	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81BCh	TPU9	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 81BEh	TPU9	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 81C0h	TPU10	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C1h	TPU10	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C2h	TPU10	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C4h	TPU10	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81C5h	TPU10	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C6h	TPU10	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81C8h	TPU10	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81CAh	TPU10	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81D0h	TPU11	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D1h	TPU11	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D2h	TPU11	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D4h	TPU11	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81D5h	TPU11	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D6h	TPU11	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	PPG
0008 81D8h	TPU11	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81DAh	TPU11	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81E6h	PPG0	PPG output control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81E7h	PPG0	PPG output mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 81E8h	PPG0	Next data enable register H	NDERH	8	8	2, 3 PCLKB	2 ICLK	
0008 81E9h	PPG0	Next data enable register L	NDERL	8	8	2, 3 PCLKB	2 ICLK	
0008 81EAh	PPG0	Output data register H	PODRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81EBh	PPG0	Output data register L	PODRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81ECh*1	PPG0	Next data register H	NDRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81EDh*2	PPG0	Next data register L	NDRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81EEh*1	PPG0	Next data register H	NDRH2	8	8	2, 3 PCLKB	2 ICLK	
0008 81EFh*2	PPG0	Next data register L	NDRL2	8	8	2, 3 PCLKB	2 ICLK	
0008 81F0h	PPG1	PPG trigger select register	PTRSLR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F6h	PPG1	PPG output control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F7h	PPG1	PPG output mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F8h	PPG1	Next data enable register H	NDERH	8	8	2, 3 PCLKB	2 ICLK	
0008 81F9h	PPG1	Next data enable register L	NDERL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FAh	PPG1	Output data register H	PODRH	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 81FBh	PPG1	Output data register L	PODRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FCh*3	PPG1	Next data register H	NDRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81FDh*4	PPG1	Next data register L	NDRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FEh*3	PPG1	Next data register H	NDRH2	8	8	2, 3 PCLKB	2 ICLK	
0008 81FFh*4	PPG1	Next data register L	NDRL2	8	8	2, 3 PCLKB	2 ICLK	
0008 8200h	TMR0	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8201h	TMR1	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8202h	TMR0	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8203h	TMR1	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8204h	TMR0	Time constant register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	
0008 8205h	TMR1	Time constant register A	TCORA	8	8*5	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (20/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 83C3h	RSPI2	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK	RSPI
0008 83C4h	RSPI2	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK	
0008 83C8h	RSPI2	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83C9h	RSPI2	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83CAh	RSPI2	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK	
0008 83CBh	RSPI2	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83CCh	RSPI2	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK	
0008 83CDh	RSPI2	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK	
0008 83CEh	RSPI2	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK	
0008 83CFh	RSPI2	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 83D0h	RSPI2	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK	
0008 83D2h	RSPI2	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	
0008 83D4h	RSPI2	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK	
0008 83D6h	RSPI2	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK	
0008 83D8h	RSPI2	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK	
0008 83DAh	RSPI2	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK	
0008 83DCh	RSPI2	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK	
0008 83DEh	RSPI2	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK	
0008 8600h	MTU3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	MTU2a
0008 8601h	MTU4	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8602h	MTU3	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8603h	MTU4	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8604h	MTU3	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8605h	MTU3	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8606h	MTU4	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8607h	MTU4	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8608h	MTU3	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8609h	MTU4	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 860Ah	MTU	Timer output master enable register	TOER	8	8	2, 3 PCLKB	2 ICLK	
0008 860Dh	MTU	Timer gate control register	TGCR	8	8	2, 3 PCLKB	2 ICLK	
0008 860Eh	MTU	Timer output control register 1	TOCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 860Fh	MTU	Timer output control register 2	TOCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8610h	MTU3	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8612h	MTU4	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8614h	MTU	Timer cycle data register	TCDR	16	16	2, 3 PCLKB	2 ICLK	
0008 8616h	MTU	Timer dead time data register	TDDR	16	16	2, 3 PCLKB	2 ICLK	
0008 8618h	MTU3	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 861Ah	MTU3	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 861Ch	MTU4	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 861Eh	MTU4	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8620h	MTU	Timer subcounter	TCNTS	16	16	2, 3 PCLKB	2 ICLK	
0008 8622h	MTU	Timer cycle buffer register	TCBR	16	16	2, 3 PCLKB	2 ICLK	
0008 8624h	MTU3	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 8626h	MTU3	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 8628h	MTU4	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 862Ah	MTU4	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 862Ch	MTU3	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 862Dh	MTU4	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8630h	MTU	Timer interrupt skipping set register	TITCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8631h	MTU	Timer interrupt skipping counter	TITCNT	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (32/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C164h	MPC	P44 pin function control register	P44PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C165h	MPC	P45 pin function control register	P45PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C166h	MPC	P46 pin function control register	P46PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C167h	MPC	P47 pin function control register	P47PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C168h	MPC	P50 pin function control register	P50PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C169h	MPC	P51 pin function control register	P51PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C16Ah	MPC	P52 pin function control register	P52PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C16Ch	MPC	P54 pin function control register	P54PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C16Dh	MPC	P55 pin function control register	P55PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C16Eh	MPC	P56 pin function control register	P56PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C170h	MPC	P60 pin function control register	P60PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C171h	MPC	P61 pin function control register	P61PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C176h	MPC	P66 pin function control register	P66PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C177h	MPC	P67 pin function control register	P67PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C178h	MPC	P70 pin function control register	P70PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C17Bh	MPC	P73 pin function control register	P73PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C17Ch	MPC	P74 pin function control register	P74PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C17Dh	MPC	P75 pin function control register	P75PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C17Eh	MPC	P76 pin function control register	P76PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C17Fh	MPC	P77 pin function control register	P77PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C180h	MPC	P80 pin function control register	P80PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C181h	MPC	P81 pin function control register	P81PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C182h	MPC	P82 pin function control register	P82PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C183h	MPC	P83 pin function control register	P83PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C186h	MPC	P86 pin function control register	P86PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C187h	MPC	P87 pin function control register	P87PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C188h	MPC	P90 pin function control register	P90PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C189h	MPC	P91 pin function control register	P91PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C18Ah	MPC	P92 pin function control register	P92PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C18Bh	MPC	P93 pin function control register	P93PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C190h	MPC	PA0 pin function control register	PA0PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C191h	MPC	PA1 pin function control register	PA1PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C192h	MPC	PA2 pin function control register	PA2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C193h	MPC	PA3 pin function control register	PA3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C194h	MPC	PA4 pin function control register	PA4PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C195h	MPC	PA5 pin function control register	PA5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C196h	MPC	PA6 pin function control register	PA6PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C197h	MPC	PA7 pin function control register	PA7PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C198h	MPC	PB0 pin function control register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C199h	MPC	PB1 pin function control register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C19Ah	MPC	PB2 pin function control register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C19Bh	MPC	PB3 pin function control register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C19Ch	MPC	PB4 pin function control register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C19Dh	MPC	PB5 pin function control register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C19Eh	MPC	PB6 pin function control register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C19Fh	MPC	PB7 pin function control register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A0h	MPC	PC0 pin function control register	PC0PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A1h	MPC	PC1 pin function control register	PC1PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A2h	MPC	PC2 pin function control register	PC2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1A3h	MPC	PC3 pin function control register	PC3PFS	8	8	2, 3 PCLKB	2 ICLK	

Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, T_a = T_{opr}

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions		
Supply current*1	High-speed operating mode	Max.*2		I _{CC} *3	—	—	100	mA	ICLK = 100 MHz PCLKB = 50 MHz FCLK = 50 MHz BCLK = 50 MHz		
		Normal	Peripheral function: clock signal supplied*4		—	52	—				
			Peripheral function: clock signal stopped*4		—	40	—				
		Sleep mode			—	25	60				
		All-module-clock-stop mode (reference value)			—	20	30				
		Increased by BGO operation*5			—	15	—				
	Low-speed operating mode 1*6				—	4	—				ICLK = 1 MHz
	Low-speed operating mode 2				—	1	—				ICLK = 32.768 kHz
	Software standby mode				—	0.2	6				
	Deep software standby mode	Power supplied to RAM and USB resume detecting unit			—	22	200	μA			
		Power not supplied to RAM and USB resume detecting unit	Power-on reset circuit and low-power function enabled consumption function disabled		—	21	60				
			Power-on reset circuit and low-power function enabled consumption function enabled		—	6.2	28				
	Increased by RTC operation				—	3	—				
	RTC operation when VCC is off				—	1.7	—		V _{BATT} = 2.3 V		
					—	3.3	—	V _{BATT} = 3.3 V			
Analog power supply current*7	During 12-bit A/D conversion (including temperature sensor)			I _{AVCC0}	—	2.3	3.2	mA			
	During 10-bit A/D conversion			I _{VREFH} *7	—	1.0	1.65				
	During D/A conversion (per unit)				—	0.7	1.0				
	Waiting for A/D, D/A conversion (all units)*8			—	—	25	35		μA		
	A/D, D/A converter in standby mode (all units)*8				—	0.1	4.0		μA		
Reference power supply current	During 12-bit A/D conversion			I _{VREFH0}	—	0.6	0.7	mA			
	Waiting for 12-bit A/D conversion (per unit)				—	0.5	0.6				
	12-bit A/D converter in standby mode (per unit)				—	0.1	2.0		μA		
RAM standby voltage				V _{RAM}	2.7	—	—	V			
VCC rising gradient				SrVCC	8.4	—	20000	μs/V			
VCC falling gradient*8				SfVCC	8.4	—	—	μs/V			

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.

Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK:PCLK:BCLK:BCLK pin = 8:4:4:2)

I_{CC} Max. = 0.87 × f + 13 (max. operation in high-speed operating mode)

I_{CC} Typ. = 0.35 × f + 5 (normal operation in high-speed operating mode)

I_{CC} Typ. = 1.0 × f + 3 (low-speed operating mode 1)

I_{CC} Max. = 0.48 × f + 12 (sleep mode)

Note 4. This does not include the BGO operation.

Note 5. This is the increase for programming or erasure of the ROM or flash memory for data storage during program execution.

Note 6. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

Note 7. The current values for 10-bit A/D converter and 10-bit D/A converter are included in the current from the VREFH pin.

Note 8. The values are the sum of I_{AVCC0} and I_{VREFH}.

Table 5.5 DC Characteristics (4) (for G Version (+85 < Ta ≤ +105°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, T_a = T_{opr}

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Supply current*1	High-speed operating mode	Max.*2		I _{CC} *3	—	—	115	mA	ICLK = 100 MHz PCLKB = 50 MHz FCLK = 50 MHz BCLK = 50 MHz	
		Normal	Peripheral function: clock signal supplied*4		—	52	—			
			Peripheral function: clock signal stopped*4		—	40	—			
		Sleep mode			—	25	75			
		All-module-clock-stop mode (reference value)			—	20	45			
		Increased by BGO operation*5			—	15	—			
	Low-speed operating mode 1*6				—	4	—			ICLK = 1 MHz ICLK = 32.768 kHz
	Low-speed operating mode 2				—	1	—			
	Software standby mode				—	0.2	6			
	Deep software standby mode	Power supplied to RAM and USB resume detecting unit			—	22	200	μA		
		Power not supplied to RAM and USB resume detecting unit	Power-on reset circuit and low-power function enabled consumption function disabled		—	21	60			
			Power-on reset circuit and low-power function enabled consumption function enabled		—	6.2	28			
		Increased by RTC operation			—	3	—			
	RTC operation when VCC is off				—	1.7	—	V _{BATT} = 2.3 V		
					—	3.3	—	V _{BATT} = 3.3 V		
Analog power supply current*7	During 12-bit A/D conversion (including temperature sensor)			I _{AVCC0}	—	2.3	3.2	mA		
	During 10-bit A/D conversion			I _{VREFH} *7	—	1.0	1.65			
	During D/A conversion (per unit)				—	0.7	1.0			
	Waiting for A/D, D/A conversion (all units)*8			—	—	25	35		μA	
	A/D, D/A converter in standby mode (all units)*8				—	0.1	5		μA	
Reference power supply current	During 12-bit A/D conversion			I _{VREFH0}	—	0.6	0.7	mA		
	Waiting for 12-bit A/D conversion (per unit)				—	0.5	0.6			
	12-bit A/D converter in standby mode (per unit)				—	0.1	2.0		μA	
RAM standby voltage				V _{RAM}	2.7	—	—	V		
VCC rising gradient				SrVCC	8.4	—	20000	μs/V		
VCC falling gradient*8				SfVCC	8.4	—	—	μs/V		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.

Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK:PCLK:BCLK:BCLK pin = 8:4:4:2)

I_{CC} Max. = 0.87 × f + 13 (max. operation in high-speed operating mode)

I_{CC} Typ. = 0.35 × f + 5 (normal operation in high-speed operating mode)

I_{CC} Typ. = 1.0 × f + 3 (low-speed operating mode 1)

I_{CC} Max. = 0.48 × f + 12 (sleep mode)

Note 4. This does not include the BGO operation.

Note 5. This is the increase for programming or erasure of the ROM or flash memory for data storage during program execution.

Note 6. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

Note 7. The current values for 10-bit A/D converter and 10-bit D/A converter are included in the current from the VREFH pin.

Note 8. The values are the sum of I_{AVCC0} and I_{VREFH}.

Table 5.19 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0

VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

PCLK = 8 to 50 MHz

 $T_a = T_{opr}$

High drive output is selected by the drive capacity control register.

Item		Symb ol	Min.*1,*2	Max.	Unit	Test Conditions
RIIC (Standard-mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 1300$	—	ns	Figure 5.37
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 600$	—	ns	
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc} : RIIC internal reference clock (IIC ϕ) Cycle

Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 2. C_b is the total capacitance of the bus lines.

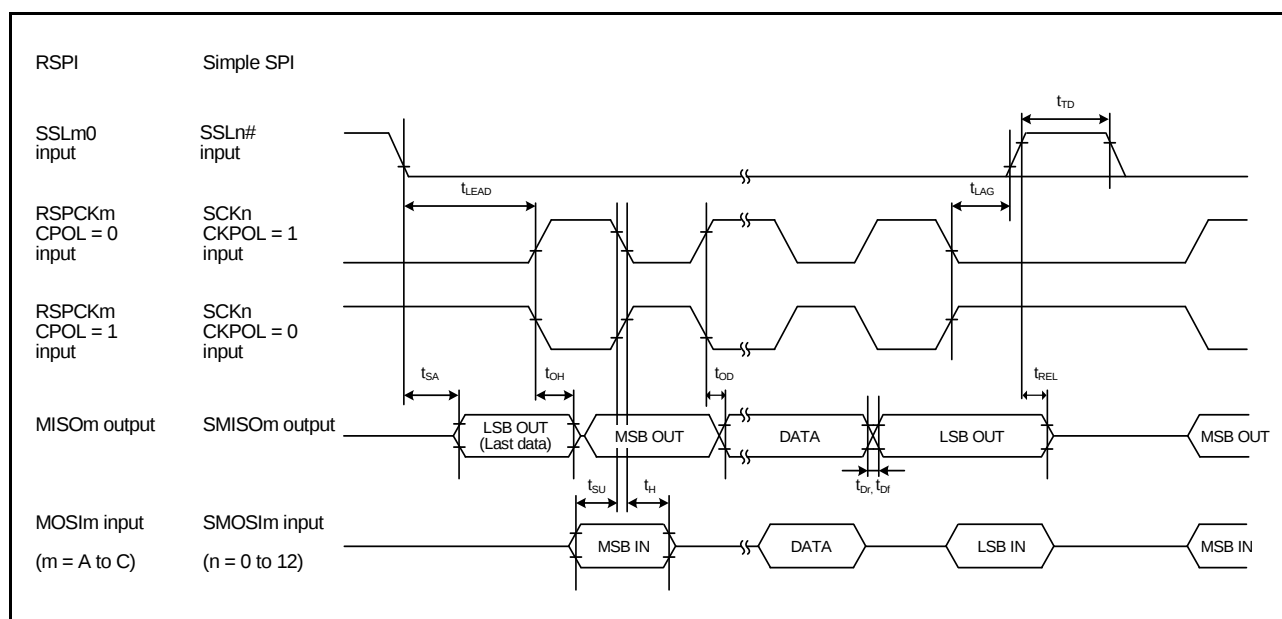


Figure 5.36 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

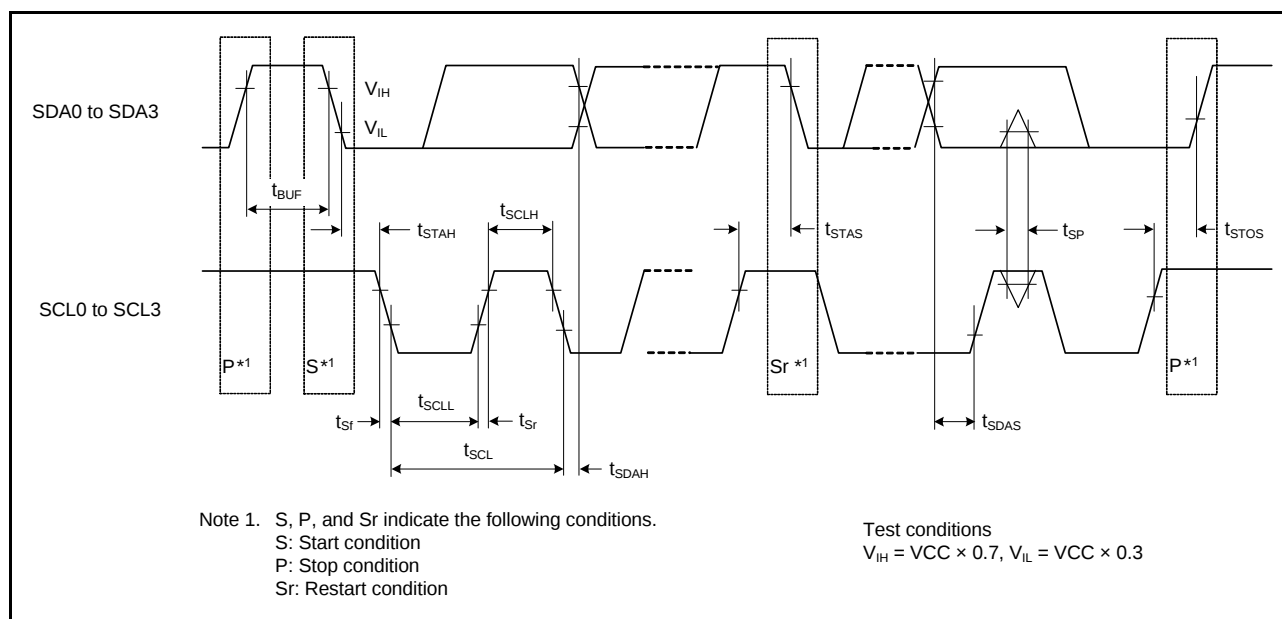


Figure 5.37 IIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

REVISION HISTORY	RX630 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.50	May 13, 2011	—	First Edition issued
1.00	Sep 13, 2011	All	1. Overview 2, 4, 6 Table 1.1 Outline of Specifications: Reset, real time clock, package, changed 8 to 9 Table 1.3 List of Products Table, changed 12 Table 1.4 List of Pin Functions: BSCANP pin, added 17 Figure 1.3 Pin Assignments (177-Pin TFLGA), added 18 Figure 1.4 Pin Assignments (176-Pin LFBGA), added 19 Figure 1.5 Pin Assignments (176-Pin LQFP): 16-pin and 18-pin, changed 20 Figure 1.6 Pin Assignments (145-Pin TFLGA), added 21 Figure 1.7 Pin Assignments (144-Pin LQFP): 16-pin, changed 22 Figure 1.8 Pin Assignments (100-Pin TFLGA), added 23 Figure 1.9 Pin Assignments (100-Pin LQFP): 7-pin, changed 25 to 32 Table 1.5 List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA), added 41 to 47 Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA), added 55 to 59 Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA), added 4. I/O Registers 75 (1) I/O Register Addresses (Address Order), changed 76 (3) Number of I/O Registers to Access Cycles, changed 77 to 116 Table 5.1 List of I/O Registers, changed 5. Electrical Characteristics 117 to 156 Added Appendix 1. Port States in Each Processing Mode 157 Figure A. 177-Pin TFLGA (PTLG0177KA-A), added 158 Figure B. 176-Pin LFBGA (PLBG0176GA-A), added 160 Figure D. 145-Pin TFLGA (PTLG0145KA-A), added 162 Figure F. 100-Pin TFLGA (PTLG0100KA-A), added