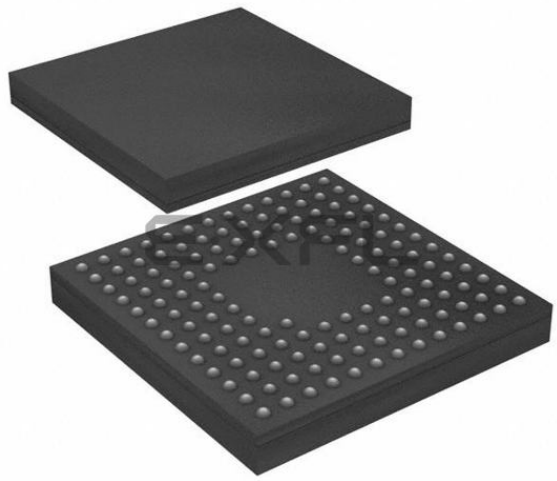
Renesas Electronics America Inc - R5F5630EDDLK#U0 Datasheet



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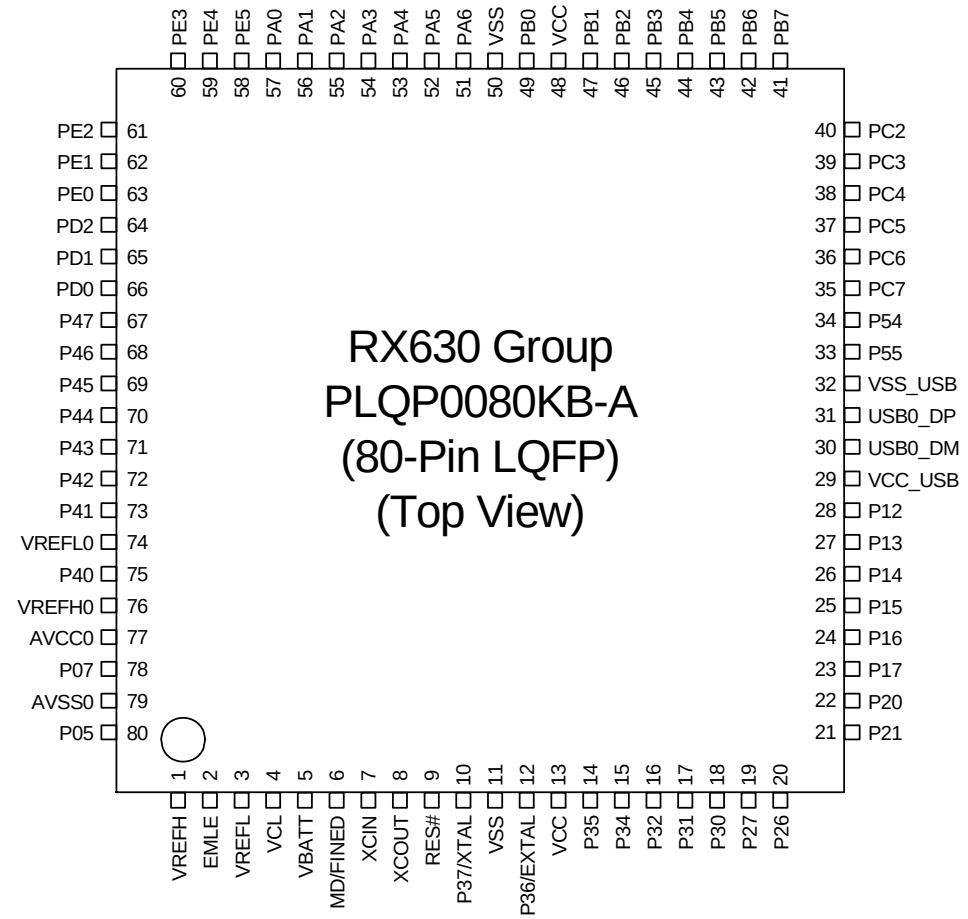
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	117
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	145-TFLGA
Supplier Device Package	145-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5630eddlk-u0

Table 1.1 Outline of Specifications (3/5)

Classification	Module/Function	Description
Timers	16-bit timer pulse unit (TPUa)	• (16 bits × 6 channels) × 2 units • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Supports the input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Support for buffered operation, phase-counting mode (two phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel. • PPG output trigger can be generated • Capable of generating conversion start triggers for the A/D converters • Signals from the input capture pins are input via a digital filter • Clock frequency measuring method
	Multi-function timer pulse unit 2 (MTU2a)	• (16 bits × 6 channels) × 1 unit • Time bases for the 6 16-bit timer channels can be provided via up to 16 pulse-input/output lines and three pulse-input lines • Select from among eight counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Generation of triggers for A/D converter conversion • Digital filter • Signals from the input capture pins are input via a digital filter • PPG output trigger can be generated • Clock frequency measuring function
	Frequency measurement function (MCK)	The MTU or unit 0 TPU module can be used to monitor the main clock, sub-clock, HOCO clock, LOCO clock, and PLL clock for abnormal frequencies.
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	Programmable pulse generator (PPG)	• (4 bits × 4 groups) × 2 units • Pulse output with the MTU or TPU output as a trigger • Maximum of 32 pulse-output possible
	8-bit timers (TMR)	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Generation of triggers for A/D converter conversion • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Realtime clock (RTCa)	• Clock sources: Main clock, sub-clock • Clock and calendar functions Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Battery backup operation • Time-capture facility for three values
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)
	Independent watchdog timer (IWDTA)	• 14 bits × 1 channel • Counter-input clock: Dedicated on-chip oscillator for the IWDT • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.11, List of Pins and Pin Functions (80-Pin LQFP).

Figure 1.10 Pin Assignment (80-Pin LQFP)

Table 1.5 List of Pins and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
M3		P24	CS4#	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3		
M4		P86		TIOCA0			
M5		P13		MTIOC0B/TIOCA5/TMO3/ PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
M6		P56	WR2#/BC2#	MTIOC3C/TIOCA1			
M7		P54	ALE	MTIOC4B/TMCI1	CTS2#/RTS2#/S2#/CTX1		
M8	BCLK	P53*3					
M9		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
M10		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/ PO29	SCK8/RSPCKA		
M11		P81		MTIOC3D/PO27	RXD10/SMISO10/SSCL10		
M12		P77	CS7#	PO23	TXD11/SMOSI11/SSDA11		
M13		PB7	A15	MTIOC3B/TIOCB5/PO31	TXD9/SMOSI9/SSDA9		
M14		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	SCK9		
M15		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/SS9#		
N1		PH5					
N2		P23		MTIOC3D/MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3		
N3		P22		MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0		
N4		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS	IRQ5	
N5		P12		MTIC5U/TMCI1	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
N6		P57	WAIT#/WR3#/ BC3#				
N7		P55	WAIT#	MTIOC4D/TMO3	CRX1/	IRQ10	
N8		PL2					
N9		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
N10		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA	IRQ14	
N11		P82		MTIOC4A/PO28	TXD10/SMOSI10/SSDA10		
N12		PC3	A19	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ IETXD		
N13		PC0	A16	MTIOC3C/TCLKC/PO17	CTS5#/RTS5#/SS5#/ SSLA1/SCL3	IRQ14	
N14		P73	CS3#	PO16			
N15		PL0					
P1		PH4					
P2		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/ IETXD	IRQ7	ADTRG#
P3		P87		TIOCA2			
P4		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE	IRQ4	
P5		P10		MTIC5W/TMRI3		IRQ0	
P6	VCC_USB						

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (1/3)

Pin Number 100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD, AD, DA
A1		P05				IRQ13	DA1
A2	VREFH						
A3		P07				IRQ15	ADTRG0#
A4	VREFL0						
A5		P43				IRQ11-DS	AN003
A6		PD0	D0[A0/D0]			IRQ0	AN008
A7		PD4	D4[A4/D4]	POE3#		IRQ4	AN012
A8		PE0	D8[A8/D8]		SCK12/SSLB1		ANEX0
A9		PE1	D9[A9/D9]	MTIOC4C/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/RSPCKB		ANEX1
A10		PE2	D10[A10/D10]	MTIOC4A/PO23	RXD12/SMISO12/ SSCL12/RXDX12/SSLB3/ MOSIB	IRQ7-DS	AN0
B1	EMLE						
B2	AVSS0						
B3	AVCC0						
B4		P40				IRQ8-DS	AN000
B5		P44				IRQ12-DS	AN004
B6		PD1	D1[A1/D1]	MTIOC4B	CTX0*1	IRQ1	AN009
B7		PD3	D3[A3/D3]	POE8#		IRQ3	AN011
B8		PD6	D6[A6/D6]	MTIC5V/POE1#		IRQ6	AN6
B9		PD7	D7[A7/D7]	MTIC5U/POE0#		IRQ7	AN7
B10		PE3	D11[A11/D11]	MTIOC4B/PO26/POE8#	CTS12#/RTS12#/SS12#/ MISOB		AN1
C1	VCL						
C2	VREFL						
C3		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
C4	VREFH0						
C5		P42				IRQ10-DS	AN002
C6		P47				IRQ15-DS	AN007
C7		PD2	D2[A2/D2]	MTIOC4D	CRX0*1	IRQ2	AN010
C8		PD5	D5[A5/D5]	MTIC5W/POE2#		IRQ5	AN013
C9		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B	RSPCKB	IRQ5	AN3
C10		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ PO28	SSLB0		AN2
D1	XCIN						
D2	XCOUT						
D3	MD/FINED						
D4	VBATT						
D5		P45				IRQ13-DS	AN005
D6		P46				IRQ14-DS	AN006
D7		PE6	D14[A14/D14]		MOSIB	IRQ6	AN4
D8		PE7	D15[A15/D15]		MISOB	IRQ7	AN5
D9		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2	IRQ11	
D10		PA0	A0/BC0#	MTIOC4A/TIOCA0/PO16	SSLA1		
E1	XTAL	P37					
E2	VSS						
E3	RES#						

Table 4.1 List of I/O Registers (Address Order) (6/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7093h	ICU	Interrupt request register 147	IR147	8	8	2 ICLK		ICUb
0008 7094h	ICU	Interrupt request register 148	IR148	8	8	2 ICLK		
0008 7095h	ICU	Interrupt request register 149	IR149	8	8	2 ICLK		
0008 7096h	ICU	Interrupt request register 150	IR150	8	8	2 ICLK		
0008 7097h	ICU	Interrupt request register 151	IR151	8	8	2 ICLK		
0008 7098h	ICU	Interrupt request register 152	IR152	8	8	2 ICLK		
0008 7099h	ICU	Interrupt request register 153	IR153	8	8	2 ICLK		
0008 709Ah	ICU	Interrupt request register 154	IR154	8	8	2 ICLK		
0008 709Bh	ICU	Interrupt request register 155	IR155	8	8	2 ICLK		
0008 709Ch	ICU	Interrupt request register 156	IR156	8	8	2 ICLK		
0008 709Dh	ICU	Interrupt request register 157	IR157	8	8	2 ICLK		
0008 709Eh	ICU	Interrupt request register 158	IR158	8	8	2 ICLK		
0008 709Fh	ICU	Interrupt request register 159	IR159	8	8	2 ICLK		
0008 70A0h	ICU	Interrupt request register 160	IR160	8	8	2 ICLK		
0008 70A1h	ICU	Interrupt request register 161	IR161	8	8	2 ICLK		
0008 70A2h	ICU	Interrupt request register 162	IR162	8	8	2 ICLK		
0008 70A3h	ICU	Interrupt request register 163	IR163	8	8	2 ICLK		
0008 70A4h	ICU	Interrupt request register 164	IR164	8	8	2 ICLK		
0008 70A5h	ICU	Interrupt request register 165	IR165	8	8	2 ICLK		
0008 70A6h	ICU	Interrupt request register 166	IR166	8	8	2 ICLK		
0008 70A7h	ICU	Interrupt request register 167	IR167	8	8	2 ICLK		
0008 70AAh	ICU	Interrupt request register 170	IR170	8	8	2 ICLK		
0008 70ABh	ICU	Interrupt request register 171	IR171	8	8	2 ICLK		
0008 70ACh	ICU	Interrupt request register 172	IR172	8	8	2 ICLK		
0008 70ADh	ICU	Interrupt request register 173	IR173	8	8	2 ICLK		
0008 70AEh	ICU	Interrupt request register 174	IR174	8	8	2 ICLK		
0008 70AFh	ICU	Interrupt request register 175	IR175	8	8	2 ICLK		
0008 70B0h	ICU	Interrupt request register 176	IR176	8	8	2 ICLK		
0008 70B1h	ICU	Interrupt request register 177	IR177	8	8	2 ICLK		
0008 70B2h	ICU	Interrupt request register 178	IR178	8	8	2 ICLK		
0008 70B3h	ICU	Interrupt request register 179	IR179	8	8	2 ICLK		
0008 70B4h	ICU	Interrupt request register 180	IR180	8	8	2 ICLK		
0008 70B5h	ICU	Interrupt request register 181	IR181	8	8	2 ICLK		
0008 70B6h	ICU	Interrupt request register 182	IR182	8	8	2 ICLK		
0008 70B7h	ICU	Interrupt request register 183	IR183	8	8	2 ICLK		
0008 70B8h	ICU	Interrupt request register 184	IR184	8	8	2 ICLK		
0008 70B9h	ICU	Interrupt request register 185	IR185	8	8	2 ICLK		
0008 70BAh	ICU	Interrupt request register 186	IR186	8	8	2 ICLK		
0008 70BBh	ICU	Interrupt request register 187	IR187	8	8	2 ICLK		
0008 70BCh	ICU	Interrupt request register 188	IR188	8	8	2 ICLK		
0008 70BDh	ICU	Interrupt request register 189	IR189	8	8	2 ICLK		
0008 70BEh	ICU	Interrupt request register 190	IR190	8	8	2 ICLK		
0008 70BFh	ICU	Interrupt request register 191	IR191	8	8	2 ICLK		
0008 70C0h	ICU	Interrupt request register 192	IR192	8	8	2 ICLK		
0008 70C1h	ICU	Interrupt request register 193	IR193	8	8	2 ICLK		
0008 70C2h	ICU	Interrupt request register 194	IR194	8	8	2 ICLK		
0008 70C3h	ICU	Interrupt request register 195	IR195	8	8	2 ICLK		
0008 70C4h	ICU	Interrupt request register 196	IR196	8	8	2 ICLK		
0008 70C5h	ICU	Interrupt request register 197	IR197	8	8	2 ICLK		
0008 70C6h	ICU	Interrupt request register 198	IR198	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (17/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8206h	TMR0	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8207h	TMR1	Time constant register B	TCORB	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8208h	TMR0	Timer counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 8209h	TMR1	Timer counter	TCNT	8	8*5	2, 3 PCLKB	2 ICLK	
0008 820Ah	TMR0	Timer counter control register	TCCR	8	8	2, 3 PCLKB	2 ICLK	
0008 820Bh	TMR1	Timer counter control register	TCCR	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8210h	TMR2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8211h	TMR3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8212h	TMR2	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8213h	TMR3	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8214h	TMR2	Time constant register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	
0008 8215h	TMR3	Time constant register A	TCORA	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8216h	TMR2	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	
0008 8217h	TMR3	Time constant register B	TCORB	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8218h	TMR2	Timer counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 8219h	TMR3	Timer counter	TCNT	8	8*5	2, 3 PCLKB	2 ICLK	
0008 821Ah	TMR2	Timer counter control register	TCCR	8	8	2, 3 PCLKB	2 ICLK	
0008 821Bh	TMR3	Timer counter control register	TCCR	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8280h	CRC	CRC control register	CRCCR	8	8	2, 3 PCLKB	2 ICLK	CRC
0008 8281h	CRC	CRC data input register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK	
0008 8282h	CRC	CRC data output register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8300h	RIIC0	I^2C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIIC
0008 8301h	RIIC0	I^2C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8302h	RIIC0	I^2C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8303h	RIIC0	I^2C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8304h	RIIC0	I^2C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 8305h	RIIC0	I^2C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK	
0008 8306h	RIIC0	I^2C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK	
0008 8307h	RIIC0	I^2C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8308h	RIIC0	I^2C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8309h	RIIC0	I^2C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 830Ah	RIIC0	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 830Ah	RIIC0	Timeout Internal Counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK	
0008 830Bh	RIIC0	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 830Bh	RIIC0	Timeout Internal Counter U	TMOCNTU	8	8	2, 3 PCLKB	2 ICLK	
0008 830Ch	RIIC0	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 830Dh	RIIC0	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 830Eh	RIIC0	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	
0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	
0008 8310h	RIIC0	I^2C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	
0008 8311h	RIIC0	I^2C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8312h	RIIC0	I^2C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	
0008 8313h	RIIC0	I^2C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	
0008 8320h	RIIC1	I^2C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8321h	RIIC1	I^2C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8322h	RIIC1	I^2C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8323h	RIIC1	I^2C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8324h	RIIC1	I^2C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 8325h	RIIC1	I^2C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK	
0008 8326h	RIIC1	I^2C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (19/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 836Fh	RIIC3	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	RIIC
0008 8370h	RIIC3	I^2C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	
0008 8371h	RIIC3	I^2C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8372h	RIIC3	I^2C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	
0008 8373h	RIIC3	I^2C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	
0008 8380h	RSPI0	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK	RSPI
0008 8381h	RSPI0	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK	
0008 8382h	RSPI0	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8383h	RSPI0	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8384h	RSPI0	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK	
0008 8388h	RSPI0	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8389h	RSPI0	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Ah	RSPI0	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Bh	RSPI0	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Ch	RSPI0	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK	
0008 838Dh	RSPI0	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK	
0008 838Eh	RSPI0	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK	
0008 838Fh	RSPI0	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8390h	RSPI0	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK	
0008 8392h	RSPI0	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	
0008 8394h	RSPI0	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK	
0008 8396h	RSPI0	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK	
0008 8398h	RSPI0	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK	
0008 839Ah	RSPI0	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK	
0008 839Ch	RSPI0	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK	
0008 839Eh	RSPI0	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK	
0008 83A0h	RSPI1	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A1h	RSPI1	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK	
0008 83A2h	RSPI1	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A3h	RSPI1	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A4h	RSPI1	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK	
0008 83A8h	RSPI1	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A9h	RSPI1	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83AAh	RSPI1	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK	
0008 83ABh	RSPI1	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83ACh	RSPI1	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK	
0008 83ADh	RSPI1	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK	
0008 83AEh	RSPI1	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK	
0008 83AFh	RSPI1	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 83B0h	RSPI1	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK	
0008 83B2h	RSPI1	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	
0008 83B4h	RSPI1	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK	
0008 83B6h	RSPI1	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK	
0008 83B8h	RSPI1	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK	
0008 83BAh	RSPI1	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK	
0008 83BCh	RSPI1	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK	
0008 83BEh	RSPI1	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK	
0008 83C0h	RSPI2	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83C1h	RSPI2	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK	
0008 83C2h	RSPI2	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (22/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8804h	MTU2	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	MTU2a
0008 8805h	MTU2	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8806h	MTU2	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8808h	MTU2	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 880Ah	MTU2	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8880h	MTU5	Timer counter U	TCNTU	16	16	2, 3 PCLKB	2 ICLK	
0008 8882h	MTU5	Timer general register U	TGRU	16	16	2, 3 PCLKB	2 ICLK	
0008 8884h	MTU5	Timer control register U	TCRU	8	8	2, 3 PCLKB	2 ICLK	
0008 8886h	MTU5	Timer I/O control register U	TIORU	8	8	2, 3 PCLKB	2 ICLK	
0008 8890h	MTU5	Timer counter V	TCNTV	16	16	2, 3 PCLKB	2 ICLK	
0008 8892h	MTU5	Timer general register V	TGRV	16	16	2, 3 PCLKB	2 ICLK	
0008 8894h	MTU5	Timer control register V	TCRV	8	8	2, 3 PCLKB	2 ICLK	
0008 8896h	MTU5	Timer I/O control register V	TIORV	8	8	2, 3 PCLKB	2 ICLK	
0008 88A0h	MTU5	Timer counter W	TCNTW	16	16	2, 3 PCLKB	2 ICLK	
0008 88A2h	MTU5	Timer general register W	TGRW	16	16	2, 3 PCLKB	2 ICLK	
0008 88A4h	MTU5	Timer control register W	TCRW	8	8	2, 3 PCLKB	2 ICLK	
0008 88A6h	MTU5	Timer I/O control register W	TIORW	8	8	2, 3 PCLKB	2 ICLK	
0008 88B2h	MTU5	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 88B4h	MTU5	Timer start register	TSTR	8	8	2, 3 PCLKB	2 ICLK	
0008 88B6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	2, 3 PCLKB	2 ICLK	
0008 8900h	POE	Input level control/status register 1	ICSR1	16	16	2, 3 PCLKB	2 ICLK	POE2a
0008 8902h	POE	Output level control/status register 1	OCSR1	16	16	2, 3 PCLKB	2 ICLK	
0008 8908h	POE	Input level control/status register 2	ICSR2	16	16	2, 3 PCLKB	2 ICLK	
0008 890Ah	POE	Software port output enable register	SPOER	8	8	2, 3 PCLKB	2 ICLK	
0008 890Bh	POE	Port output enable control register 1	POECR1	8	8	2, 3 PCLKB	2 ICLK	
0008 890Ch	POE	Port output enable control register 2	POECR2	8	8	2, 3 PCLKB	2 ICLK	
0008 890Eh	POE	Input level control/status register 3	ICSR3	16	16	2, 3 PCLKB	2 ICLK	
0008 9000h	S12AD	A/D control register	ADCSR	8	8	2, 3 PCLKB	2 ICLK	S12ADa
0008 9004h	S12AD	A/D channel select register 0	ADANS0	16	16	2, 3 PCLKB	2 ICLK	
0008 9006h	S12AD	A/D channel select register 1	ADANS1	16	16	2, 3 PCLKB	2 ICLK	
0008 9008h	S12AD	A/D-converted value addition mode select register 0	ADADS0	16	16	2, 3 PCLKB	2 ICLK	
0008 900Ah	S12AD	A/D-converted value addition mode select register 1	ADADS1	16	16	2, 3 PCLKB	2 ICLK	
0008 900Ch	S12AD	A/D-converted value addition count select register	ADADC	8	8	2, 3 PCLKB	2 ICLK	
0008 900Eh	S12AD	A/D control extended register	ADCER	16	16	2, 3 PCLKB	2 ICLK	
0008 9010h	S12AD	A/D start trigger select register	ADSTRGR	8	8	2, 3 PCLKB	2 ICLK	
0008 9012h	S12AD	A/D conversion extended input control register	ADEXICR	16	16	2, 3 PCLKB	2 ICLK	
0008 901Ah	S12AD	A/D temperature sensor data register	ADTSDR	16	16	2, 3 PCLKB	2 ICLK	
0008 901Ch	S12AD	A/D internal reference voltage data register	ADOCDR	16	16	2, 3 PCLKB	2 ICLK	
0008 9020h	S12AD	A/D data register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK	
0008 9022h	S12AD	A/D data register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK	
0008 9024h	S12AD	A/D data register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK	
0008 9026h	S12AD	A/D data register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK	
0008 9028h	S12AD	A/D data register 4	ADDR4	16	16	2, 3 PCLKB	2 ICLK	
0008 902Ah	S12AD	A/D data register 5	ADDR5	16	16	2, 3 PCLKB	2 ICLK	
0008 902Ch	S12AD	A/D data register 6	ADDR6	16	16	2, 3 PCLKB	2 ICLK	
0008 902Eh	S12AD	A/D data register 7	ADDR7	16	16	2, 3 PCLKB	2 ICLK	
0008 9030h	S12AD	A/D data register 8	ADDR8	16	16	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (28/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 B332h	SCI12	Timer prescaler register	TPRE	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 B333h	SCI12	Timer count register	TCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C000h	PORT0	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C001h	PORT1	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C002h	PORT2	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C003h	PORT3	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C004h	PORT4	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C005h	PORT5	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C006h	PORT6	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C007h	PORT7	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C008h	PORT8	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C009h	PORT9	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Ah	PORTA	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Bh	PORTB	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Ch	PORTC	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Dh	PORTD	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Eh	PORTE	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Fh	PORTF	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C010h	PORTG	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C011h	PORTH	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C012h	PORTJ	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C013h	PORTK	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C014h	PORTL	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C020h	PORT0	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C021h	PORT1	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C022h	PORT2	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C023h	PORT3	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C024h	PORT4	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C025h	PORT5	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C026h	PORT6	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C027h	PORT7	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C028h	PORT8	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C029h	PORT9	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Ah	PORTA	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Bh	PORTB	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Ch	PORTC	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Dh	PORTD	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Eh	PORTE	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Fh	PORTF	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C030h	PORTG	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C031h	PORTH	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C032h	PORTJ	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C033h	PORTK	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C034h	PORTL	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C040h	PORT0	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C041h	PORT1	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C042h	PORT2	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C043h	PORT3	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C044h	PORT4	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C045h	PORT5	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (41/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000A 0094h	USB0	Pipe 2 transaction counter enable register	PIPE2TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	USBa
000A 0096h	USB0	Pipe 2 transaction counter register	PIPE2TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	
000A 0098h	USB0	Pipe 3 transaction counter enable register	PIPE3TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	
000A 009Ah	USB0	Pipe 3 transaction counter register	PIPE3TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	
000A 009Ch	USB0	Pipe 4 transaction counter enable register	PIPE4TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	
000A 009Eh	USB0	Pipe 4 transaction counter register	PIPE4TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	
000A 00A0h	USB0	Pipe 5 transaction counter enable register	PIPE5TRE	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	
000A 00A2h	USB0	Pipe 5 transaction counter register	PIPE5TRN	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	
000A 0400h	USB0	Deep standby USB transceiver control/pin monitor register	DPUSR0R	32	32	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	
000A 0404h	USB0	Deep standby USB suspend/resume interrupt register	DPUSR1R	32	32	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/(frequency ratio of ICLK/PCLKB)*8	

Table 4.1 List of I/O Registers (Address Order) (42/42)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
007F C402h	FLASH	Flash mode register	FMODR	8	8	2, 3 FCLK	2, 3 ICLK	Flash Memory
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2, 3 FCLK	2, 3 ICLK	
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2, 3 FCLK	2, 3 ICLK	
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2, 3 FCLK	2, 3 ICLK	
007F C440h	FLASH	E2 DataFlash read enable register 0	DFLRE0	16	16	2, 3 FCLK	2, 3 ICLK	
007F C442h	FLASH	E2 DataFlash read enable register 1	DFLRE1	16	16	2, 3 FCLK	2, 3 ICLK	
007F C450h	FLASH	E2 DataFlash P/E enable register 0	DFLWE0	16	16	2, 3 FCLK	2, 3 ICLK	
007F C452h	FLASH	E2 DataFlash P/E enable register 1	DFLWE1	16	16	2, 3 FCLK	2, 3 ICLK	
007F C454h	FLASH	FCU RAM enable register	FCURAME	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2, 3 FCLK	2, 3 ICLK	
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2, 3 FCLK	2, 3 ICLK	
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFB4h	FLASH	Flash protection register	FPROTR	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFCAh	FLASH	E2 data flash blank check control register	DFLBCCNT	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFCEh	FLASH	E2 DataFlash blank check status register	DFLBCSTAT	16	16	2, 3 FCLK	2, 3 ICLK	
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2, 3 FCLK	2, 3 ICLK	
FEFF FAC0h	FLASH	Unique ID register 0*9	UIDR0	8	8	1 ICLK	1 ICLK	
FEFF FAC1h	FLASH	Unique ID register 1*9	UIDR1	8	8	1 ICLK	1 ICLK	
FEFF FAC2h	FLASH	Unique ID register 2*9	UIDR2	8	8	1 ICLK	1 ICLK	
FEFF FAC3h	FLASH	Unique ID register 3*9	UIDR3	8	8	1 ICLK	1 ICLK	
FEFF FAC4h	FLASH	Unique ID register 4*9	UIDR4	8	8	1 ICLK	1 ICLK	
FEFF FAC5h	FLASH	Unique ID register 5*9	UIDR5	8	8	1 ICLK	1 ICLK	
FEFF FAC6h	FLASH	Unique ID register 6*9	UIDR6	8	8	1 ICLK	1 ICLK	
FEFF FAC7h	FLASH	Unique ID register 7*9	UIDR7	8	8	1 ICLK	1 ICLK	
FEFF FAC8h	FLASH	Unique ID register 8*9	UIDR8	8	8	1 ICLK	1 ICLK	
FEFF FAC9h	FLASH	Unique ID register 9*9	UIDR9	8	8	1 ICLK	1 ICLK	
FEFF FACAh	FLASH	Unique ID register 10*9	UIDR10	8	8	1 ICLK	1 ICLK	
FEFF FACBh	FLASH	Unique ID register 11*9	UIDR11	8	8	1 ICLK	1 ICLK	
FEFF FACCh	FLASH	Unique ID register 12*9	UIDR12	8	8	1 ICLK	1 ICLK	
FEFF FACDh	FLASH	Unique ID register 13*9	UIDR13	8	8	1 ICLK	1 ICLK	
FEFF FACEh	FLASH	Unique ID register 14*9	UIDR14	8	8	1 ICLK	1 ICLK	
FEFF FACFh	FLASH	Unique ID register 15*9	UIDR15	8	8	1 ICLK	1 ICLK	
FEFF FAD2h	TEMPS	Temperature sensor calibration data register*9	TSCDRL	8	8	1 ICLK	1 ICLK	Temperature sensor
FEFF FAD3h	TEMPS	Temperature sensor calibration data register*9	TSCDRH	8	8	1 ICLK	1 ICLK	

Note 1. When the same output trigger is specified for pulse output groups 2 and 3 by the PPG0.PCR setting, the PPG0.NDRH address is 000881ECh. When different output triggers are specified, the PPG0.NDRH addresses for pulse output groups 2 and 3 are 000881EEh and 000881ECh, respectively.

Note 2. When the same output trigger is specified for pulse output groups 0 and 1 by the PPG0.PCR setting, the PPG0.NDRL address is 000881EDh. When different output triggers are specified, the PPG0.NDRL addresses for pulse output groups 0 and 1 are 000881EFh and 000881EDh, respectively.

Note 3. When the same output trigger is specified for pulse output groups 6 and 7 by the PPG1.PCR setting, the PPG1.NDRH address is 000881FCh. When different output triggers are specified, the PPG1.NDRH addresses for pulse output groups 6 and 7 are 000881FEh and 000881FCh, respectively.

Note 4. When the same output trigger is specified for pulse output groups 4 and 5 by the PPG1.PCR setting, the PPG1.NDRL address is 000881FDh. When different output triggers are specified, the PPG1.NDRL addresses for pulse output groups 4 and 5 are 000881FFh and 000881FDh, respectively.

Note 5. Odd addresses should not be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0 or TMR2 register. Table 26.4 lists register allocation for 16-bit access in the User's manual: Hardware.

Note 6. The CAN2 module is not provided in products less than 1 Mbyte of ROM.

Note 7. The CAN0 module is not provided in products less than 512 Kbytes of ROM.

Note 8. When the register is accessed while the USB is operating, a delay may be generated in accessing.

Note 9. These registers are only present in the G version.

5.2 DC Characteristics

Table 5.2 DC Characteristics (1)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin*1 MTU input pin*1 TMR input pin*1 SCI input pin*1 ADTRG# input pin*1 RES#, NMI	V_{IH}	VCC × 0.8	—	VCC + 0.3	V	
		V_{IL}	–0.3	—	VCC × 0.2		
		ΔV_T	VCC × 0.06	—	—		
	RIIC input pin (except for SMBus)	V_{IH}	VCC × 0.7	—	5.8		
		V_{IL}	–0.3	—	VCC × 0.3		
		ΔV_T	VCC × 0.05	—	—		
	Ports for 5 V tolerant*2	V_{IH}	VCC × 0.8	—	5.8		
		V_{IL}	–0.3	—	VCC × 0.2		
	Other input pins excluding ports for 5 V tolerant*3	V_{IH}	VCC × 0.8	—	VCC + 0.3		
		V_{IL}	–0.3	—	VCC × 0.2		
Input high voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL, RSPI, WAIT#, TCK		VCC × 0.8	—	VCC + 0.3		
	XCIN*3		VCC × 0.8	—	VCC + 0.3		
	D0 to D31		VCC × 0.7	—	VCC + 0.3		
	RIIC (SMBus)		2.1	—	VCC + 0.3		
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	–0.3	—	VCC × 0.1	V	
	EXTAL, RSPI, WAIT#, TCK		–0.3	—	VCC × 0.2		
	XCIN*3		–0.3	—	VCC × 0.2		
	D0 to D31		–0.3	—	VCC × 0.3		
	RIIC (SMBus)		–0.3	—	0.8		

Note 1. This does not include the pins, which are multiplexed as ports for 5 V tolerant.
Note 2. Ports 07, 12 to 17, 20 to 25, 30 to 34, 50 to 52, 54 to 57, 67, 74 to 77, 80 to 82, A1 to A4, A6, B, and C are 5 V tolerant.
Note 3. For P32, P31, P30, and XCIN, input as follows when the V_{BATT} power supply is selected.
VIH Min. = V_{BATT} × 0.8, VIH Max. = V_{BATT} + 0.3, VIL Min. = –0.3, VIL Max. = V_{BATT} × 0.2

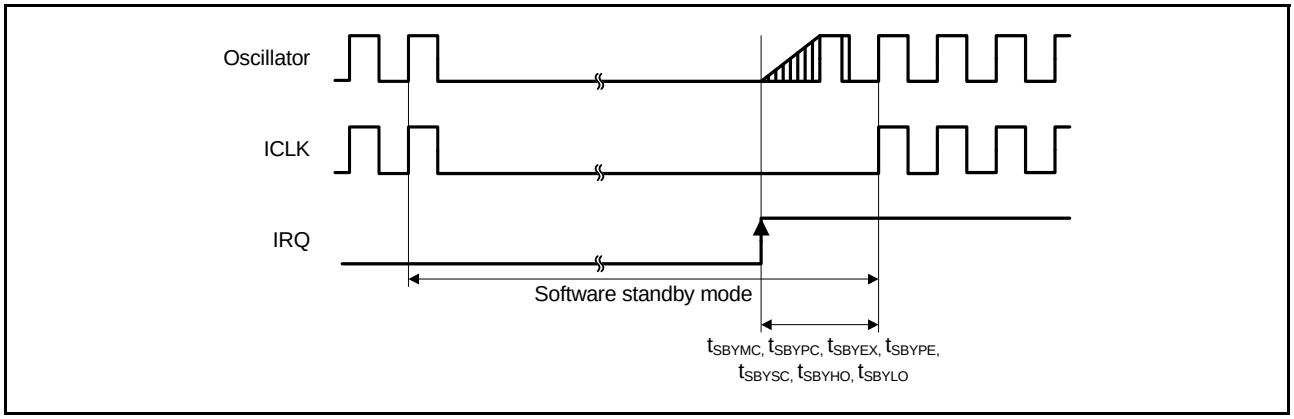


Figure 5.13 Software Standby Mode Cancellation Timing

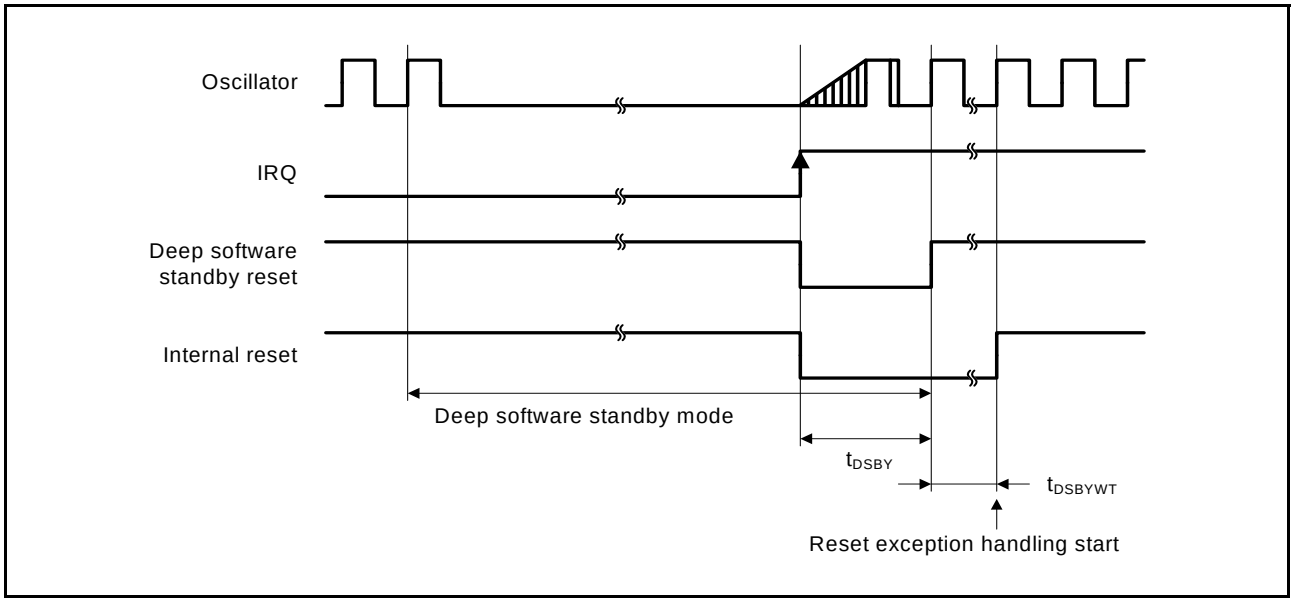


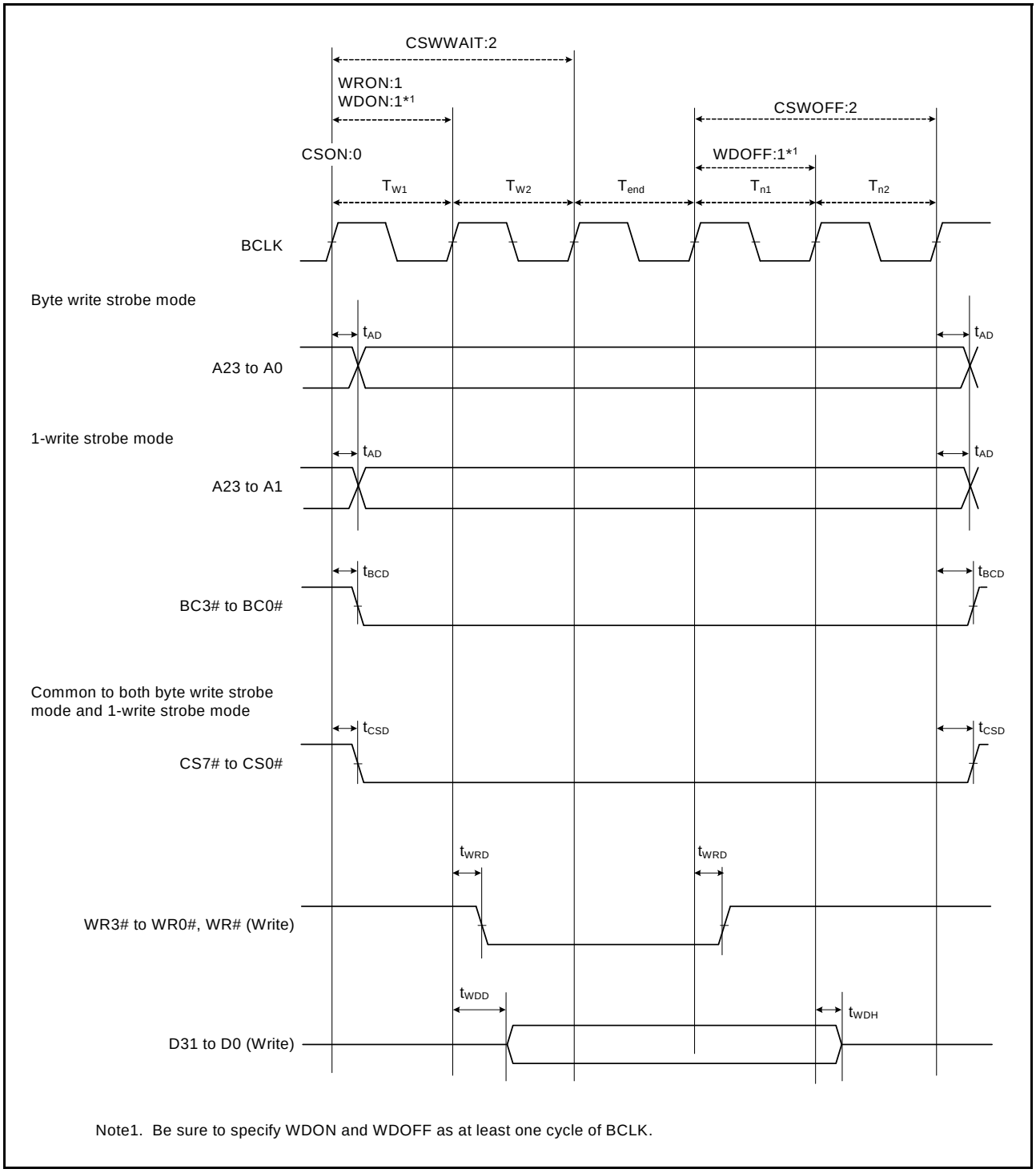
Figure 5.14 Deep Software Standby Mode Cancellation Timing

5.3.4 Control Signal Timing

Table 5.14 Control Signal Timing

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	tc (PCLK) × 2 ≤ 200 ns Figure 5.15
		tc (PCLK) × 2				tc (PCLK) × 2 > 200 ns Figure 5.15
IRQ pulse width	t_{IRQW}	200	—	—	ns	tc (PCLK) × 2 ≤ 200 ns Figure 5.16
		tc (PCLK) × 2				tc (PCLK) × 2 > 200 ns Figure 5.16



Note1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 5.20 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

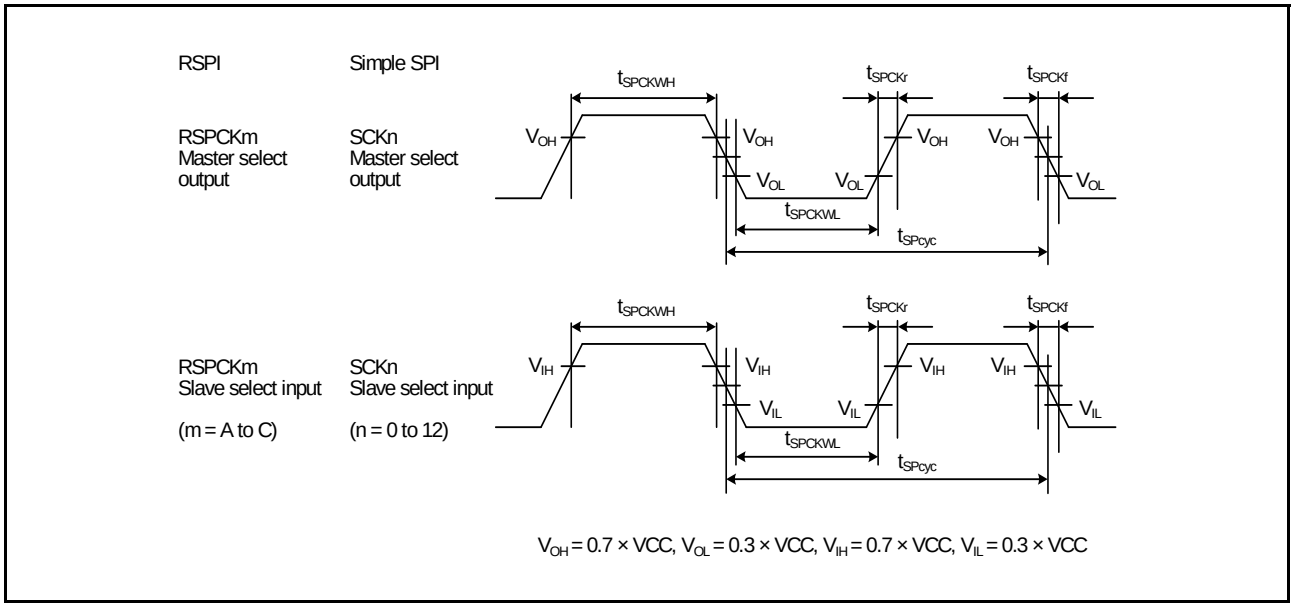


Figure 5.32 RSPI Clock Timing and Simple SPI Clock Timing

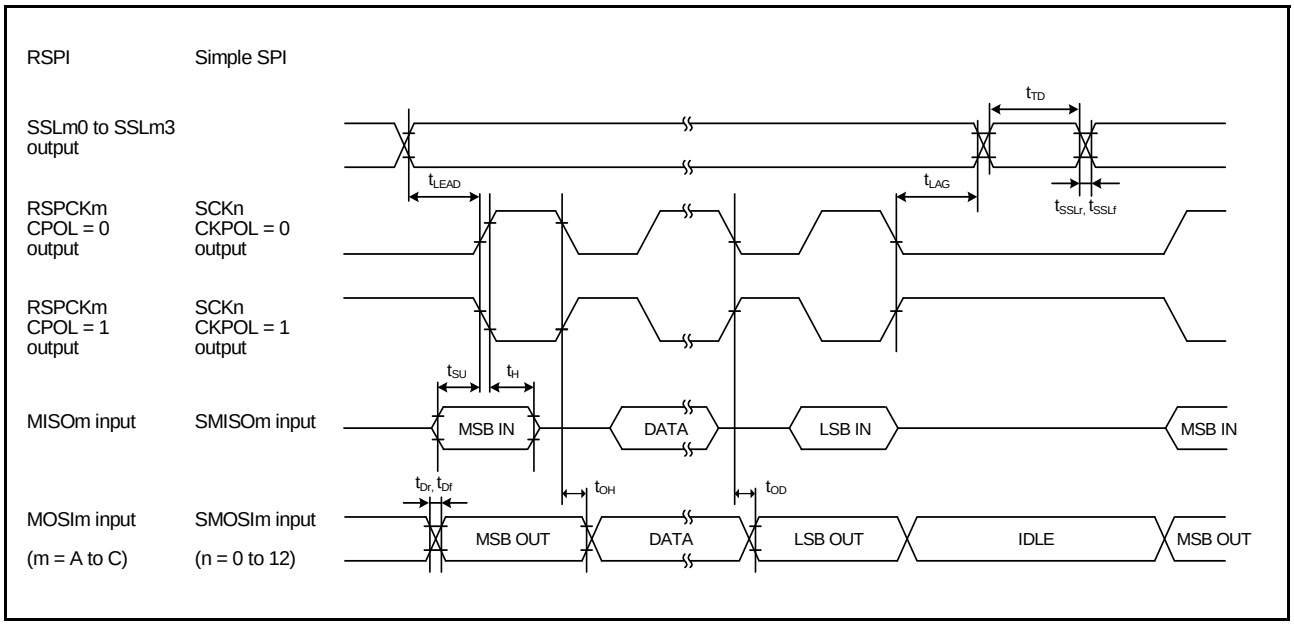


Figure 5.33 RSPI Timing (Master, CPHA = 0) and Simple SPI Timing (Master, CKPH = 1)

Table 5.23 12-Bit A/D Conversion Characteristics

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a = T_{opr}$

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			12	12	12	Bit	
Conversion time*1 (Operation at PCLK = 50 MHz)	AN0 to AN7	Permissible signal source impedance (max.) = 1.0 kΩ	1.0 (0.4)*2	—	—	µs	Sampling in 20 states
	Other channels	Permissible signal source impedance (max.) = 1.0 kΩ, AVCC ≥ 3.0 V	2.0 (1.4)*2	—	—	µs	Sampling in 70 states
		Permissible signal source impedance (max.) = 1.0 kΩ, AVCC ≥ 2.7 V	5.6 (5.0)*2	—	—	µs	Sampling in 250 states
Analog input capacitance			—	—	30	pF	
Offset error			—	±2.0	±7.5	LSB	
Full-scale error			—	±2.0	±7.5	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	±2.5	±8.0	LSB	
DNL differential nonlinearity error			—	±2.0	±4.0	LSB	
INL integral nonlinearity error			—	±2.0	±4.0	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.
Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The value in parentheses indicates the sampling time.

Table 5.24 A/D Internal Reference Voltage Characteristics

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
A/D Internal reference voltage	1.45	1.50	1.55	V	

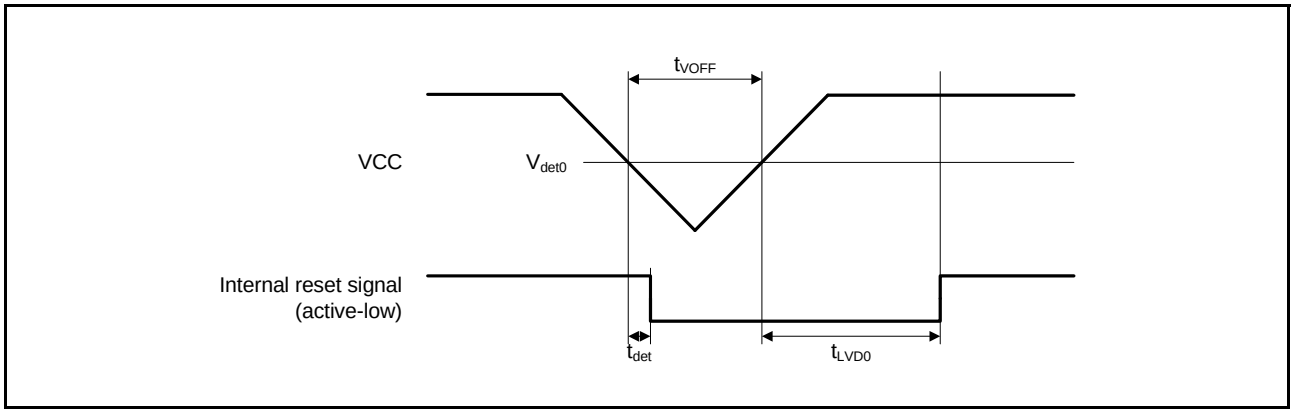


Figure 5.41 Voltage Detection Circuit Timing (V_{det0})

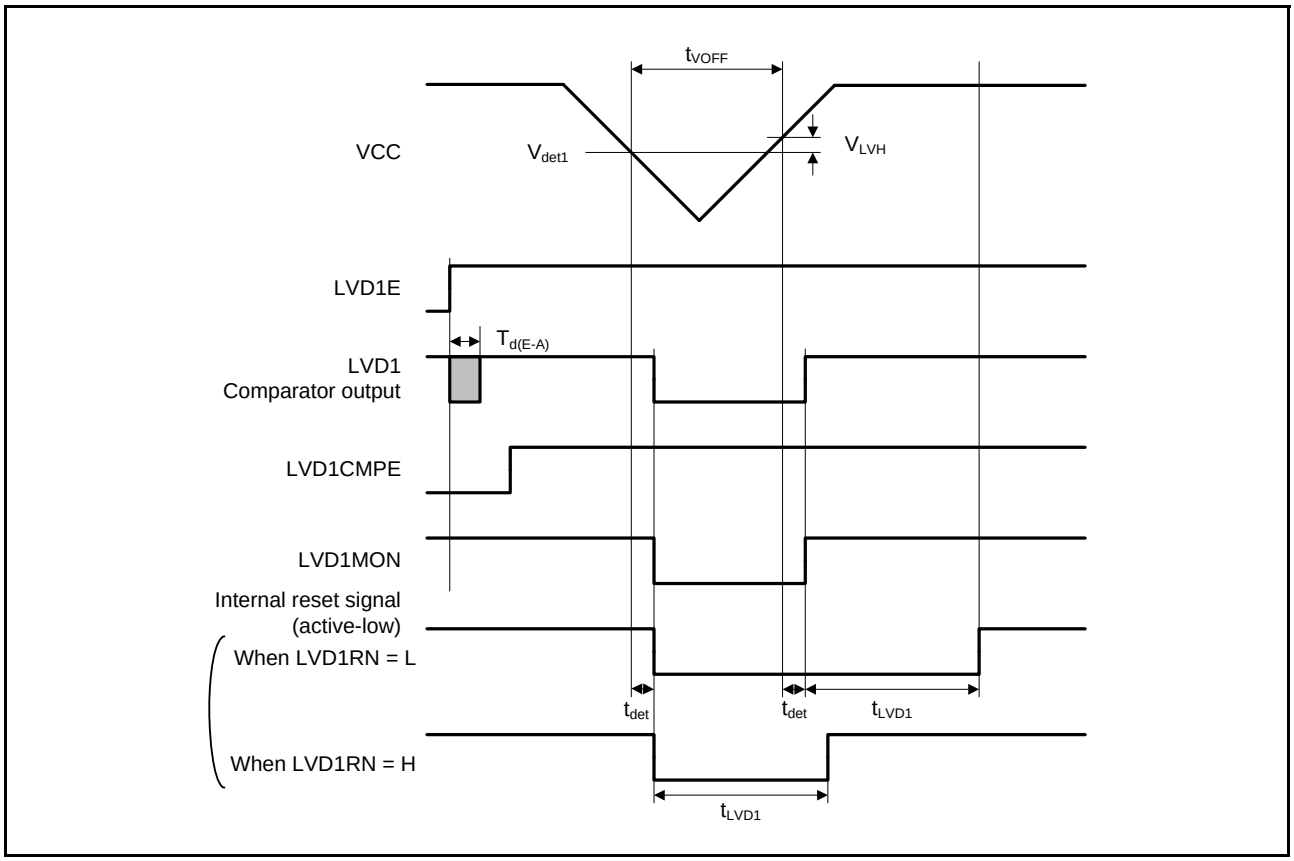


Figure 5.42 Voltage Detection Circuit Timing (V_{det1})

5.9 Oscillation Stop Detection Timing

Table 5.28 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.44

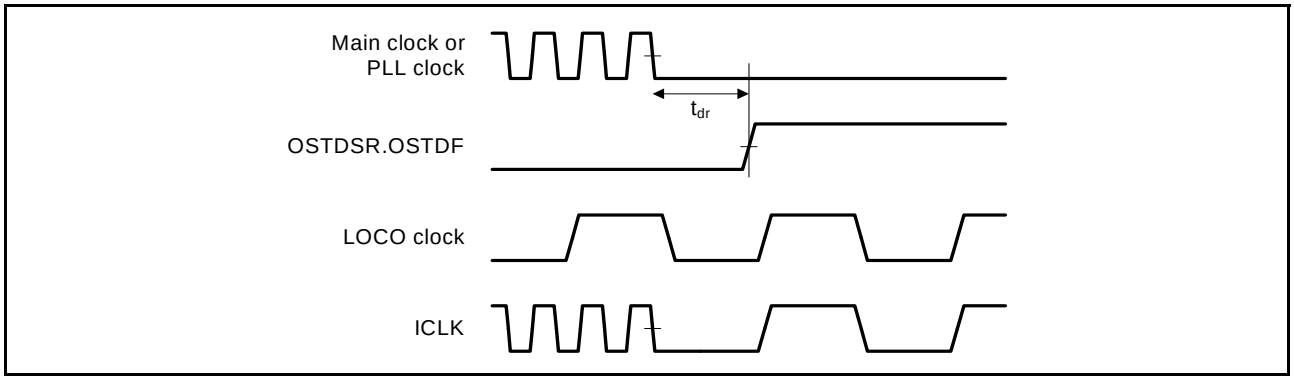
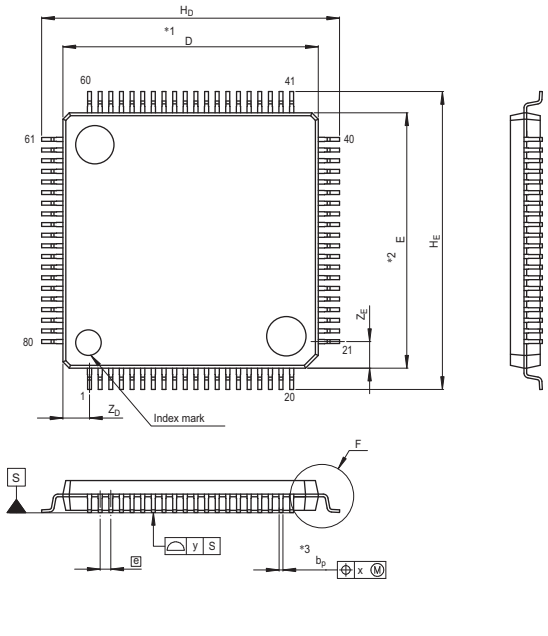
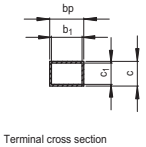
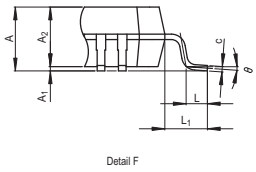


Figure 5.44 Oscillation Stop Detection Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure H 80-Pin LQFP (PLQP0080KB-A)

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