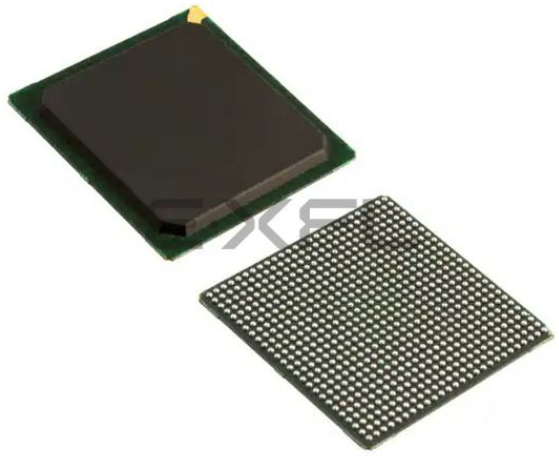

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	444
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3pe1500-1fgg676i

I/Os Per Package[1]

ProASIC3E Devices	A3PE600		A3PE1500 [3]		A3PE3000 [3]	
Cortex-M1 Devices [2]			M1A3PE1500		M1A3PE3000	
	I/O Types					
Package	Single-Ended I/O[1]	Differential I/O Pairs	Single-Ended I/O[1]	Differential I/O Pairs	Single-Ended I/O[1]	Differential I/O Pairs
PQ208	147	65	147	65	147	65
FG256	165	79	–	–	–	–
FG324	–	–	–	–	221	110
FG484	270	135	280	139	341	168
FG676	–	–	444	222	–	–
FG896	–	–	–	–	620	310

Notes:

1. *When considering migrating your design to a lower- or higher-density device, refer to the ProASIC3E FPGA Fabric User's Guide to ensure compliance with design and board migration requirements.*
2. *Each used differential I/O pair reduces the number of single-ended I/Os available by two.*
3. *For A3PE1500 and A3PE3000 devices, the usage of certain I/O standards is limited as follows:*
   – SSTL3(I) and (II): up to 40 I/Os per north or south bank
   – LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank
   – SSTL2(I) and (II) / GTL+ 2.5 V/ GTL 2.5 V: up to 72 I/Os per north or south bank
4. *FG256 and FG484 are footprint-compatible packages.*
5. *When using voltage-referenced I/O standards, one I/O pin should be assigned as a voltage-referenced pin (VREF) per minibank (group of I/Os).*
6. *"G" indicates RoHS-compliant packages. Refer to the "ProASIC3E Ordering Information" on page III for the location of the "G" in the part number.*

Table 1-2 • ProASIC3E FPGAs Package Sizes Dimensions

Package	PQ208	FG256	FG324	FG484	FG676	FG896
Length × Width (mm\mm)	28 × 28	17 × 17	19 × 19	23 × 23	27 × 27	31 × 31
Nominal Area (mm^2)	784	289	361	529	729	961
Pitch (mm)	0.5	1.0	1.0	1.0	1.0	1.0
Height (mm)	3.40	1.60	1.63	2.23	2.23	2.23

ProASIC3E Device Status

ProASIC3E Devices	Status	M1 ProASIC3E Devices	Status
A3PE600	Production		
A3PE1500	Production	M1A3PE1500	Production
A3PE3000	Production	M1A3PE3000	Production

VersaTiles

The ProASIC3E core consists of VersaTiles, which have been enhanced beyond the ProASIC[PLUS]® core tiles. The ProASIC3E VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-2 for VersaTile configurations.

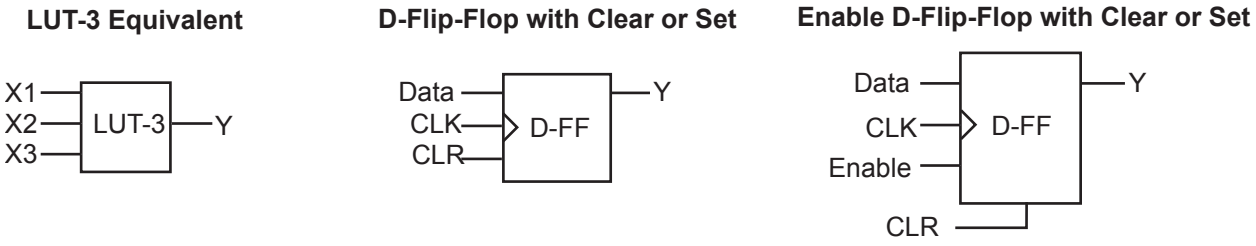

Figure 1-2 • **VersaTile Configurations**

User Nonvolatile FlashROM

ProASIC3E devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3E IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC3E development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

2 – ProASIC3E DC and Switching Characteristics

General Specifications

DC and switching characteristics for –F speed grade targets are based only on simulation.

The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI [2]	DC I/O output buffer supply voltage	–0.3 to 3.75	V
VMV [2]	DC I/O input buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG} [3]	Storage temperature	–65 to +150	°C
T_J [3]	Junction temperature	+125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-3 on page 2-2.*
2. *VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information.*
3. *For flash programming and retention maximum limits, refer to Table 2-3 on page 2-2, and for recommended operating limits, refer to Table 2-2 on page 2-2.*

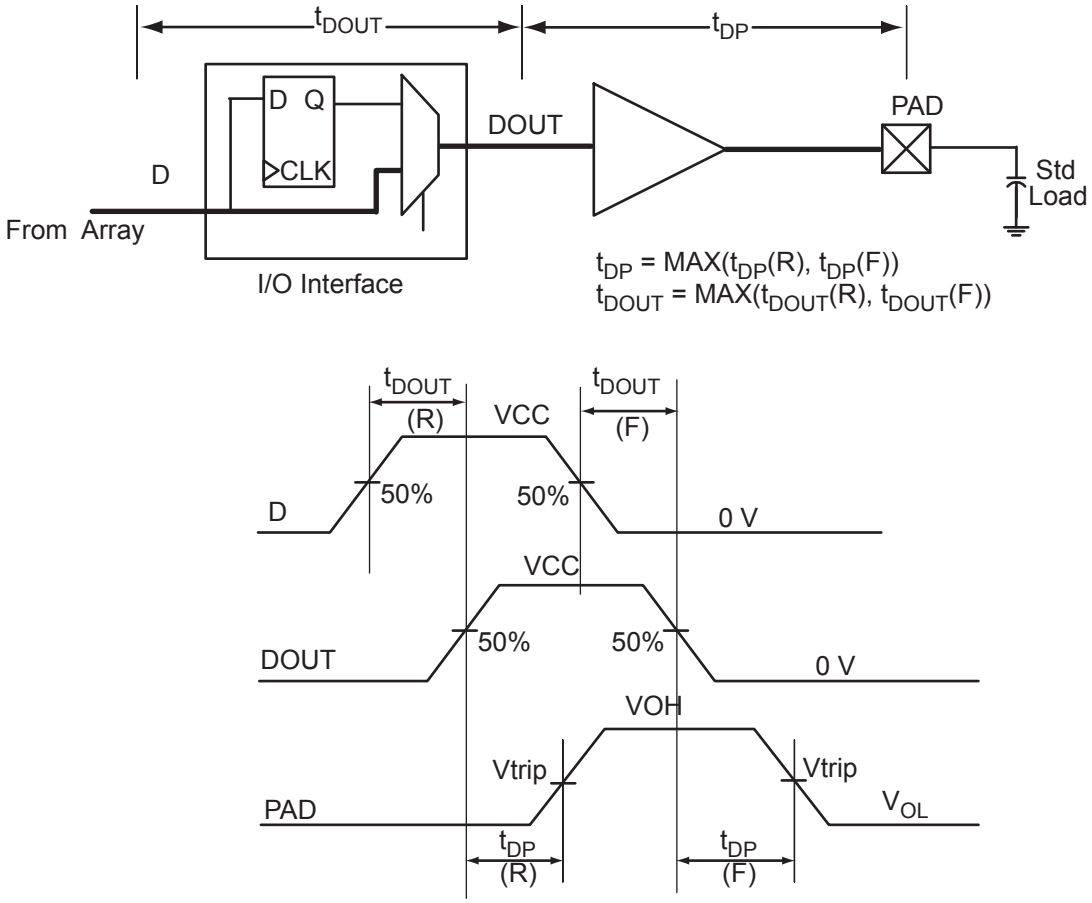

Figure 2-4 • **Output Buffer Model and Delays (example)**

Table 2-19 • I/O Output Buffer Maximum Resistances[1] (continued)

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V GTL+	35 mA	12	–
2.5 V GTL+	33 mA	15	–
HSTL (I)	8 mA	50	50
HSTL (II)	15 mA[4]	25	25
SSTL2 (I)	15 mA	27	31
SSTL2 (II)	18 mA	13	15
SSTL3 (I)	14 mA	44	69
SSTL3 (II)	21 mA	18	32

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website at www.microsemi.com/index.php?option=com_content&id=1671&lang=en&view=article.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / IOLspec
3. $R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / IOHspec
4. *Output drive strength is below JEDEC specification.*

Table 2-20 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

	$R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω)	
VCCI	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
3.3 V (Wide Range I/Os)	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / $I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / $I_{(WEAK\ PULL\text{-}DOWN\text{-}MIN)}$

Table 2-32 • 3.3 V LVCMOS Wide Range Low Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	4 mA	Std.	0.66	17.02	0.04	1.83	2.38	0.43	17.02	13.74	4.16	3.78	20.42	17.14	ns
		–1	0.56	14.48	0.04	1.55	2.02	0.36	14.48	11.69	3.54	3.21	17.37	14.58	ns
		–2	0.49	12.71	0.03	1.36	1.78	0.32	12.71	10.26	3.11	2.82	15.25	12.80	ns
100 µA	8 mA	Std.	0.66	12.16	0.04	1.83	2.38	0.43	12.16	9.78	4.70	4.74	15.55	13.17	ns
		–1	0.56	10.34	0.04	1.55	2.02	0.36	10.34	8.32	4.00	4.03	13.23	11.20	ns
		–2	0.49	9.08	0.03	1.36	1.78	0.32	9.08	7.30	3.51	3.54	11.61	9.84	ns
100µA	12 mA	Std.	0.66	9.32	0.04	1.83	2.38	0.43	9.32	7.62	5.06	5.36	12.71	11.02	ns
		–1	0.56	7.93	0.04	1.55	2.02	0.36	7.93	6.48	4.31	4.56	10.81	9.37	ns
		–2	0.49	6.96	0.03	1.36	1.78	0.32	6.96	5.69	3.78	4.00	9.49	8.23	ns
100 µA	16 mA	Std.	0.66	8.69	0.04	1.83	2.38	0.43	8.69	7.17	5.14	5.53	12.08	10.57	ns
		–1	0.56	7.39	0.04	1.55	2.02	0.36	7.39	6.10	4.37	4.71	10.28	8.99	ns
		–2	0.49	6.49	0.03	1.36	1.78	0.32	6.49	5.36	3.83	4.13	9.02	7.89	ns
100 µA	24 mA	Std.	0.66	8.11	0.04	1.83	2.38	0.43	8.11	7.13	5.23	6.13	11.50	10.52	ns
		–1	0.56	6.90	0.04	1.55	2.02	0.36	6.90	6.06	4.45	5.21	9.78	8.95	ns
		–2	0.49	6.05	0.03	1.36	1.78	0.32	6.05	5.32	3.91	4.57	8.59	7.86	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *Software default selection highlighted in gray.*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-69 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
18 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

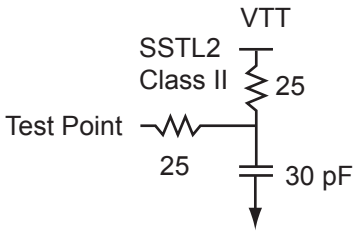

Figure 2-19 • AC Loading

Table 2-70 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-71 • SSTL 2 Class II
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	0.66	2.17	0.04	1.33	0.43	2.21	1.77			4.44	ns
–1	0.56	0.56	1.84	0.04	1.14	0.36	1.88	1.51			3.78	ns
–2	0.49	0.49	1.62	0.03	1.00	0.32	1.65	1.32			3.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by the Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and DDR. However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-22. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3E also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

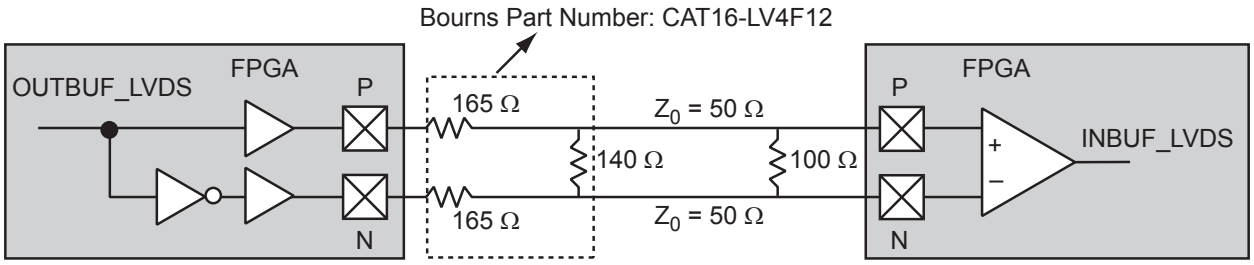

Figure 2-22 • **LVDS Circuit Diagram and Board-Level Implementation**

Timing Characteristics

Table 2-80 • LVDS
Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.66	1.87	0.04	1.82	ns
–1	0.56	1.59	0.04	1.55	ns
–2	0.49	1.40	0.03	1.36	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-23. The input and output buffer delays are available in the LVDS section in Table 2-80.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: R_S = 60 Ω and R_T = 70 Ω, given Z_0 = 50 Ω (2") and Z_{stub} = 50 Ω (~1.5").

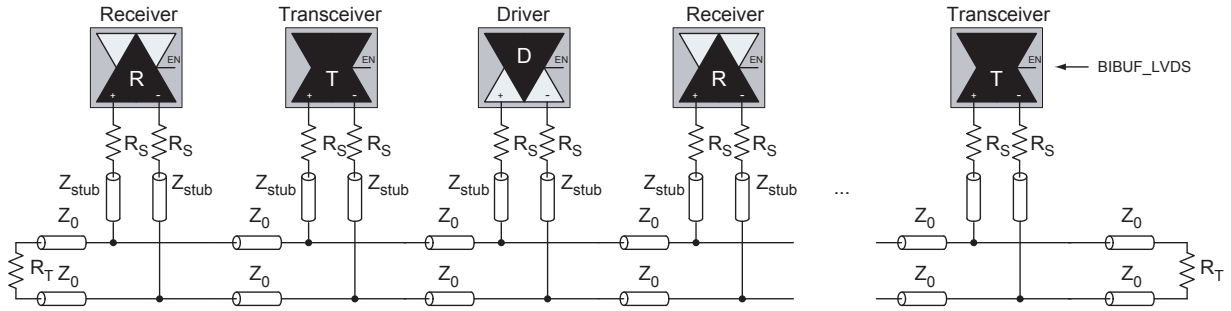

Figure 2-23 • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers

Input Register

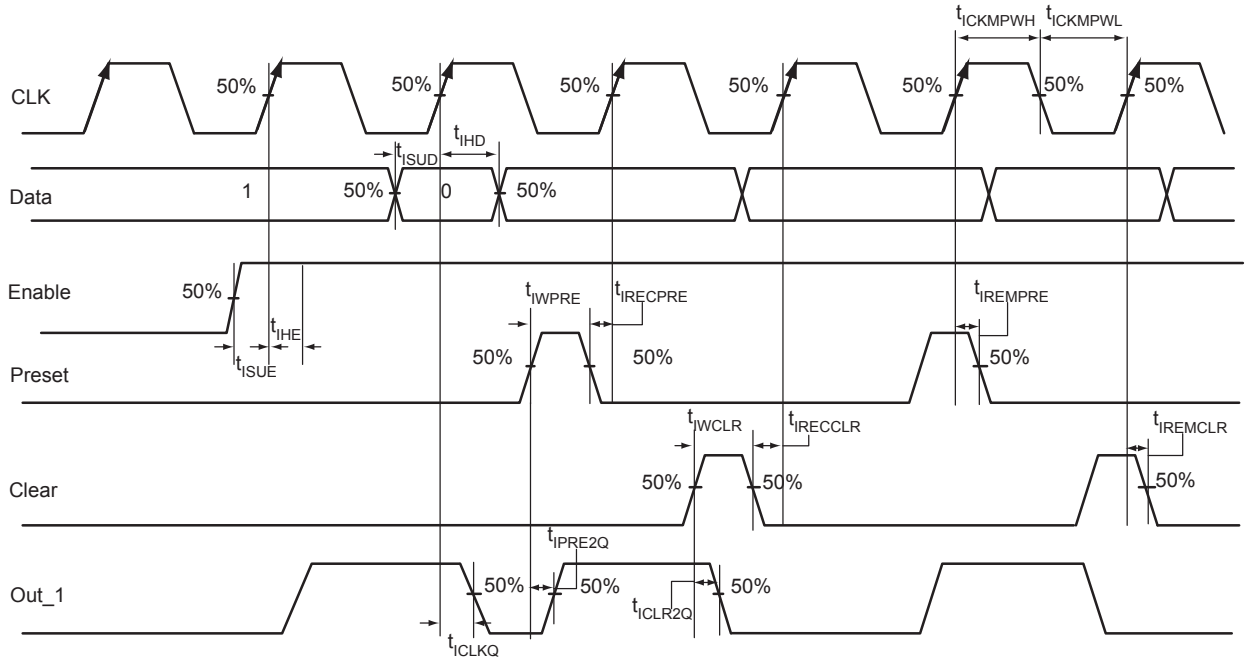

Figure 2-27 • **Input Register Timing Diagram**

Timing Characteristics

Table 2-86 • **Input Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.27	0.32	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.26	0.30	0.35	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.37	0.42	0.50	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.45	0.52	0.61	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.45	0.52	0.61	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.41	0.48	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.32	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Output Enable Register

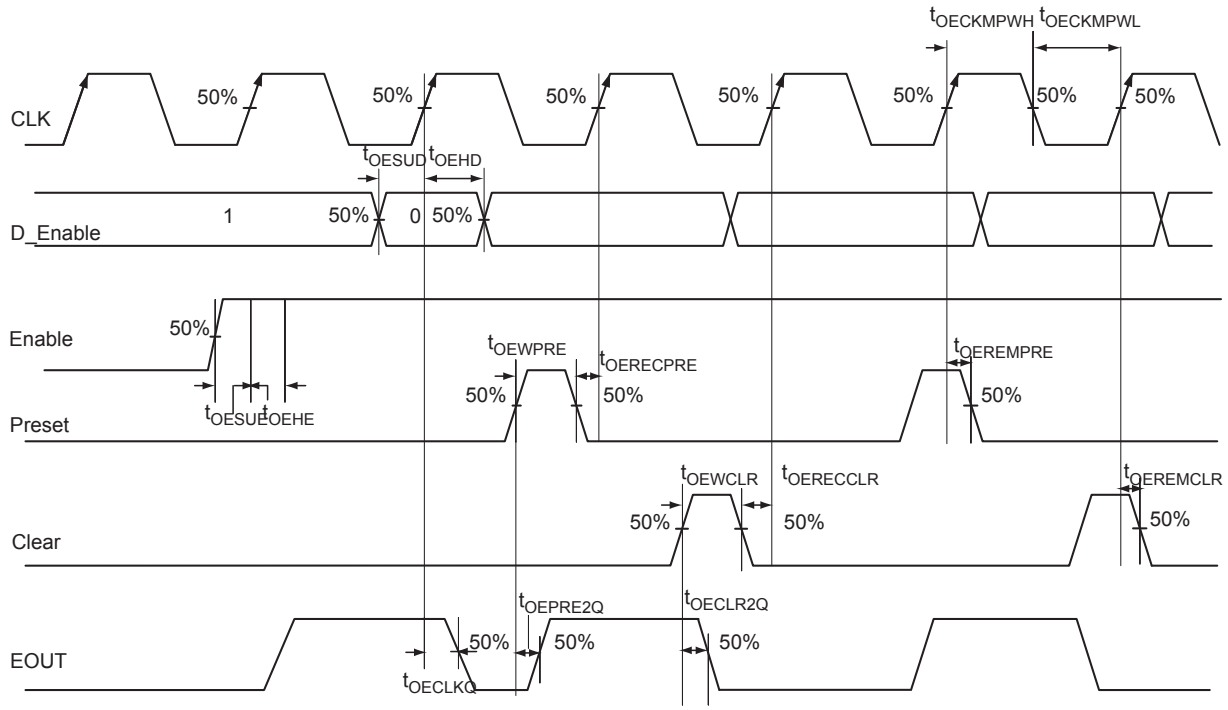

Figure 2-29 • **Output Enable Register Timing Diagram**

Timing Characteristics

Table 2-88 • **Output Enable Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.59	0.67	0.79	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.31	0.36	0.42	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.44	0.50	0.58	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.67	0.76	0.89	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.67	0.76	0.89	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.22	0.25	0.30	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.22	0.25	0.30	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.32	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Timing Characteristics

Table 2-99 • RAM4K9
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.28	0.33	ns
t_{AH}	Address hold time	0.00	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.14	0.16	0.19	ns
t_{ENH}	REN, WEN hold time	0.10	0.11	0.13	ns
t_{BKS}	BLK setup time	0.23	0.27	0.31	ns
t_{BKH}	BLK hold time	0.02	0.02	0.02	ns
t_{DS}	Input data (DIN) setup time	0.18	0.21	0.25	ns
t_{DH}	Input data (DIN) hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	1.79	2.03	2.39	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.36	2.68	3.15	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	0.89	1.02	1.20	ns
t_{C2CWWL} [1]	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Closing Edge	0.33	0.28	0.25	ns
t_{C2CWWH} [1]	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge	0.30	0.26	0.23	ns
t_{C2CRWH} [1]	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.45	0.38	0.34	ns
t_{C2CWRH} [1]	Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge	0.49	0.42	0.37	ns
t_{RSTBQ}	RESET Low to data out Low on DO (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on DO (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.21	0.24	0.29	ns
t_{CYC}	Clock cycle time	3.23	3.68	4.32	ns
F_{MAX}	Maximum frequency	310	272	231	MHz

Notes:

1. *For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

FG324	
Pin Number	**A3PE3000 FBGA**
N1	IO247NDB6V1
N2	IO247PDB6V1
N3	IO251NPB6V2
N4	GEC0/IO236NDB6V0
N5	VCOMPLE
N6	IO212NDB5V2
N7	IO212PDB5V2
N8	IO192NPB4V4
N9	IO174PDB4V2
N10	IO170PDB4V2
N11	GDA2/IO154PPB4V0
N12	GDB2/IO155PPB4V0
N13	GDA1/IO153PPB3V4
N14	VCOMPLD
N15	GDB0/IO152NDB3V4
N16	GDB1/IO152PDB3V4
N17	IO138NDB3V3
N18	IO138PDB3V3
P1	IO245PDB6V1
P2	GNDQ
P3	VMV6
P4	GEC1/IO236PDB6V0
P5	VCCPLE
P6	IO214PDB5V2
P7	VCCIB5
P8	GND
P9	IO174NDB4V2
P10	IO170NDB4V2
P11	GND
P12	VCCIB4
P13	IO155NPB4V0
P14	VCCPLD
P15	VJTAG
P16	GDC0/IO151NDB3V4
P17	GDC1/IO151PDB3V4
P18	IO142PDB3V3

FG324	
Pin Number	**A3PE3000 FBGA**
R1	IO245NDB6V1
R2	VCCIB6
R3	GEA1/IO234PPB6V0
R4	IO232NDB5V4
R5	GEB2/IO232PDB5V4
R6	IO214NDB5V2
R7	IO202PDB5V1
R8	IO194PDB5V0
R9	IO186PDB4V4
R10	IO178PDB4V3
R11	IO168NSB4V1
R12	IO164PDB4V1
R13	GDC2/IO156PDB4V0
R14	TCK
R15	VPUMP
R16	TRST
R17	VCCIB3
R18	IO142NDB3V3
T1	IO241PDB6V0
T2	GEA0/IO234NPB6V0
T3	IO233NPB5V4
T4	IO231NPB5V4
T5	VMV5
T6	IO208NDB5V1
T7	IO202NDB5V1
T8	IO194NDB5V0
T9	IO186NDB4V4
T10	IO178NDB4V3
T11	IO166NPB4V1
T12	IO164NDB4V1
T13	IO156NDB4V0
T14	VMV4
T15	TDI
T16	GNDQ
T17	TDO
T18	IO146PDB3V4

FG324	
Pin Number	**A3PE3000 FBGA**
U1	IO241NDB6V0
U2	GEA2/IO233PPB5V4
U3	GEC2/IO231PPB5V4
U4	VCCIB5
U5	GNDQ
U6	IO208PDB5V1
U7	IO198PPB5V0
U8	VCCIB5
U9	IO182NPB4V3
U10	IO180NPB4V3
U11	VCCIB4
U12	IO166PPB4V1
U13	IO162PDB4V1
U14	GNDQ
U15	VCCIB4
U16	TMS
U17	VMV3
U18	IO146NDB3V4
V1	GND
V2	IO218NDB5V3
V3	IO218PDB5V3
V4	IO206NDB5V1
V5	IO206PDB5V1
V6	IO198NPB5V0
V7	GND
V8	IO190NDB4V4
V9	IO190PDB4V4
V10	IO182PPB4V3
V11	IO180PPB4V3
V12	GND
V13	IO162NDB4V1
V14	IO160NDB4V0
V15	IO160PDB4V0
V16	IO158NDB4V0
V17	IO158PDB4V0
V18	GND

FG484	
Pin Number	A3PE3000 Function
H19	IO100PDB2V2
H20	VCC
H21	VMV2
H22	IO105PDB2V2
J1	IO285NDB7V1
J2	IO285PDB7V1
J3	VMV7
J4	IO279PDB7V0
J5	IO283PDB7V1
J6	IO281PDB7V0
J7	IO287NDB7V1
J8	VCCIB7
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB2
J16	IO84NDB2V0
J17	IO104NDB2V2
J18	IO104PDB2V2
J19	IO106PPB2V3
J20	GNDQ
J21	IO109PDB2V3
J22	IO107PDB2V3
K1	IO277NDB7V0
K2	IO277PDB7V0
K3	GNDQ
K4	IO279NDB7V0
K5	IO283NDB7V1
K6	IO281NDB7V0
K7	GFC1/IO275PPB7V0
K8	VCCIB7
K9	VCC
K10	GND

FG484	
Pin Number	A3PE3000 Function
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB2
K16	GCC1/IO112PPB2V3
K17	IO108NDB2V3
K18	IO108PDB2V3
K19	IO110NPB2V3
K20	IO106NPB2V3
K21	IO109NDB2V3
K22	IO107NDB2V3
L1	IO257PSB6V2
L2	IO276PDB7V0
L3	IO276NDB7V0
L4	GFB0/IO274NPB7V0
L5	GFA0/IO273NDB6V4
L6	GFB1/IO274PPB7V0
L7	VCOMPLF
L8	GFC0/IO275NPB7V0
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO112NPB2V3
L16	GCB1/IO113PPB2V3
L17	GCA0/IO114NPB3V0
L18	VCOMPLC
L19	GCB0/IO113NPB2V3
L20	IO110PPB2V3
L21	IO111NDB2V3
L22	IO111PDB2V3
M1	GNDQ
M2	IO255NPB6V2

FG484	
Pin Number	A3PE3000 Function
M3	IO272NDB6V4
M4	GFA2/IO272PDB6V4
M5	GFA1/IO273PDB6V4
M6	VCCPLF
M7	IO271NDB6V4
M8	GFB2/IO271PDB6V4
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO116PPB3V0
M16	GCA1/IO114PPB3V0
M17	GCC2/IO117PPB3V0
M18	VCCPLC
M19	GCA2/IO115PDB3V0
M20	IO115NDB3V0
M21	IO126PDB3V1
M22	IO124PSB3V1
N1	IO255PPB6V2
N2	IO253NDB6V2
N3	VMV6
N4	GFC2/IO270PPB6V4
N5	IO261PPB6V3
N6	IO263PDB6V3
N7	IO263NDB6V3
N8	VCCIB6
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB3
N16	IO116NPB3V0

FG484	
Pin Number	A3PE3000 Function
N17	IO132NPB3V2
N18	IO117NPB3V0
N19	IO132PPB3V2
N20	GNDQ
N21	IO126NDB3V1
N22	IO128PDB3V1
P1	IO247PDB6V1
P2	IO253PDB6V2
P3	IO270NPB6V4
P4	IO261NPB6V3
P5	IO249PPB6V1
P6	IO259PDB6V3
P7	IO259NDB6V3
P8	VCCIB6
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB3
P16	GDB0/IO152NPB3V4
P17	IO136NDB3V2
P18	IO136PDB3V2
P19	IO138PDB3V3
P20	VMV3
P21	IO130PDB3V2
P22	IO128NDB3V1
R1	IO247NDB6V1
R2	IO245PDB6V1
R3	VCC
R4	IO249NPB6V1
R5	IO251NDB6V2
R6	IO251PDB6V2
R7	GEC0/IO236NPB6V0
R8	VMV5

FG484	
Pin Number	A3PE3000 Function
R9	VCCIB5
R10	VCCIB5
R11	IO196NDB5V0
R12	IO196PDB5V0
R13	VCCIB4
R14	VCCIB4
R15	VMV3
R16	VCCPLD
R17	GDB1/IO152PPB3V4
R18	GDC1/IO151PDB3V4
R19	IO138NDB3V3
R20	VCC
R21	IO130NDB3V2
R22	IO134PDB3V2
T1	IO243PPB6V1
T2	IO245NDB6V1
T3	IO243NPB6V1
T4	IO241PDB6V0
T5	IO241NDB6V0
T6	GEC1/IO236PPB6V0
T7	VCOMPLE
T8	GNDQ
T9	GEA2/IO233PPB5V4
T10	IO206NDB5V1
T11	IO202NDB5V1
T12	IO194NDB5V0
T13	IO186NDB4V4
T14	IO186PDB4V4
T15	GNDQ
T16	VCOMPLD
T17	VJTAG
T18	GDC0/IO151NDB3V4
T19	GDA1/IO153PDB3V4
T20	IO144PDB3V3
T21	IO140PDB3V3
T22	IO134NDB3V2

FG484	
Pin Number	A3PE3000 Function
U1	IO240PPB6V0
U2	IO238PDB6V0
U3	IO238NDB6V0
U4	GEB1/IO235PDB6V0
U5	GEB0/IO235NDB6V0
U6	VMV6
U7	VCCPLE
U8	IO233NPB5V4
U9	IO222PPB5V3
U10	IO206PDB5V1
U11	IO202PDB5V1
U12	IO194PDB5V0
U13	IO176NDB4V2
U14	IO176PDB4V2
U15	VMV4
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO153NDB3V4
U20	IO144NDB3V3
U21	IO140NDB3V3
U22	IO142PDB3V3
V1	IO239PDB6V0
V2	IO240NPB6V0
V3	GND
V4	GEA1/IO234PDB6V0
V5	GEA0/IO234NDB6V0
V6	GNDQ
V7	GEC2/IO231PDB5V4
V8	IO222NPB5V3
V9	IO204NDB5V1
V10	IO204PDB5V1
V11	IO195NDB5V0
V12	IO195PDB5V0
V13	IO178NDB4V3
V14	IO178PDB4V3

FG676	
Pin Number	A3PE1500 Function
G13	IO21NDB0V2
G14	IO27PDB0V3
G15	IO35NDB1V0
G16	IO39PDB1V0
G17	IO51NDB1V2
G18	IO53NDB1V2
G19	VCCIB1
G20	GBA2/IO58PPB2V0
G21	GNDQ
G22	IO64NDB2V1
G23	IO64PDB2V1
G24	IO72PDB2V2
G25	IO72NDB2V2
G26	IO78PDB2V2
H1	IO208NDB7V2
H2	IO208PDB7V2
H3	IO209NDB7V2
H4	IO209PDB7V2
H5	IO219NDB7V3
H6	GAC2/IO219PDB7V3
H7	VCCIB7
H8	VCC
H9	VCCIB0
H10	VCCIB0
H11	VCCIB0
H12	VCCIB0
H13	VCCIB0
H14	VCCIB1
H15	VCCIB1
H16	VCCIB1
H17	VCCIB1
H18	VCCIB1
H19	VCC
H20	VCC
H21	IO58NPB2V0
H22	IO70PDB2V1

FG676	
Pin Number	A3PE1500 Function
H23	IO69PDB2V1
H24	IO76PDB2V2
H25	IO76NDB2V2
H26	IO78NDB2V2
J1	IO197NDB7V0
J2	IO197PDB7V0
J3	VMV7
J4	IO215NDB7V3
J5	IO215PDB7V3
J6	IO214PDB7V3
J7	IO214NDB7V3
J8	VCCIB7
J9	VCC
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	VCC
J15	VCC
J16	VCC
J17	VCC
J18	VCC
J19	VCCIB2
J20	IO62PDB2V0
J21	IO62NDB2V0
J22	IO70NDB2V1
J23	IO69NDB2V1
J24	VMV2
J25	IO80PDB2V3
J26	IO80NDB2V3
K1	IO195PDB7V0
K2	IO199NDB7V1
K3	IO199PDB7V1
K4	IO205NDB7V1
K5	IO205PDB7V1
K6	IO217PDB7V3

FG676	
Pin Number	A3PE1500 Function
K7	IO217NDB7V3
K8	VCCIB7
K9	VCC
K10	GND
K11	GND
K12	GND
K13	GND
K14	GND
K15	GND
K16	GND
K17	GND
K18	VCC
K19	VCCIB2
K20	IO65PDB2V1
K21	IO65NDB2V1
K22	IO74PDB2V2
K23	IO74NDB2V2
K24	IO75PDB2V2
K25	IO75NDB2V2
K26	IO84PDB2V3
L1	IO195NDB7V0
L2	IO198PPB7V0
L3	GNDQ
L4	IO201PDB7V1
L5	IO201NDB7V1
L6	IO210NDB7V2
L7	IO210PDB7V2
L8	VCCIB7
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	GND
L15	GND
L16	GND

Revision	Changes	Page
Revision 9 (Aug 2009) Product Brief v1.2	All references to speed grade –F have been removed from this document.	N/A
	The "Pro I/Os with Advanced I/O Standards" section was revised to add definitions of hot-swap and cold-sparing.	1-6
DC and Switching Characteristics v1.3	3.3 V LVCMOS and 1.2 V LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained 3.3 V LVCMOS and 1.2 V LVCMOS data.	N/A
	IIL and IIH input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables.	N/A
	–F was removed from the datasheet. The speed grade is no longer supported.	N/A
	In the Table 2-2 • Recommended Operating Conditions [1] "3.0 V DC supply voltage" and note 4 are new.	2-2
	The Table 2-4 • Overshoot and Undershoot Limits [1] table was updated.	2-3
	The Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays table was updated.	2-5
	There are new parameters and data was updated in the Table 2-99 • RAM4K9 table.	2-76
	There are new parameters and data was updated in the Table 2-100 • RAM512X18 table.	2-77
Revision 8 (Feb 2008) Product Brief v1.1	Table 1-2 • ProASIC3E FPGAs Package Sizes Dimensions is new.	1-II
Revision 7 (Jun 2008) DC and Switching Characteristics v1.2	The title of Table 2-4 • Overshoot and Undershoot Limits [1] was modified to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted.	2-3
	Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels was updated.	2-50
Revision 6 (Jun 2008)	The A3PE600 "FG484" table was missing G22. The pin and its function were added to the table.	4-27
Revision 5 (Jun 2008) Packaging v1.4	The naming conventions changed for the following pins in the "FG484" for the A3PE600: **Pin Number** — **New Function Name** J19 — IO45PPB2V1 K20 — IO45NPB2V1 M2 — IO114NPB6V1 N1 — IO114PPB6V1 N4 — GFC2/IO115PPB6V1 P3 — IO115NPB6V1	4-22
Revision 4 (Apr 2008) Product Brief v1.0	The product brief portion of the datasheet was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.	N/A
Packaging v1.3	The "FG324" package diagram was replaced.	4-12

Revision	Changes	Page
Revision 3 (Apr 2008) Packaging v1.2	The following pins had duplicates and the extra pins were deleted from the "PQ208" A3PE3000 table: 36, 62, 171 Note: There were no pin function changes in this update.	4-2
	The following pins had duplicates and the extra pins were deleted from the "FG324" table: E2, E3, E16, E17, P2, P3, T16, U17 Note: There were no pin function changes in this update.	4-12
	The "FG256" pin table was updated for the A3PE600 device because the old PAT were based on the IFX die, and this is the final UMC die version.	4-9
	The "FG484" was updated for the A3PE600 device because the old PAT were based on the IFX die, and this is the final UMC die version.	4-22
	The following pins had duplicates and the extra pins were deleted from the "FG896" table: AD6, AE5, AE28, AF29, F5, F26, G6, G25 Note: There were no pin function changes in this update.	4-41
Revision 2 (Mar 2008) Product Brief rev. 1	The FG324 package was added to the "ProASIC3E Product Family" table, the "I/Os Per Package1" table, and the "Temperature Grade Offerings" table for A3PE3000.	I, II, IV
Revision 1 (Feb 2008) DC and Switching Characteristics v1.1	In Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature 1, Maximum Operating Junction Temperature was changed from 110°C to 100°C for both commercial and industrial grades.	2
	The "PLL Behavior at Brownout Condition" section is new.	2-4
	In the "PLL Contribution—PPLL" section, the following was deleted: FCLKIN is the input clock frequency.	2-10
	In Table 2-14 • Summary of Maximum and Minimum DC Input Levels, the note was incorrect. It previously said T_J and it was corrected and changed to T_A.	2-17
	In Table 2-98 • ProASIC3E CCC/PLL Specification, the SCLK parameter and note 1 are new.	2-70
	Table 2-103 • JTAG 1532 was populated with the parameter data, which was not in the previous version of the document.	2-83
Revision 1 (cont'd) Packaging v1.1	The "PQ208" pin table for A3PE3000 was updated.	4-2
	The "FG324" pin table for A3PE3000 is new.	4-13
	The "FG484" pin table for A3PE3000 is new.	4-17
	The "FG896" pin table for A3PE3000 is new.	4-41
Revision 0 (Jan 2008)	This document was previously in datasheet v2.1. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is 51700098-001-0.	N/A
v2.1 (July 2007)	CoreMP7 information was removed from the "Features and Benefits" section.	1-I
	The M1 device part numbers have been updated in ProASIC3E Product Family, "Packaging Tables", "Temperature Grade Offerings", "Speed Grade and Temperature Grade Matrix", and "Speed Grade and Temperature Grade Matrix".	1-I

Revision	Changes	Page
v2.1 (continued)	The words "ambient temperature" were added to the temperature range in the "Temperature Grade Offerings", "Speed Grade and Temperature Grade Matrix", and "Speed Grade and Temperature Grade Matrix" sections.	1-I
	The "Clock Conditioning Circuit (CCC) and PLL" section was updated.	1-I
	The caption "Main (chip)" in Figure 2-9 • Overview of Automotive ProASIC3 VersaNet Global Network was changed to "Chip (main)."	2-9
	The T_J parameter in Table 3-2 • Recommended Operating Conditions was changed to T_A, ambient temperature, and table notes 4–6 were added.	3-2
	The "PLL Macro" section was updated to add information on the VCO and PLL outputs during power-up.	2-15
v2.0 (April 2007)	In the "Temperature Grade Offerings" section, Ambient was deleted.	iii
	Ambient was deleted from "Temperature Grade Offerings".	iii
	Ambient was deleted from the "Speed Grade and Temperature Grade Matrix".	iv
	The "PLL Macro" section was updated to include power-up information.	2-15
	Table 2-13 • ProASIC3E CCC/PLL Specification was updated.	2-30
	Figure 2-19 • Peak-to-Peak Jitter Definition is new.	2-18
	The "SRAM and FIFO" section was updated with operation and timing requirement information.	2-21
	The "RESET" section was updated with read and write information.	2-25
	The "RESET" section was updated with read and write information.	2-25
	The "Introduction" in the "Advanced I/Os" section was updated to include information on input and output buffers being disabled.	2-28
	In the Table 2-15 • Levels of Hot-Swap Support, the ProASIC3 compliance descriptions were updated for levels 3 and 4.	2-34
	Table 2-45 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3E Devices was updated.	2-64
	Notes 3, 4, and 5 were added to Table 2-17 • Comparison Table for 5 V–Compliant Receiver Scheme. 5 x 52.72 was changed to 52.7 and the Maximum current was updated from 4 x 52.7 to 5 x 52.7.	2-40
	The "VCCPLF PLL Supply Voltage" section was updated.	2-50
	The "VPUMP Programming Supply Voltage" section was updated.	2-50
	The "GL Globals" section was updated to include information about direct input into quadrant clocks.	2-51
	VJTAG was deleted from the "TCK Test Clock" section.	2-51
	In Table 2-22 • Recommended Tie-Off Values for the TCK and TRST Pins, TSK was changed to TCK in note 2. Note 3 was also updated.	2-51
	Ambient was deleted from Table 3-2 • Recommended Operating Conditions. VPUMP programming mode was changed from "3.0 to 3.6" to "3.15 to 3.45".	3-2
	Note 3 is new in Table 3-4 • Overshoot and Undershoot Limits (as measured on quiet I/Os).	3-2
	In EQ 3-2, 150 was changed to 110 and the result changed to 5.88.	3-5

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51700098-15/06.15