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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	
Total RAM Bits	276480
Number of I/O	147
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3pe1500-1pq208

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	VMV (V)	Static Power PDC2 (mW) ¹	Dynamic Power PAC9 (µW/MHz) ²
HSTL (I)	1.5	0.17	2.03
HSTL (II)	1.5	0.17	2.03
SSTL2 (I)	2.5	1.38	4.48
SSTL2 (II)	2.5	1.38	4.48
SSTL3 (I)	3.3	3.21	9.26
SSTL3 (II)	3.3	3.21	9.26
Differential			-
LVDS/B-LVDS/M-LVDS	2.5	2.26	1.50
LVPECL	3.3	5.71	2.17

Table 2-8 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings (continued)

Notes:

1. PDC2 is the static power (where applicable) measured on VMV.

2. PAC9 is the total dynamic power measured on VCC and VMV.

3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.

Table 2-9 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings ¹

	C _{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW) ²	Dynamic Power PAC10 (µW/MHz) ³
Single-Ended			•	•
3.3 V LVTTL/LVCMOS	35	3.3	-	474.70
3.3 V LVTTL/LVCMOS Wide Range ⁴	35	3.3	-	474.70
2.5 V LVCMOS	35	2.5	-	270.73
1.8 V LVCMOS	35	1.8	-	151.78
1.5 V LVCMOS (JESD8-11)	35	1.5	-	104.55
3.3 V PCI	10	3.3	-	204.61
3.3 V PCI-X	10	3.3	-	204.61
Voltage-Referenced				
3.3 V GTL	10	3.3	-	24.08
2.5 V GTL	10	2.5	-	13.52
3.3 V GTL+	10	3.3	-	24.10
2.5 V GTL+	10	2.5	-	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.22
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.60

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.

2. PDC3 is the static power (where applicable) measured on VCCI.

3. PAC10 is the total dynamic power measured on VCC and VCCI.

4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.



Figure 2-4 • Output Buffer Model and Delays (example)

Summary of I/O Timing Characteristics – Default I/O Software Settings

Standard	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_REF)	Measuring Trip Point (Vtrip)
3.3 V LVTTL / 3.3 V LVCMOS	-	_	1.4 V
3.3 V LVCMOS Wide Range	-	-	1.4 V
2.5 V LVCMOS	-	-	1.2 V
1.8 V LVCMOS	-	-	0.90 V
1.5 V LVCMOS	-	-	0.75 V
3.3 V PCI	-	-	0.285 * VCCI (RR) 0.615 * VCCI (FF))
3.3 V PCI-X	_	-	0.285 * VCCI (RR) 0.615 * VCCI (FF)
3.3 V GTL	0.8 V	1.2 V	VREF
2.5 V GTL	0.8 V	1.2 V	VREF
3.3 V GTL+	1.0 V	1.5 V	VREF
2.5 V GTL+	1.0 V	1.5 V	VREF
HSTL (I)	0.75 V	0.75 V	VREF
HSTL (II)	0.75 V	0.75 V	VREF
SSTL2 (I)	1.25 V	1.25 V	VREF
SSTL2 (II)	1.25 V	1.25 V	VREF
SSTL3 (I)	1.5 V	1.485 V	VREF
SSTL3 (II)	1.5 V	1.485 V	VREF
LVDS	_	-	Cross point
LVPECL	_	_	Cross point

Table 2-15 • Summary of AC Measuring Points

Table 2-16 • I/O AC Parameter Definitions

Parameter	Definition
t _{DP}	Data to Pad delay through the Output Buffer
t _{PY}	Pad to Data delay through the Input Buffer with Schmitt trigger disabled
t _{DOUT}	Data to Output Buffer delay through the I/O interface
t _{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t _{DIN}	Input Buffer to Data delay through the I/O interface
t _{PYS}	Pad to Data delay through the Input Buffer with Schmitt trigger enabled
t _{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t _{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t _{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t _{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t _{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t _{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

3.3 V LVCMOS Wide Range

3.3 V LVCMOS Wide Range	Equivalent Software Default Drive	v	IL	v	Ŧ	VOL	VOH	IOL	юн	IOSL	IOSH	IIL ²	IIH ³
Drive Strength	Strength Option ¹	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	μA	μA	Max. mA ⁴	Max. mA ⁴	μA ⁵	μA ⁵
100 µA	2 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	27	25	10	10
100 µA	4 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	27	25	10	10
100 µA	6 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	54	51	10	10
100 µA	8 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	54	51	10	10
100 µA	12 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	109	103	10	10
100 µA	16 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	127	132	10	10
100 µA	24 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	181	268	10	10

Table 2-29 • Minimum and Maximum DC Input and Output Levels

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

3. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN< VCCI. Input current is larger when operating outside recommended ranges.

4. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

5. Currents are measured at 85°C junction temperature.

6. Software default selection highlighted in gray.



Figure 2-7 • AC Loading

Table 2-30 • 3.3 V LVCMOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	3.3	1.4	_	35

Note: **Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

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ProASIC3E DC and Switching Characteristics

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
4 mA	Std.	0.66	12.00	0.04	1.51	1.66	0.43	12.23	11.61	2.72	2.20	14.46	13.85	ns
	–1	0.56	10.21	0.04	1.29	1.41	0.36	10.40	9.88	2.31	1.87	12.30	11.78	ns
	-2	0.49	8.96	0.03	1.13	1.24	0.32	9.13	8.67	2.03	1.64	10.80	10.34	ns
8 mA	Std.	0.66	8.73	0.04	1.51	1.66	0.43	8.89	8.01	3.10	2.93	11.13	10.25	ns
	–1	0.56	7.43	0.04	1.29	1.41	0.36	7.57	6.82	2.64	2.49	9.47	8.72	ns
	-2	0.49	6.52	0.03	1.13	1.24	0.32	6.64	5.98	2.32	2.19	8.31	7.65	ns
12 mA	Std.	0.66	6.77	0.04	1.51	1.66	0.43	6.90	6.11	3.37	3.39	9.14	8.34	ns
	–1	0.56	5.76	0.04	1.29	1.41	0.36	5.87	5.20	2.86	2.89	7.77	7.10	ns
	-2	0.49	5.06	0.03	1.13	1.24	0.32	5.15	4.56	2.51	2.53	6.82	6.23	ns
16 mA	Std.	0.66	6.31	0.04	1.51	1.66	0.43	6.42	5.73	3.42	3.52	8.66	7.96	ns
	–1	0.56	5.37	0.04	1.29	1.41	0.36	5.46	4.87	2.91	3.00	7.37	6.77	ns
	-2	0.49	4.71	0.03	1.13	1.24	0.32	4.80	4.28	2.56	2.63	6.47	5.95	ns
24 mA	Std.	0.66	5.93	0.04	1.51	1.66	0.43	6.04	5.70	3.49	4.00	8.28	7.94	ns
	-1	0.56	5.05	0.04	1.29	1.41	0.36	5.14	4.85	2.97	3.40	7.04	6.75	ns
	-2	0.49	4.43	0.03	1.13	1.24	0.32	4.51	4.26	2.61	2.99	6.18	5.93	ns

Table 2-36 • 2.5 V LVCMOS Low Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Timing Characteristics

Table 2-43 • 1.5 V LVCMOS High Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
2 mA	Std.	0.66	8.53	0.04	1.70	2.14	0.43	7.26	8.53	3.39	2.79	9.50	10.77	ns
	-1	0.56	7.26	0.04	1.44	1.82	0.36	6.18	7.26	2.89	2.37	8.08	9.16	ns
	-2	0.49	6.37	0.03	1.27	1.60	0.32	5.42	6.37	2.53	2.08	7.09	8.04	ns
4 mA	Std.	0.66	5.41	0.04	1.70	2.14	0.43	5.22	5.41	3.75	3.48	7.45	7.65	ns
	-1	0.56	4.60	0.04	1.44	1.82	0.36	4.44	4.60	3.19	2.96	6.34	6.50	ns
	-2	0.49	4.04	0.03	1.27	1.60	0.32	3.89	4.04	2.80	2.60	5.56	5.71	ns
6 mA	Std.	0.66	4.80	0.04	1.70	2.14	0.43	4.89	4.75	3.83	3.67	7.13	6.98	ns
	-1	0.56	4.09	0.04	1.44	1.82	0.36	4.16	4.04	3.26	3.12	6.06	5.94	ns
	-2	0.49	3.59	0.03	1.27	1.60	0.32	3.65	3.54	2.86	2.74	5.32	5.21	ns
8 mA	Std.	0.66	4.42	0.04	1.70	2.14	0.43	4.50	3.62	3.96	4.37	6.74	5.86	ns
	-1	0.56	3.76	0.04	1.44	1.82	0.36	3.83	3.08	3.37	3.72	5.73	4.98	ns
	-2	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns
12 mA	Std.	0.66	4.42	0.04	1.70	2.14	0.43	4.50	3.62	3.96	4.37	6.74	5.86	ns
	-1	0.56	3.76	0.04	1.44	1.82	0.36	3.83	3.08	3.37	3.72	5.73	4.98	ns
	-2	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{zLS}	t _{zHS}	Units
2 mA	Std.	0.66	14.11	0.04	1.70	2.14	0.43	14.37	13.14	3.40	2.68	16.61	15.37	ns
	-1	0.56	12.00	0.04	1.44	1.82	0.36	12.22	11.17	2.90	2.28	14.13	13.08	ns
	-2	0.49	10.54	0.03	1.27	1.60	0.32	10.73	9.81	2.54	2.00	12.40	11.48	ns
4 mA	Std.	0.66	11.23	0.04	1.70	2.14	0.43	11.44	9.87	3.77	3.36	13.68	12.10	ns
	-1	0.56	9.55	0.04	1.44	1.82	0.36	9.73	8.39	3.21	2.86	11.63	10.29	ns
	-2	0.49	8.39	0.03	1.27	1.60	0.32	8.54	7.37	2.81	2.51	10.21	9.04	ns
6 mA	Std.	0.66	10.45	0.04	1.70	2.14	0.43	10.65	9.24	3.84	3.55	12.88	11.48	ns
	-1	0.56	8.89	0.04	1.44	1.82	0.36	9.06	7.86	3.27	3.02	10.96	9.76	ns
	-2	0.49	7.81	0.03	1.27	1.60	0.32	7.95	6.90	2.87	2.65	9.62	8.57	ns
8 mA	Std.	0.66	10.02	0.04	1.70	2.14	0.43	10.20	9.23	3.97	4.22	12.44	11.47	ns
	-1	0.56	8.52	0.04	1.44	1.82	0.36	8.68	7.85	3.38	3.59	10.58	9.75	ns
	-2	0.49	7.48	0.03	1.27	1.60	0.32	7.62	6.89	2.97	3.15	9.29	8.56	ns
12 mA	Std.	0.66	10.02	0.04	1.70	2.14	0.43	10.20	9.23	3.97	4.22	12.44	11.47	ns
	-1	0.56	8.52	0.04	1.44	1.82	0.36	8.68	7.85	3.38	3.59	10.58	9.75	ns
	-2	0.49	7.48	0.03	1.27	1.60	0.32	7.62	6.89	2.97	3.15	9.29	8.56	ns

Table 2-44 • 1.5 V LVCMOS Low Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-66 • Minimum and Maximum	DC Input and Output Levels
----------------------------------	----------------------------

SSTL2 Class I	i VIL				VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Min. Max. V V		Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA²	μA²
15 mA	-0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15	87	83	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

2. Currents are measured at 85°C junction temperature.



Figure 2-18 • AC Loading

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-68 • SSTL 2 Class I

```
Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 2.3 V, VREF = 1.25 V
```

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{zLS}	t _{zHS}	Units
Std.	0.66	2.13	0.04	1.33	0.43	2.17	1.85			4.40	4.08	ns
–1	0.56	1.81	0.04	1.14	0.36	1.84	1.57			3.74	3.47	ns
-2	0.49	1.59	0.03	1.00	0.32	1.62	1.38			3.29	3.05	ns

I/O Register Specifications



Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Figure 2-25 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Input Register





Timing Characteristics

Table 2-86 • Input Data Register Propagation DelaysCommercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.27	0.32	ns
t _{ISUD}	Data Setup Time for the Input Data Register	0.26	0.30	0.35	ns
t _{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t _{ISUE}	Enable Setup Time for the Input Data Register	0.37	0.42	0.50	ns
t _{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t _{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.45	0.52	0.61	ns
t _{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.45	0.52	0.61	ns
t _{IREMCLR}	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	0.00	ns
t _{IRECCLR}	Asynchronous Clear Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
t _{IREMPRE}	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	0.00	ns
t _{IRECPRE}	Asynchronous Preset Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
t _{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
t _{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
t _{ICKMPWH}	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.41	0.48	ns
t _{ICKMPWL}	Clock Minimum Pulse Width Low for the Input Data Register	0.32	0.37	0.43	ns





Figure 2-29 • Output Enable Register Timing Diagram

Timing Characteristics

Table 2-88 • Output Enable Register Propagation DelaysCommercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{OECLKQ}	Clock-to-Q of the Output Enable Register	0.59	0.67	0.79	ns
t _{OESUD}	Data Setup Time for the Output Enable Register	0.31	0.36	0.42	ns
t _{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	0.00	ns
t _{OESUE}	Enable Setup Time for the Output Enable Register	0.44	0.50	0.58	ns
t _{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	0.00	ns
t _{OECLR2Q}	Asynchronous Clear-to-Q of the Output Enable Register	0.67	0.76	0.89	ns
t _{OEPRE2Q}	Asynchronous Preset-to-Q of the Output Enable Register	0.67	0.76	0.89	ns
t _{OEREMCLR}	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
t _{OERECCLR}	Asynchronous Clear Recovery Time for the Output Enable Register	0.22	0.25	0.30	ns
t _{OEREMPRE}	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
t _{OERECPRE}	Asynchronous Preset Recovery Time for the Output Enable Register	0.22	0.25	0.30	ns
t _{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
t _{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
t _{OECKMPWH}	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.41	0.48	ns
t _{OECKMPWL}	Clock Minimum Pulse Width Low for the Output Enable Register	0.32	0.37	0.43	ns

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3E library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion*, *IGLOO®/e*, *and ProASIC3/E Macro Library Guide*.



Figure 2-34 • Sample of Combinatorial Cells

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ProASIC3E DC and Switching Characteristics

Timing Characteristics

Table 2-93 • Combinatorial Cell Propagation Delays Commercial-Case Conditions: T₁ = 70°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	-2	-1	Std.	Units
INV	Y = !A	t _{PD}	0.40	0.46	0.54	ns
AND2	$Y = A \cdot B$	t _{PD}	0.47	0.54	0.63	ns
NAND2	Y = !(A · B)	t _{PD}	0.47	0.54	0.63	ns
OR2	Y = A + B	t _{PD}	0.49	0.55	0.65	ns
NOR2	Y = !(A + B)	t _{PD}	0.49	0.55	0.65	ns
XOR2	Y = A ⊕ B	t _{PD}	0.74	0.84	0.99	ns
MAJ3	Y = MAJ(A, B, C)	t _{PD}	0.70	0.79	0.93	ns
XOR3	$Y = A \oplus B \oplus C$	t _{PD}	0.87	1.00	1.17	ns
MUX2	Y = A !S + B S	t _{PD}	0.51	0.58	0.68	ns
AND3	$Y = A \cdot B \cdot C$	t _{PD}	0.56	0.64	0.75	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

VersaTile Specifications as a Sequential Module

The ProASIC3E library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.



Figure 2-36 • Sample of Sequential Cells



ProASIC3E DC and Switching Characteristics

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-98 • ProASIC3E CCC/PLL Specification

Parameter	Minimum	Typical	Maximum	Units
Clock Conditioning Circuitry Input Frequency fIN_CCC	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f _{OUT_CCC}	0.75		350	MHz
Delay Increments in Programmable Delay Blocks ^{1, 2}		160 ³		ps
Serial Clock (SCLK) for Dynamic PLL ⁴			125	MHz
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
CCC Output Peak-to-Peak Period Jitter F _{CCC_OUT}	Ma	x Peak-to-Pe	ak Period Jitter	
	1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%		0.70%	
24 MHz to 100 MHz	1.00%		1.20%	
100 MHz to 250 MHz	1.75%		2.00%	
250 MHz to 350 MHz	2.50%		5.60%	
Acquisition Time LockControl = 0			300	μs
LockControl = 1			6.0	ms
Tracking Jitter ⁵ LockControl = 0			1.6	ns
LockControl = 1			0.8	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 ^{1, 2}	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2 ^{1,2}	0.025		5.56	ns
Delay Range in Block: Fixed Delay ^{1,4}		2.2		ns

Notes:

1. This delay is a function of voltage and temperature. See Table 2-6 on page 2-5 for deratings

2. $T_J = 25^{\circ}C$, VCC = 1.5 V.

3. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help for more information.

4. Maximum value obtained for a -2 speed-grade device in worst-case commercial conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

5. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.

Wicrosemi. ProASIC3E DC and Switching Characteristics







Figure 2-44 • RAM Write, Output as Write Data. Applicable to RAM4K9 Only.



Figure 2-45 • RAM Reset. Applicable to Both RAM4K9 and RAM512x18.

Refer to the I/O Structure section of the *ProASIC3E FPGA Fabric User's Guide* for an explanation of the naming of global pins.

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pullup/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 W to 1 k Ω will satisfy the requirements. Refer to Table 3-1 for more information.

VJTAG	Tie-Off Resistance
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Table 3-1 • Recommended Tie-Off Values for the TCK and TRST Pins

Notes:

- 1. Equivalent parallel resistance if more than one device is on the JTAG chain
- 2. The TCK pin can be pulled up/down.
- 3. The TRST pin is pulled down.

TDI

TMS

Test Data Input

Test Data Output

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-1 and must satisfy the parallel resistance value requirement. The values in Table 3-1 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements.

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Package Pin Assignments

FG484					
Pin Number	A3PE1500 Function				
V15	IO112NDB4V0				
V16	GDB2/IO112PDB4V0				
V17	TDI				
V18	GNDQ				
V19	TDO				
V20	GND				
V21	NC				
V22	IO105NDB3V2				
W1	NC				
W2	NC				
W3	NC				
W4	GND				
W5	IO165NDB5V3				
W6	GEB2/IO165PDB5V3				
W7	IO164NDB5V3				
W8	IO153NDB5V2				
W9	IO153PDB5V2				
W10	IO147NDB5V1				
W11	IO133NDB4V2				
W12	IO130NDB4V2				
W13	IO130PDB4V2				
W14	IO113NDB4V0				
W15	GDC2/IO113PDB4V0				
W16	IO111NDB4V0				
W17	GDA2/IO111PDB4V0				
W18	TMS				
W19	GND				
W20	NC				
W21	NC				
W22	NC				
Y1	VCCIB6				
Y2	NC				
Y3	NC				
Y4	IO161NDB5V3				
Y5	GND				
Y6	IO163NDB5V3				

FG484					
Pin Number	A3PE1500 Function				
Y7	IO163PDB5V3				
Y8	VCC				
Y9	VCC				
Y10	IO147PDB5V1				
Y11	IO133PDB4V2				
Y12	IO131NPB4V2				
Y13	NC				
Y14	VCC				
Y15	VCC				
Y16	NC				
Y17	NC				
Y18	GND				
Y19	NC				
Y20	NC				
Y21	NC				
Y22	VCCIB3				



Revision	Changes					
Revision 9 (Aug 2009)	All references to speed grade	-F have been removed from this document.	N/A			
Product Brief v1.2						
	The "Pro I/Os with Advance definitions of hot-swap and co	ed I/O Standards" section was revised to add Id-sparing.	1-6			
DC and Switching Characteristics v1.3	3.3 V LVCMOS and 1.2 V L datasheet. This affects all ta LVCMOS data.	VCMOS Wide Range support was added to the ables that contained 3.3 V LVCMOS and 1.2 V	N/A			
	IIL and IIH input leakage cur Maximum DC Input and Outpu	rrent information was added to all "Minimum and it Levels" tables.	N/A			
	–F was removed from the data	asheet. The speed grade is no longer supported.	N/A			
	In the Table 2-2 • Recomme voltage" and note 4 are new.	In the Table 2-2 • Recommended Operating Conditions ¹ "3.0 V DC supply voltage" and note 4 are new.				
	The Table 2-4 • Overshoot and	The Table 2-4 • Overshoot and Undershoot Limits ¹ table was updated.				
	The Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays table was updated.					
	There are new parameters and data was updated in the Table 2-99 • RAM4K9 table.					
	There are new parameters and data was updated in the Table 2-100 • RAM512X18 table.					
Revision 8 (Feb 2008)	Table 1-2 • ProASIC3E FPGAs Package Sizes Dimensions is new.					
Product Brief v1.1						
Revision 7 (Jun 2008)	The title of Table 2-4 • Over remove "as measured on que	shoot and Undershoot Limits ¹ was modified to uiet I/Os." Table note 2 was revised to remove	2-3			
Characteristics v1.2	"estimated SSO density over o	cycles." Table note 3 was deleted.				
	Table 2-78 • LVDS Minimum updated.	and Maximum DC Input and Output Levels was	2-50			
Revision 6 (Jun 2008)	The A3PE600 "FG484" table added to the table.	was missing G22. The pin and its function were	4-27			
Revision 5 (Jun 2008) Packaging v1 4	The naming conventions char A3PE600:	nged for the following pins in the "FG484" for the	4-22			
	Pin Number	New Function Name				
	J19	IO45PPB2V1				
	K20	IO45NPB2V1				
	M2	IO114NPB6V1				
	N1	IO114PPB6V1				
	N4	GFC2/IO115PPB6V1				
	P3	IO115NPB6V1				
Revision 4 (Apr 2008) Product Brief v1.0	The product brief portion of the a version number, starting at features, benefits, ordering offerings. The second section	e datasheet was divided into two sections and given v1.0. The first section of the document includes information, and temperature and speed grade is a device family overview.	N/A			
Packaging v1.3	The "FG324" package diagram was replaced.					



Revision	Changes			
Advance v0.3	The "Methodology" section was updated.			
(continuea)	The A3PE3000 "208-Pin PQFP" pin table was updated.	4-6		



Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "ProASIC3E Device Status" table on page II, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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