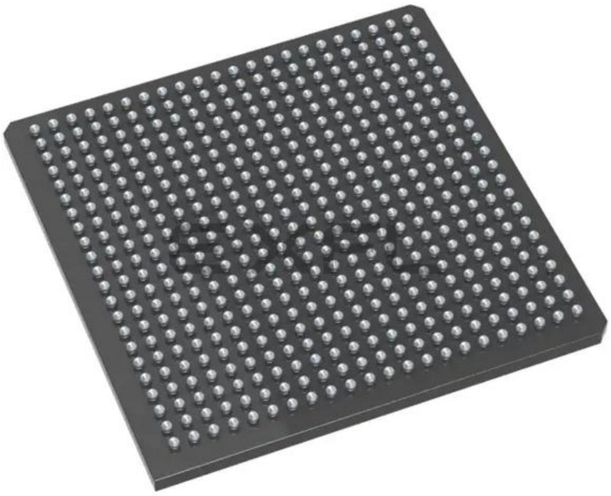
Microchip Technology - A3PE1500-2FG484 Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	280
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3pe1500-2fg484

Advanced Architecture

The proprietary ProASIC3E architecture provides granularity comparable to standard-cell ASICs. The ProASIC3E device consists of five distinct and programmable architectural features (Figure 1-1 on page 3):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- Pro I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the ProASIC3E core tile as either a three-input lookup table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC family of third-generation architecture Flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

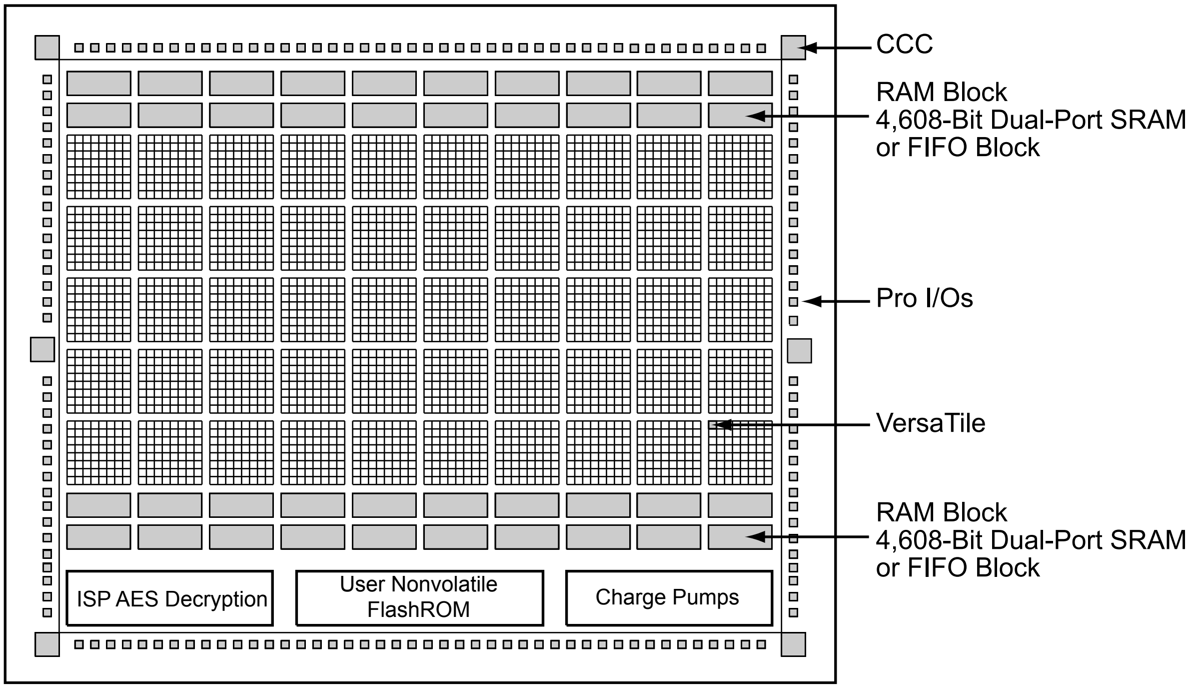


Figure 1-1 • **ProASIC3E Device Architecture Overview**

SRAM and FIFO

ProASIC3E devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

ProASIC3E devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC3E family contains six CCCs, each with an integrated PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

To maximize user I/Os, only the center east and west PLLs are available in devices using the PQ208 package. However, all six CCC blocks are still usable; the four corner CCCs allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from –7.56 ns to +11.12 ns
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration.
- Output duty cycle = 50% ± 1.5% or better
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used
- Maximum acquisition time = 300 µs
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter— allowable input jitter is up to 1.5 ns
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × (350 MHz / f_{OUT_CCC})

Global Clocking

ProASIC3E devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high fanout nets.

Thermal Characteristics

Introduction

The temperature variable in Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 1

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 110°C. EQ 2 shows a sample calculation of the absolute maximum power dissipation allowed for an 896-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{110\text{°C} - 70\text{°C}}{13.6\text{°C/W}} = 5.88\text{ W}$$

EQ 2

Table 2-5 • **Package Thermal Resistivities**

Package Type	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	200 ft./min.	500 ft./min.	
Plastic Quad Flat Package (PQFP)	208	8.0	26.1	22.5	20.8	C/W
Plastic Quad Flat Package (PQFP) with embedded heat spreader in A3PE3000	208	3.8	16.2	13.3	11.9	C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.9	22.8	21.5	C/W
	484	3.2	20.5	17.0	15.9	C/W
	676	3.2	16.4	13.0	12.0	C/W
	896	2.4	13.6	10.4	9.4	C/W

Temperature and Voltage Derating Factors

Table 2-6 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, VCC = 1.425 V)**

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.87	0.92	0.95	1.00	1.02	1.04
1.500	0.83	0.88	0.90	0.95	0.97	0.98
1.575	0.80	0.85	0.87	0.92	0.93	0.95

Calculating Power Dissipation

Quiescent Supply Current

Table 2-7 • **Quiescent Supply Current Characteristics**

	A3PE600	A3PE1500	A3PE3000
Typical (25°C)	5 mA	12 mA	25 mA
Maximum (Commercial)	30 mA	70 mA	150 mA
Maximum (Industrial)	45 mA	105 mA	225 mA

Notes:

1. *IDD Includes VCC, VPUMP, VCCI, and VMV currents. Values do not include I/O static contribution, which is shown in Table 2-8 and Table 2-9 on page 2-7.*
2. *–F speed grade devices may experience higher standby IDD of up to five times the standard IDD and higher I/O leakage.*

Power per I/O Pin

Table 2-8 • **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings**

	VMV (V)	Static Power PDC2 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	–	17.39
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	–	25.51
3.3 V LVTTL/LVCMOS Wide Range[3]	3.3	–	16.34
3.3 V LVTTL/LVCMOS Wide Range – Schmitt trigger[3]	3.3	–	24.49
2.5 V LVCMOS	2.5	–	5.76
2.5 V LVCMOS – Schmitt trigger	2.5	–	7.16
1.8 V LVCMOS	1.8	–	2.72
1.8 V LVCMOS – Schmitt trigger	1.8	–	2.80
1.5 V LVCMOS (JESD8-11)	1.5	–	2.08
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	2.00
3.3 V PCI	3.3	–	18.82
3.3 V PCI – Schmitt trigger	3.3	–	20.12
3.3 V PCI-X	3.3	–	18.82
3.3 V PCI-X – Schmitt trigger	3.3	–	20.12
Voltage-Referenced			
3.3 V GTL	3.3	2.90	8.23
2.5 V GTL	2.5	2.13	4.78
3.3 V GTL+	3.3	2.81	4.14
2.5 V GTL+	2.5	2.57	3.71

Notes:

1. *PDC2 is the static power (where applicable) measured on VMV.*
2. *PAC9 is the total dynamic power measured on VCC and VMV.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.*

User I/O Characteristics

Timing Model

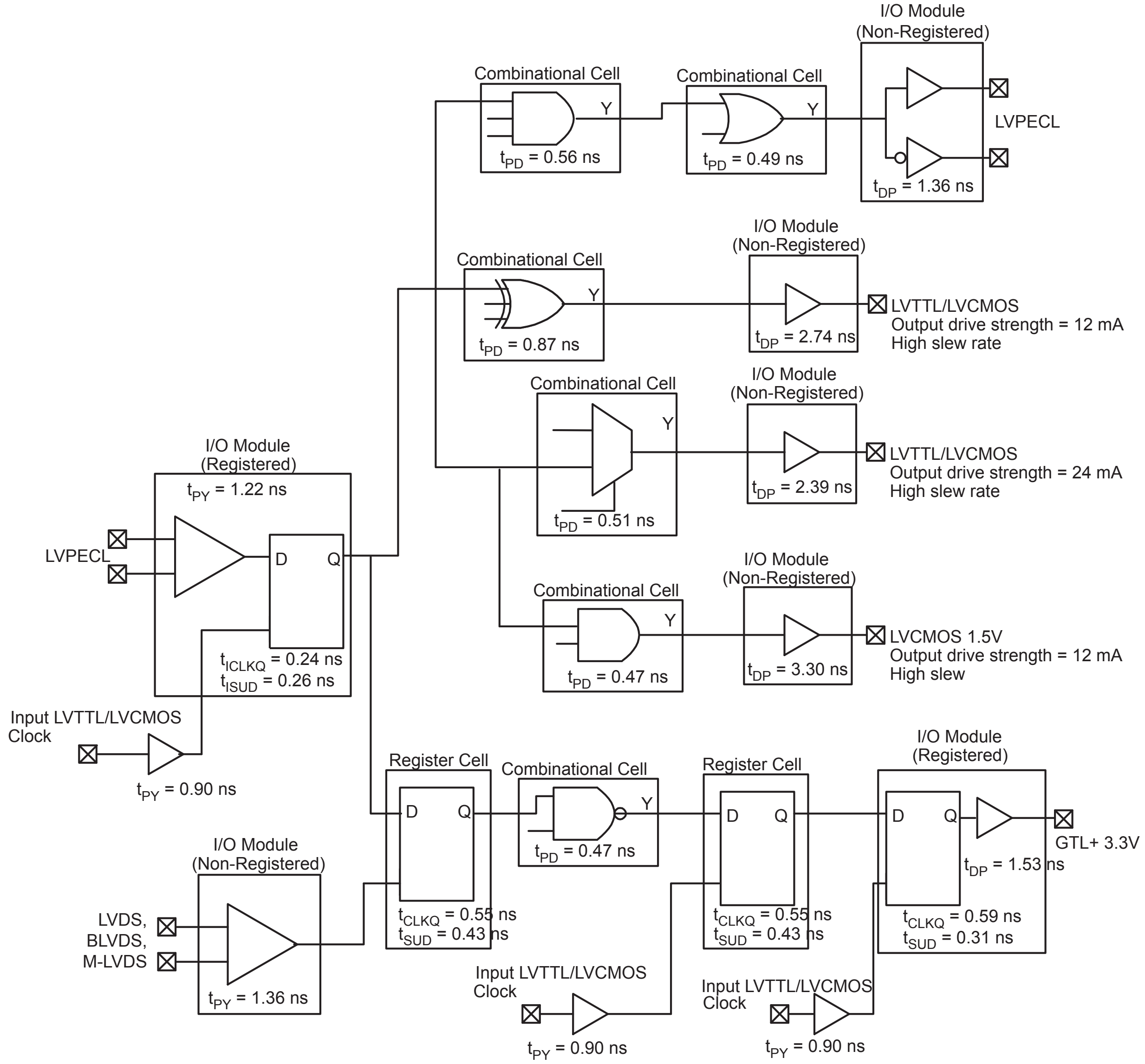


Figure 2-2 • **Timing Model**
Operating Conditions: –2 Speed, Commercial Temperature Range (T_J = 70°C), Worst-Case VCC = 1.425 V

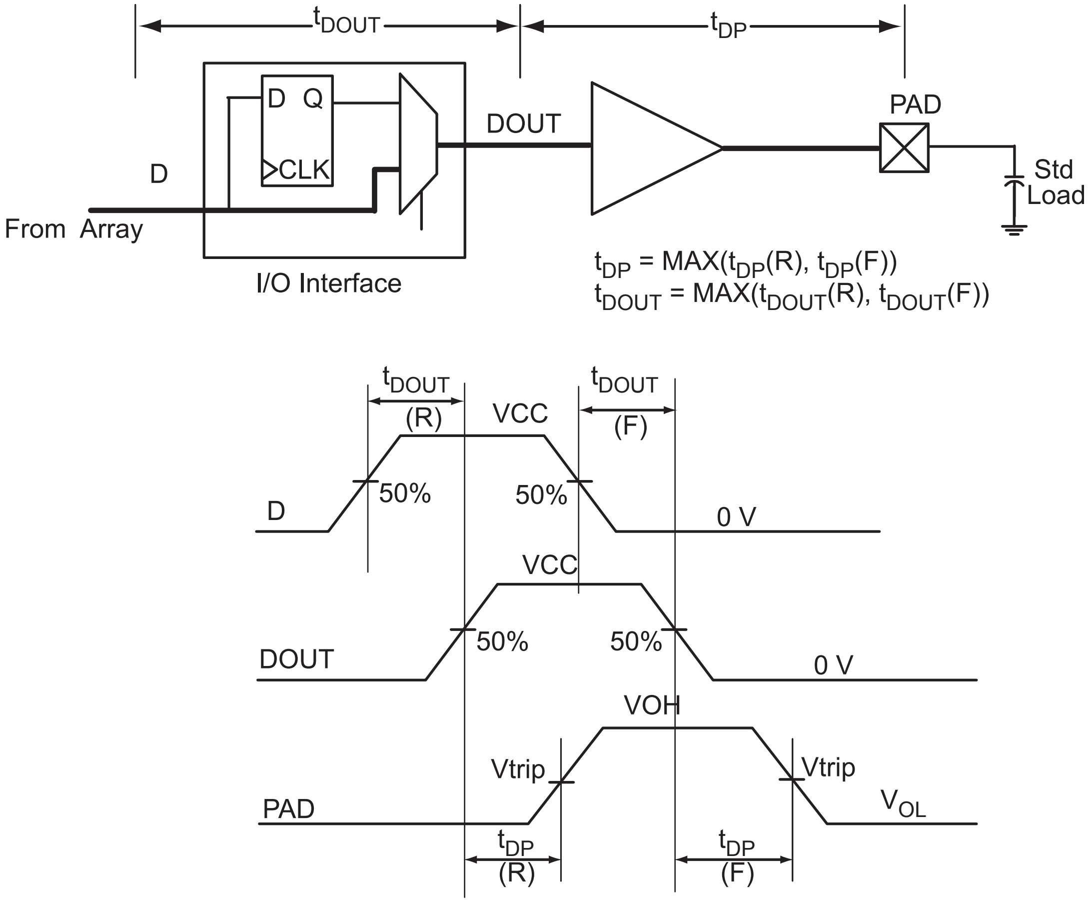


Figure 2-4 • **Output Buffer Model and Delays (example)**

Table 2-17 • **Summary of I/O Timing Characteristics—Software Default Settings**
–2 Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option)[1]	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)
3.3 V LVTTL / 3.3 V LVCMOS	12	12	High	35	–	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81
3.3 V LVCMOS Wide Range[2]	100 µA	12	High	35	–	0.49	4.24	0.03	1.36	1.78	0.32	4.24	3.25	3.78	4.17	6.77	5.79
2.5 V LVCMOS	12	12	High	35	–	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28
1.8 V LVCMOS	12	12	High	35	–	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98
1.5 V LVCMOS	12	12	High	35	–	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37
3.3 V PCI	Per PCI spec	–	High	10	25 [3]	0.49	2.09	0.03	0.78	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16
3.3 V PCI-X	Per PCI-X spec	–	High	10	25[3]	0.49	2.09	0.03	0.78	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16
3.3 V GTL	20 [4]	–	High	10	25	0.45	1.55	0.03	2.19	–	0.32	1.52	1.55	–	–	3.19	3.22
2.5 V GTL	20 [4]	–	High	10	25	0.45	1.59	0.03	1.83	–	0.32	1.61	1.59	–	–	3.28	3.26
3.3 V GTL+	35	–	High	10	25	0.45	1.53	0.03	1.19	–	0.32	1.56	1.53	–	–	3.23	3.20
2.5 V GTL+	33	–	High	10	25	0.45	1.65	0.03	1.13	–	0.32	1.68	1.57	–	–	3.35	3.24
HSTL (I)	8	–	High	20	50	0.49	2.37	0.03	1.59	–	0.32	2.42	2.35	–	–	4.09	4.02
HSTL (II)	15 [4]	–	High	20	25	0.49	2.26	0.03	1.59	–	0.32	2.30	2.03	–	–	3.97	3.70
SSTL2 (I)	15	–	High	30	50	0.49	1.59	0.03	1.00	–	0.32	1.62	1.38	–	–	3.29	3.05
SSTL2 (II)	18	–	High	30	25	0.49	1.62	0.03	1.00	–	0.32	1.65	1.32	–	–	3.32	2.99
SSTL3 (I)	14	–	High	30	50	0.49	1.72	0.03	0.93	–	0.32	1.75	1.37	–	–	3.42	3.04
SSTL3 (II)	21	–	High	30	25	0.49	1.54	0.03	0.93	–	0.32	1.57	1.25	–	–	3.24	2.92
LVDS/B-LVDS/ M-LVDS	24	–	High	–	–	0.49	1.40	0.03	1.36	–	–	–	–	–	–	–	–
LVPECL	24	–	High	–	–	0.49	1.36	0.03	1.22	–	–	–	–	–	–	–	–

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3V wide range as specified in the JESD8b specification.*
3. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-38 for connectivity. This resistor is not required during normal operation.*
4. *Output drive strength is below JEDEC specification.*
5. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

***Table 2-33* • Minimum and Maximum DC Input and Output Levels**

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max., V**	**Min. V**	**mA**	**mA**	**Max. mA[3]**	**Max. mA[3]**	**μA[4]**	**μA[4]**
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

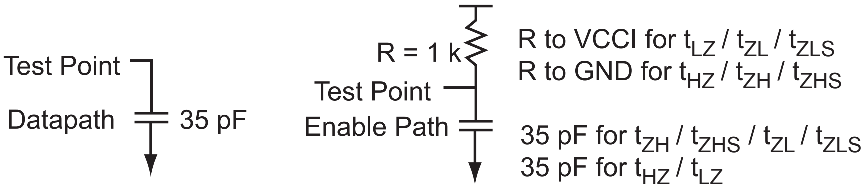


***Figure 2-8* • AC Loading**

***Table 2-34* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

***Table 2-57* • Minimum and Maximum DC Input and Output Levels**

2.5 V GTL+	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA**[1]	**Max. mA**[1]	**µA**[2]	**µA**[2]
33 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

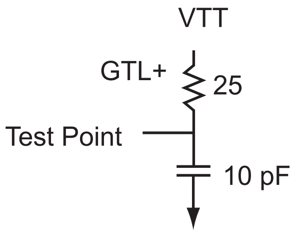


***Figure 2-15* • AC Loading**

***Table 2-58* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

***Table 2-59* • 2.5 V GTL+**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 2.3 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.60	2.21	0.04	1.51	0.43	2.25	2.10			4.48	4.34	ns
–1	0.51	1.88	0.04	1.29	0.36	1.91	1.79			3.81	3.69	ns
–2	0.45	1.65	0.03	1.13	0.32	1.68	1.57			3.35	3.24	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-72 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	μA[2]	μA[2]
14 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14	54	51	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.

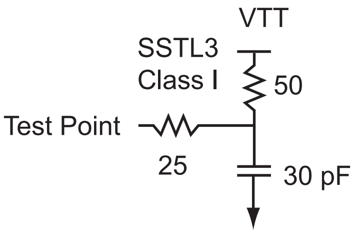


Figure 2-20 • AC Loading

Table 2-73 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-74 • SSTL3 Class I
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.31	0.04	1.25	0.43	2.35	1.84			4.59	4.07	ns
–1	0.56	1.96	0.04	1.06	0.36	2.00	1.56			3.90	3.46	ns
–2	0.49	1.72	0.03	0.93	0.32	1.75	1.37			3.42	3.04	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL[1]	Output Lower Current	0.65	0.91	1.16	mA
IOH[1]	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
IIH[2]	Input High Leakage Current			10	µA
IIL[2]	Input Low Leakage Current			10	µA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage [2]	100	350		mV

Notes:

1. *IOL/IOH defined by VODIFF/(Resistor Network).*
2. *Currents are measured at 85°C junction temperature.*

Table 2-79 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)
1.075	1.325	Cross point	–

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Output Register

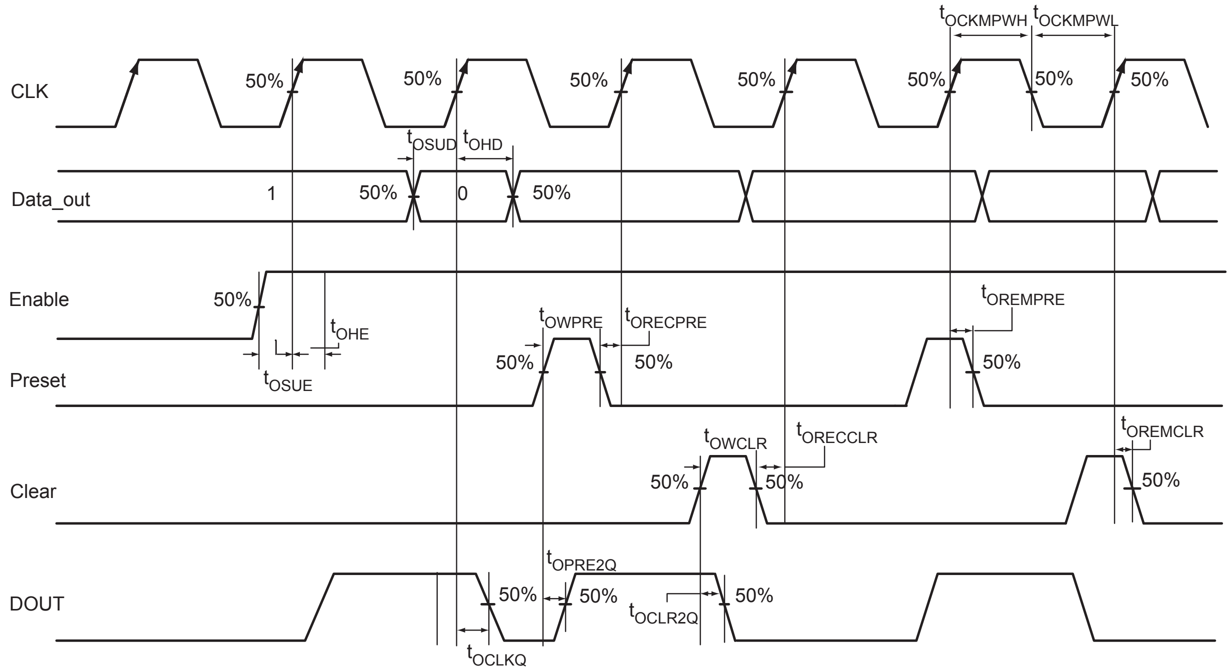


Figure 2-28 • **Output Register Timing Diagram**

Timing Characteristics

Table 2-87 • **Output Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.59	0.67	0.79	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.31	0.36	0.42	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.44	0.50	0.59	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.80	0.91	1.07	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.80	0.91	1.07	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.41	0.48	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Timing Waveforms

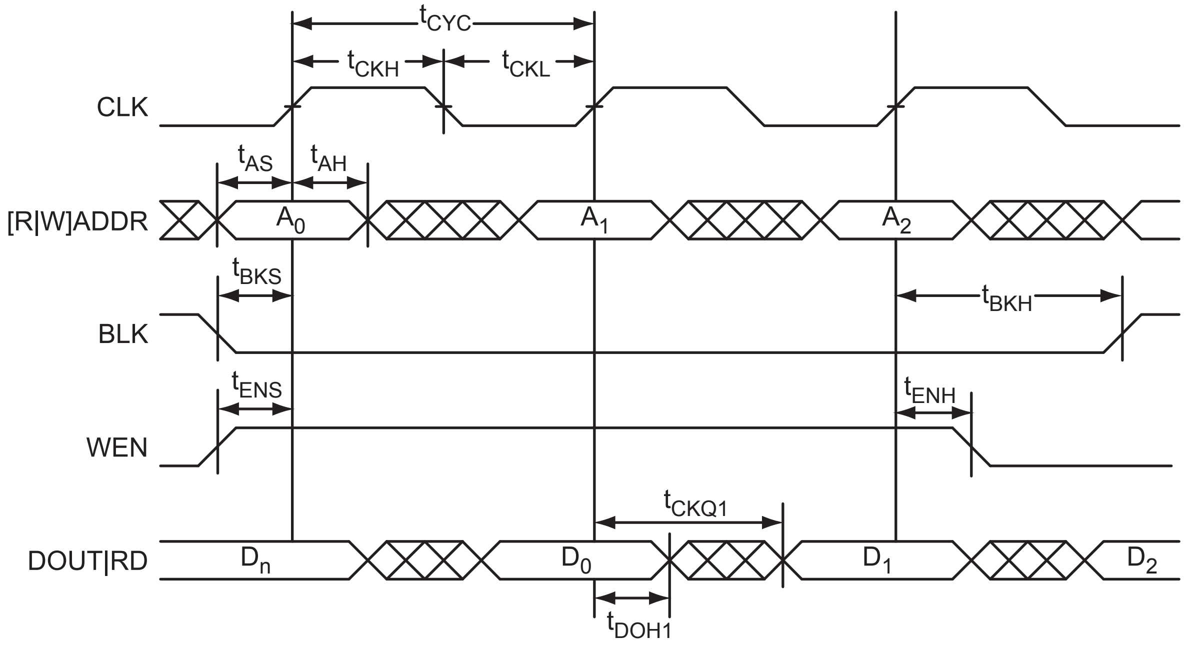


***Figure 2-41* • RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.**

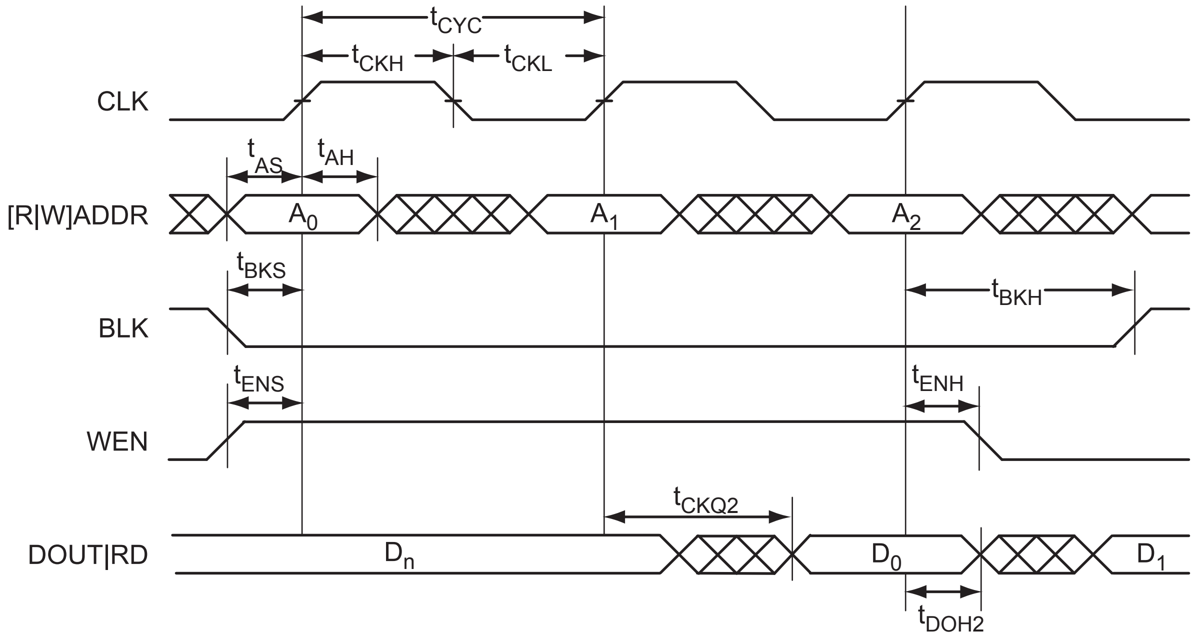


***Figure 2-42* • RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.**

FIFO

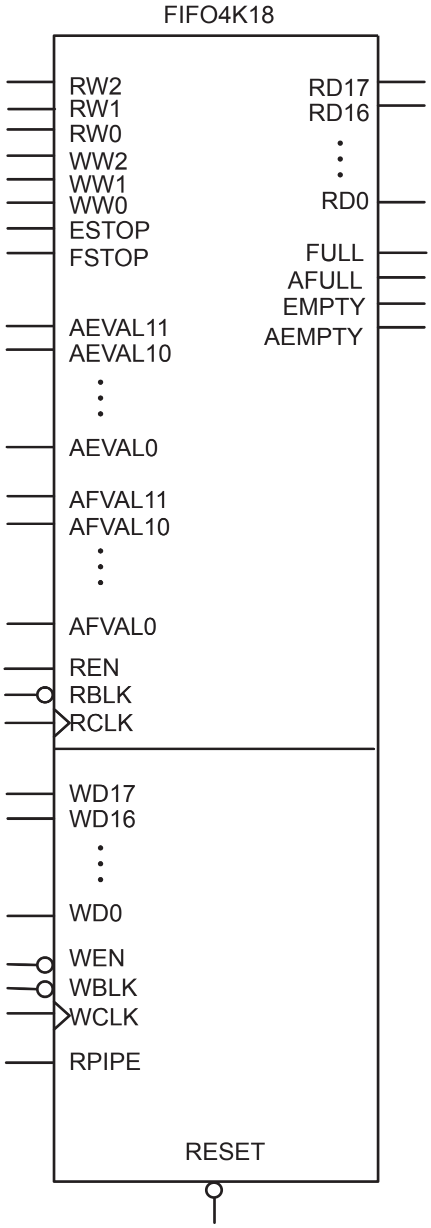


Figure 2-46 • **FIFO Model**

VJTAG JTAG Supply Voltage

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

VPUMP Programming Supply Voltage

For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

User-Defined Supply Pins

VREF I/O Voltage Reference

Reference voltage for I/O minibanks. VREF pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, can be designated the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One VREF pin can support the number of I/Os available in its minibank.

User Pins

I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

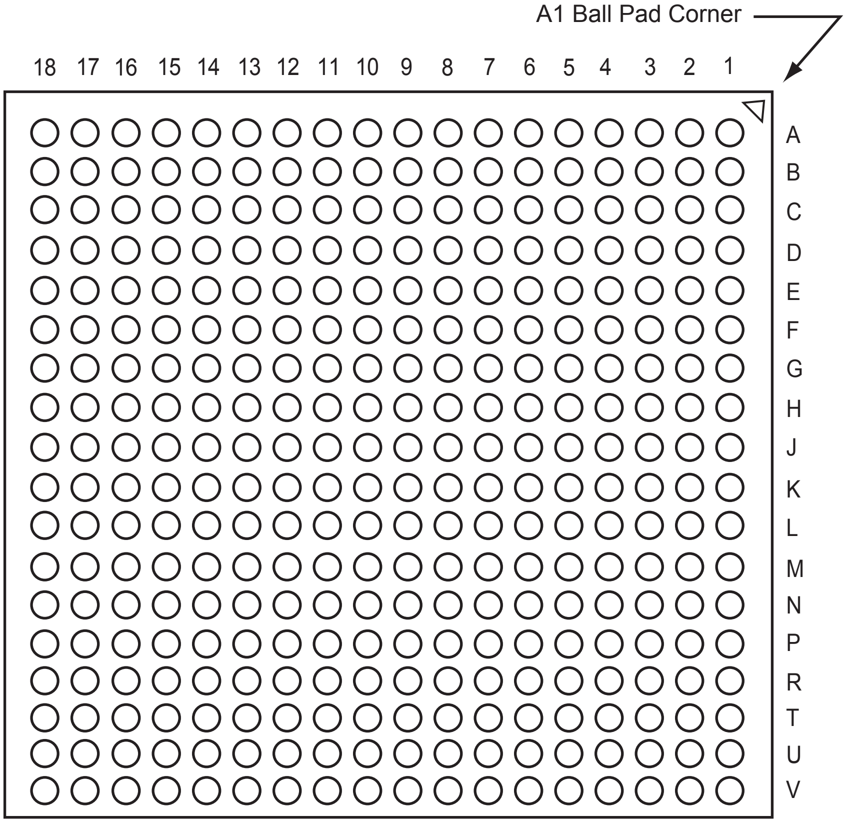
GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *ProASIC3E FPGA Fabric User's Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

PQ208	
Pin Number	A3PE1500 Function
1	GND
2	GNDQ
3	VMV7
4	GAB2/IO220PSB7V3
5	GAA2/IO221PDB7V3
6	IO221NDB7V3
7	GAC2/IO219PDB7V3
8	IO219NDB7V3
9	IO215PDB7V3
10	IO215NDB7V3
11	IO212PDB7V2
12	IO212NDB7V2
13	IO208PDB7V2
14	IO208NDB7V2
15	IO204PSB7V1
16	VCC
17	GND
18	VCCIB7
19	IO200PDB7V1
20	IO200NDB7V1
21	IO196PSB7V0
22	GFC1/IO192PSB7V0
23	GFB1/IO191PDB7V0
24	GFB0/IO191NDB7V0
25	VCOMPLF
26	GFA0/IO190NPB6V2
27	VCCPLF
28	GFA1/IO190PPB6V2
29	GND
30	GFA2/IO189PDB6V2
31	IO189NDB6V2
32	GFB2/IO188PPB6V2
33	GFC2/IO187PPB6V2
34	IO188NPB6V2
35	IO187NPB6V2
36	VCC
37	IO184PDB6V2
38	IO184NDB6V2
39	IO180PSB6V1
40	VCCIB6
41	GND
42	IO176PDB6V1
43	IO176NDB6V1
44	GEC1/IO169PDB6V0
45	GEC0/IO169NDB6V0
46	GEB1/IO168PPB6V0
47	GEA1/IO167PPB6V0
48	GEB0/IO168NPB6V0
49	GEA0/IO167NPB6V0
50	VMV6
51	GNDQ
52	GND
53	VMV5
54	GNDQ
55	IO166NDB5V3
56	GEA2/IO166PDB5V3
57	IO165NDB5V3
58	GEB2/IO165PDB5V3
59	IO164NDB5V3
60	GEC2/IO164PDB5V3
61	IO163PSB5V3
62	VCCIB5
63	IO161PSB5V3
64	IO157NDB5V2
65	GND
66	IO157PDB5V2
67	IO153NDB5V2
68	IO153PDB5V2
69	IO149NDB5V1
70	IO149PDB5V1
71	VCC
72	VCCIB5
73	IO145NDB5V1
74	IO145PDB5V1
75	IO143NDB5V1
76	IO143PDB5V1
77	IO137NDB5V0
78	IO137PDB5V0
79	IO135NDB5V0
80	IO135PDB5V0
81	GND
82	IO131NDB4V2
83	IO131PDB4V2
84	IO129NDB4V2
85	IO129PDB4V2
86	IO127NDB4V2
87	IO127PDB4V2
88	VCC
89	VCCIB4
90	IO121NDB4V1
91	IO121PDB4V1
92	IO119NDB4V1
93	IO119PDB4V1
94	IO113NDB4V0
95	GDC2/IO113PDB4V0
96	IO112NDB4V0
97	GND
98	GDB2/IO112PDB4V0
99	GDA2/IO111PSB4V0
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV4
105	GND
106	VPUMP
107	GNDQ
108	TDO

FG324



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/products/fpga-soc/solutions*.

FG324	
Pin Number	**A3PE3000 FBGA**
G1	GND
G2	IO287PDB7V1
G3	IO287NDB7V1
G4	IO283PPB7V1
G5	VCCIB7
G6	IO279PDB7V0
G7	IO291NPB7V2
G8	VCC
G9	IO26NDB0V3
G10	IO34NDB0V4
G11	VCC
G12	IO94NPB2V1
G13	IO98PDB2V2
G14	VCCIB2
G15	GCC0/IO112NPB2V3
G16	IO104PDB2V2
G17	IO104NDB2V2
G18	GND
H1	IO267PDB6V4
H2	VCCIB7
H3	IO283NPB7V1
H4	GFB1/IO274PPB7V0
H5	GND
H6	IO279NDB7V0
H7	VCC
H8	VCC
H9	GND
H10	GND
H11	VCC
H12	VCC
H13	IO98NDB2V2
H14	GND
H15	GCB1/IO113PDB2V3
H16	GCC1/IO112PPB2V3
H17	VCCIB2
H18	IO108PDB2V3

FG324	
Pin Number	**A3PE3000 FBGA**
J1	IO267NDB6V4
J2	GFA0/IO273NDB6V4
J3	VCOMPLF
J4	GFA2/IO272PDB6V4
J5	GFB0/IO274NPB7V0
J6	GFC0/IO275NDB7V0
J7	GFC1/IO275PDB7V0
J8	GND
J9	GND
J10	GND
J11	GND
J12	GCA2/IO115PDB3V0
J13	GCA1/IO114PDB3V0
J14	GCA0/IO114NDB3V0
J15	GCB0/IO113NDB2V3
J16	VCOMPLC
J17	IO120NPB3V0
J18	IO108NDB2V3
K1	IO263PDB6V3
K2	GFA1/IO273PDB6V4
K3	VCCPLF
K4	IO272NDB6V4
K5	GFC2/IO270PPB6V4
K6	GFB2/IO271PDB6V4
K7	IO271NDB6V4
K8	GND
K9	GND
K10	GND
K11	GND
K12	IO115NDB3V0
K13	GCB2/IO116PDB3V0
K14	IO116NDB3V0
K15	GCC2/IO117PDB3V0
K16	VCCPLC
K17	IO124NPB3V1
K18	IO120PPB3V0

FG324	
Pin Number	**A3PE3000 FBGA**
L1	IO263NDB6V3
L2	VCCIB6
L3	IO259PDB6V3
L4	IO259NDB6V3
L5	GND
L6	IO270NPB6V4
L7	VCC
L8	VCC
L9	GND
L10	GND
L11	VCC
L12	VCC
L13	IO132PDB3V2
L14	GND
L15	IO117NDB3V0
L16	IO128NPB3V1
L17	VCCIB3
L18	IO124PPB3V1
M1	GND
M2	IO255PDB6V2
M3	IO255NDB6V2
M4	IO251PPB6V2
M5	VCCIB6
M6	GEB0/IO235NDB6V0
M7	GEB1/IO235PDB6V0
M8	VCC
M9	IO192PPB4V4
M10	IO154NPB4V0
M11	VCC
M12	GDA0/IO153NPB3V4
M13	IO132NDB3V2
M14	VCCIB3
M15	IO134NDB3V2
M16	IO134PDB3V2
M17	IO128PPB3V1
M18	GND

Revision	Changes	Page
Revision 11 (August 2012)	Added a Note stating "VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information." to Table 2-1 • Absolute Maximum Ratings and Table 2-2 • Recommended Operating Conditions [1] (SAR 38322).	2-1 3-1 2-1
	The drive strength, IOL, and IOH value for 3.3 V GTL and 2.5 V GTL was changed from 25 mA to 20 mA in the following tables (SAR 31924): "Summary of Maximum and Minimum DC Input and Output Levels" table "Summary of I/O Timing Characteristics—Software Default Settings" table "I/O Output Buffer Maximum Resistances[1]" table "Minimum and Maximum DC Input and Output Levels" table) "Minimum and Maximum DC Input and Output Levels" table Also added note stating "Output drive strength is below JEDEC specification" for Tables 2-17 and 2-19. Additionally, the IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected from 51 to 35 (for 3.3 V GTL+) and from 40 to 33 (for 2.5 V GTL+) in table Table 2-13 (SAR 39714).	2-16 2-19 2-20 2-39 2-40
	"Duration of Short Circuit Event Before Failure" table was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 37934).	2-22
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34796): "It uses a 5 V–tolerant input buffer and push-pull output buffer." This change was made in revision 10 and omitted from the change table in error.	2-30
Revision 11 (continued)	Figure 2-11 was updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34889).	2-38
	In Table 2-81 VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 37222).	2-52
	Figure 2-47and Figure 2-48 are new (SAR 34848).	2-79
	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions and Packaging" chapter: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with “Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks” (SAR 38322). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1

Revision	Changes	Page
Advance v0.3 (continued)	The "Methodology" section was updated.	3-9
	The A3PE3000 "208-Pin PQFP" pin table was updated.	4-6