# Microchip Technology - A3PE1500-2FGG484 Datasheet

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 276480 |
| Number of I/O | 280 |
| Number of Gates | 1500000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a3pe1500-2fgg484 |

## Advanced Architecture

The proprietary ProASIC3E architecture provides granularity comparable to standard-cell ASICs. The ProASIC3E device consists of five distinct and programmable architectural features (Figure 1-1 on page 3):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- Pro I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the ProASIC3E core tile as either a three-input lookup table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC family of third-generation architecture Flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

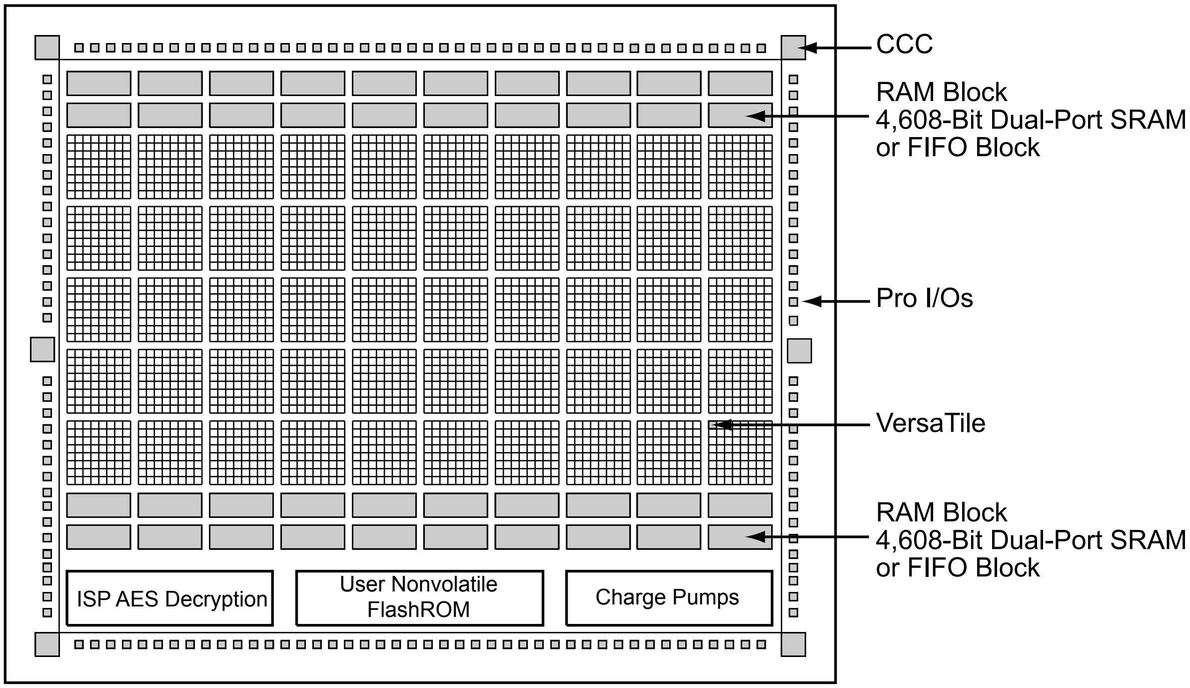

*Figure 1-1 •* **ProASIC3E Device Architecture Overview**

### Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-11 on page 2-11.

$F_{CLK}$ is the global clock signal frequency.

### Routing Net Contribution—$P_{NET}$

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-11 on page 2-11.

$F_{CLK}$ is the global clock signal frequency.

### I/O Input Buffer Contribution—$P_{INPUTS}$

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$

$N_{INPUTS}$ is the number of I/O input buffers used in the design.

$\alpha_2$ is the I/O buffer toggle rate—guidelines are provided in Table 2-11 on page 2-11.

$F_{CLK}$ is the global clock signal frequency.

### I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

$\alpha_2$ is the I/O buffer toggle rate—guidelines are provided in Table 2-11 on page 2-11.

$\beta_1$ is the I/O buffer enable rate—guidelines are provided in Table 2-12 on page 2-11.

$F_{CLK}$ is the global clock signal frequency.

### RAM Contribution—$P_{MEMORY}$

$P_{MEMORY} = PAC11 * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

$N_{BLOCKS}$ is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

$\beta_2$ is the RAM enable rate for read operations—guidelines are provided in Table 2-12 on page 2-11.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

$\beta_3$ is the RAM enable rate for write operations—guidelines are provided in Table 2-12 on page 2-11.

### PLL Contribution—$P_{PLL}$

$P_{PLL} = PAC13 + PAC14 * F_{CLKOUT}$

$F_{CLKOUT}$ is the output clock frequency.[1]

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[1] *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution (PAC14 * $F_{CLKOUT}$ product) to the total PLL contribution.*

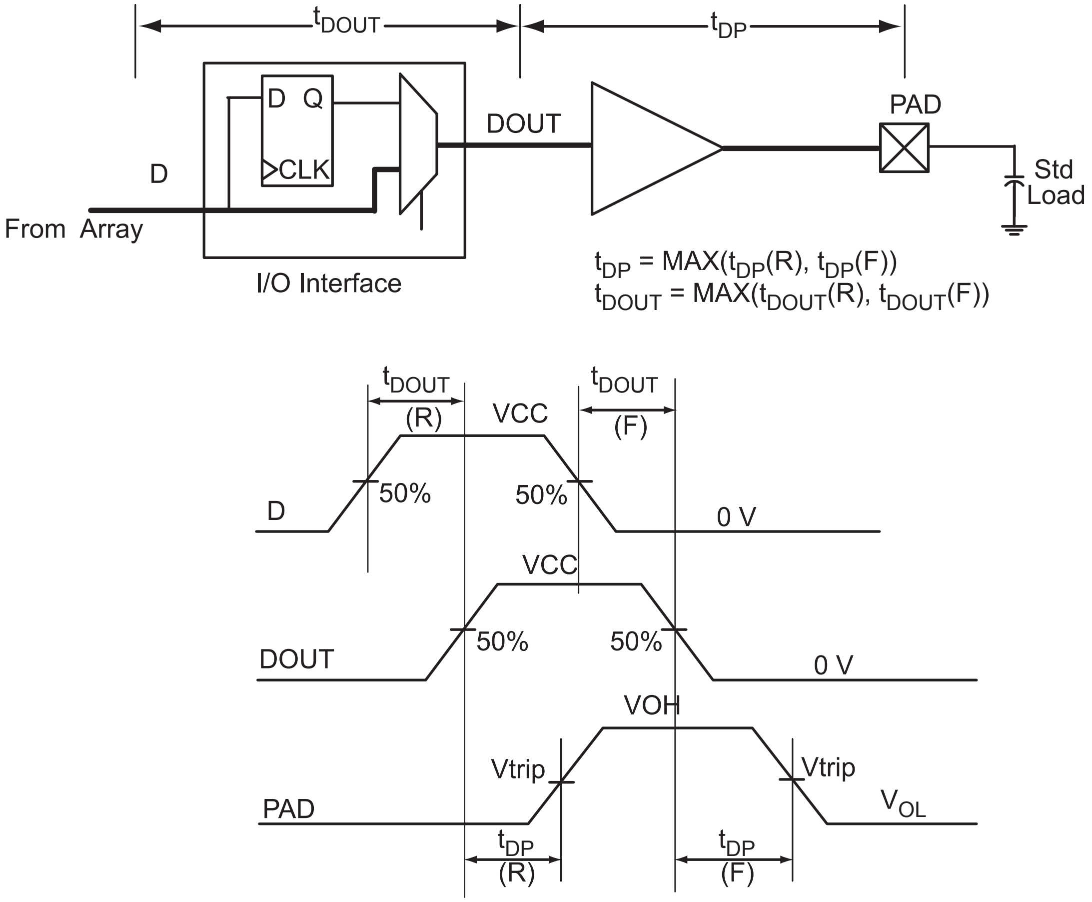

***Figure 2-4 •*** **Output Buffer Model and Delays (example)**

***Table 2-28* • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 12 mA | Std. | 0.66 | 6.03 | 0.04 | 1.20 | 1.57 | 0.43 | 6.14 | 5.02 | 3.28 | 3.47 | 8.37 | 7.26 | ns |
| | –1 | 0.56 | 5.13 | 0.04 | 1.02 | 1.33 | 0.36 | 5.22 | 4.27 | 2.79 | 2.95 | 7.12 | 6.17 | ns |
| | –2 | 0.49 | 4.50 | 0.03 | 0.90 | 1.17 | 0.32 | 4.58 | 3.75 | 2.45 | 2.59 | 6.25 | 5.42 | ns |
| 16 mA | Std. | 0.66 | 5.62 | 0.04 | 1.20 | 1.57 | 0.43 | 5.72 | 4.72 | 3.32 | 3.58 | 7.96 | 6.96 | ns |
| | –1 | 0.56 | 4.78 | 0.04 | 1.02 | 1.33 | 0.36 | 4.87 | 4.02 | 2.83 | 3.04 | 6.77 | 5.92 | ns |
| | –2 | 0.49 | 4.20 | 0.03 | 0.90 | 1.17 | 0.32 | 4.27 | 3.53 | 2.48 | 2.67 | 5.94 | 5.20 | ns |
| 24 mA | Std. | 0.66 | 5.24 | 0.04 | 1.20 | 1.57 | 0.43 | 5.34 | 4.69 | 3.39 | 3.96 | 7.58 | 6.93 | ns |
| | –1 | 0.56 | 4.46 | 0.04 | 1.02 | 1.33 | 0.36 | 4.54 | 3.99 | 2.88 | 3.37 | 6.44 | 5.89 | ns |
| | –2 | 0.49 | 3.92 | 0.03 | 0.90 | 1.17 | 0.32 | 3.99 | 3.50 | 2.53 | 2.96 | 5.66 | 5.17 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

### *Timing Characteristics*

***Table 2-35* • 2.5 V LVCMOS High Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 0.66 | 8.82 | 0.04 | 1.51 | 1.66 | 0.43 | 8.13 | 8.82 | 2.72 | 2.29 | 10.37 | 11.05 | ns |
| | –1 | 0.56 | 7.50 | 0.04 | 1.29 | 1.41 | 0.36 | 6.92 | 7.50 | 2.31 | 1.95 | 8.82 | 9.40 | ns |
| | –2 | 0.49 | 6.58 | 0.03 | 1.13 | 1.24 | 0.32 | 6.07 | 6.58 | 2.03 | 1.71 | 7.74 | 8.25 | ns |
| 8 mA | Std. | 0.66 | 5.27 | 0.04 | 1.51 | 1.66 | 0.43 | 5.27 | 5.27 | 3.10 | 3.03 | 7.50 | 7.51 | ns |
| | –1 | 0.56 | 4.48 | 0.04 | 1.29 | 1.41 | 0.36 | 4.48 | 4.48 | 2.64 | 2.58 | 6.38 | 6.38 | ns |
| | –2 | 0.49 | 3.94 | 0.03 | 1.13 | 1.24 | 0.32 | 3.93 | 3.94 | 2.32 | 2.26 | 5.60 | 5.61 | ns |
| 12 mA | Std. | 0.66 | 3.74 | 0.04 | 1.51 | 1.66 | 0.43 | 3.81 | 3.49 | 3.37 | 3.49 | 6.05 | 5.73 | ns |
| | –1 | 0.56 | 3.18 | 0.04 | 1.29 | 1.41 | 0.36 | 3.24 | 2.97 | 2.86 | 2.97 | 5.15 | 4.87 | ns |
| | –2 | 0.49 | 2.80 | 0.03 | 1.13 | 1.24 | 0.32 | 2.85 | 2.61 | 2.51 | 2.61 | 4.52 | 4.28 | ns |
| 16 mA | Std. | 0.66 | 3.53 | 0.04 | 1.51 | 1.66 | 0.43 | 3.59 | 3.12 | 3.42 | 3.62 | 5.83 | 5.35 | ns |
| | –1 | 0.56 | 3.00 | 0.04 | 1.29 | 1.41 | 0.36 | 3.06 | 2.65 | 2.91 | 3.08 | 4.96 | 4.55 | ns |
| | –2 | 0.49 | 2.63 | 0.03 | 1.13 | 1.24 | 0.32 | 2.68 | 2.33 | 2.56 | 2.71 | 4.35 | 4.00 | ns |
| 24 mA | Std. | 0.66 | 3.26 | 0.04 | 1.51 | 1.66 | 0.43 | 3.32 | 2.48 | 3.49 | 4.11 | 5.56 | 4.72 | ns |
| | –1 | 0.56 | 2.77 | 0.04 | 1.29 | 1.41 | 0.36 | 2.83 | 2.11 | 2.97 | 3.49 | 4.73 | 4.01 | ns |
| | –2 | 0.49 | 2.44 | 0.03 | 1.13 | 1.24 | 0.32 | 2.48 | 1.85 | 2.61 | 3.07 | 4.15 | 3.52 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

### Timing Characteristics

**Table 2-39 • 1.8 V LVCMOS High Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 12.10 | 0.04 | 1.45 | 1.91 | 0.43 | 9.59 | 12.10 | 2.78 | 1.64 | 11.83 | 14.34 | ns |
| | –1 | 0.56 | 10.30 | 0.04 | 1.23 | 1.62 | 0.36 | 8.16 | 10.30 | 2.37 | 1.39 | 10.06 | 12.20 | ns |
| | –2 | 0.49 | 9.04 | 0.03 | 1.08 | 1.42 | 0.32 | 7.16 | 9.04 | 2.08 | 1.22 | 8.83 | 10.71 | ns |
| 4 mA | Std. | 0.66 | 7.05 | 0.04 | 1.45 | 1.91 | 0.43 | 6.20 | 7.05 | 3.25 | 2.86 | 8.44 | 9.29 | ns |
| | –1 | 0.56 | 6.00 | 0.04 | 1.23 | 1.62 | 0.36 | 5.28 | 6.00 | 2.76 | 2.44 | 7.18 | 7.90 | ns |
| | –2 | 0.49 | 5.27 | 0.03 | 1.08 | 1.42 | 0.32 | 4.63 | 5.27 | 2.43 | 2.14 | 6.30 | 6.94 | ns |
| 6 mA | Std. | 0.66 | 4.52 | 0.04 | 1.45 | 1.91 | 0.43 | 4.47 | 4.52 | 3.57 | 3.47 | 6.70 | 6.76 | ns |
| | –1 | 0.56 | 3.85 | 0.04 | 1.23 | 1.62 | 0.36 | 3.80 | 3.85 | 3.04 | 2.95 | 5.70 | 5.75 | ns |
| | –2 | 0.49 | 3.38 | 0.03 | 1.08 | 1.42 | 0.32 | 3.33 | 3.38 | 2.66 | 2.59 | 5.00 | 5.05 | ns |
| 8 mA | Std. | 0.66 | 4.12 | 0.04 | 1.45 | 1.91 | 0.43 | 4.20 | 3.99 | 3.63 | 3.62 | 6.43 | 6.23 | ns |
| | –1 | 0.56 | 3.51 | 0.04 | 1.23 | 1.62 | 0.36 | 3.57 | 3.40 | 3.09 | 3.08 | 5.47 | 5.30 | ns |
| | –2 | 0.49 | 3.08 | 0.03 | 1.08 | 1.42 | 0.32 | 3.14 | 2.98 | 2.71 | 2.71 | 4.81 | 4.65 | ns |
| 12 mA | Std. | 0.66 | 3.80 | 0.04 | 1.45 | 1.91 | 0.43 | 3.87 | 3.09 | 3.73 | 4.24 | 6.10 | 5.32 | ns |
| | –1 | 0.56 | 3.23 | 0.04 | 1.23 | 1.62 | 0.36 | 3.29 | 2.63 | 3.18 | 3.60 | 5.19 | 4.53 | ns |
| | –2 | 0.49 | 2.83 | 0.03 | 1.08 | 1.42 | 0.32 | 2.89 | 2.31 | 2.79 | 3.16 | 4.56 | 3.98 | ns |
| 16 mA | Std. | 0.66 | 3.80 | 0.04 | 1.45 | 1.91 | 0.43 | 3.87 | 3.09 | 3.73 | 4.24 | 6.10 | 5.32 | ns |
| | –1 | 0.56 | 3.23 | 0.04 | 1.23 | 1.62 | 0.36 | 3.29 | 2.63 | 3.18 | 3.60 | 5.19 | 4.53 | ns |
| | –2 | 0.49 | 2.83 | 0.03 | 1.08 | 1.42 | 0.32 | 2.89 | 2.31 | 2.79 | 3.16 | 4.56 | 3.98 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

### Timing Characteristics

***Table 2-43*** **• 1.5 V LVCMOS High Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 8.53 | 0.04 | 1.70 | 2.14 | 0.43 | 7.26 | 8.53 | 3.39 | 2.79 | 9.50 | 10.77 | ns |
| | –1 | 0.56 | 7.26 | 0.04 | 1.44 | 1.82 | 0.36 | 6.18 | 7.26 | 2.89 | 2.37 | 8.08 | 9.16 | ns |
| | –2 | 0.49 | 6.37 | 0.03 | 1.27 | 1.60 | 0.32 | 5.42 | 6.37 | 2.53 | 2.08 | 7.09 | 8.04 | ns |
| 4 mA | Std. | 0.66 | 5.41 | 0.04 | 1.70 | 2.14 | 0.43 | 5.22 | 5.41 | 3.75 | 3.48 | 7.45 | 7.65 | ns |
| | –1 | 0.56 | 4.60 | 0.04 | 1.44 | 1.82 | 0.36 | 4.44 | 4.60 | 3.19 | 2.96 | 6.34 | 6.50 | ns |
| | –2 | 0.49 | 4.04 | 0.03 | 1.27 | 1.60 | 0.32 | 3.89 | 4.04 | 2.80 | 2.60 | 5.56 | 5.71 | ns |
| 6 mA | Std. | 0.66 | 4.80 | 0.04 | 1.70 | 2.14 | 0.43 | 4.89 | 4.75 | 3.83 | 3.67 | 7.13 | 6.98 | ns |
| | –1 | 0.56 | 4.09 | 0.04 | 1.44 | 1.82 | 0.36 | 4.16 | 4.04 | 3.26 | 3.12 | 6.06 | 5.94 | ns |
| | –2 | 0.49 | 3.59 | 0.03 | 1.27 | 1.60 | 0.32 | 3.65 | 3.54 | 2.86 | 2.74 | 5.32 | 5.21 | ns |
| 8 mA | Std. | 0.66 | 4.42 | 0.04 | 1.70 | 2.14 | 0.43 | 4.50 | 3.62 | 3.96 | 4.37 | 6.74 | 5.86 | ns |
| | –1 | 0.56 | 3.76 | 0.04 | 1.44 | 1.82 | 0.36 | 3.83 | 3.08 | 3.37 | 3.72 | 5.73 | 4.98 | ns |
| | –2 | 0.49 | 3.30 | 0.03 | 1.27 | 1.60 | 0.32 | 3.36 | 2.70 | 2.96 | 3.27 | 5.03 | 4.37 | ns |
| 12 mA | Std. | 0.66 | 4.42 | 0.04 | 1.70 | 2.14 | 0.43 | 4.50 | 3.62 | 3.96 | 4.37 | 6.74 | 5.86 | ns |
| | –1 | 0.56 | 3.76 | 0.04 | 1.44 | 1.82 | 0.36 | 3.83 | 3.08 | 3.37 | 3.72 | 5.73 | 4.98 | ns |
| | –2 | 0.49 | 3.30 | 0.03 | 1.27 | 1.60 | 0.32 | 3.36 | 2.70 | 2.96 | 3.27 | 5.03 | 4.37 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

***Table 2-44*** **• 1.5 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 14.11 | 0.04 | 1.70 | 2.14 | 0.43 | 14.37 | 13.14 | 3.40 | 2.68 | 16.61 | 15.37 | ns |
| | –1 | 0.56 | 12.00 | 0.04 | 1.44 | 1.82 | 0.36 | 12.22 | 11.17 | 2.90 | 2.28 | 14.13 | 13.08 | ns |
| | –2 | 0.49 | 10.54 | 0.03 | 1.27 | 1.60 | 0.32 | 10.73 | 9.81 | 2.54 | 2.00 | 12.40 | 11.48 | ns |
| 4 mA | Std. | 0.66 | 11.23 | 0.04 | 1.70 | 2.14 | 0.43 | 11.44 | 9.87 | 3.77 | 3.36 | 13.68 | 12.10 | ns |
| | –1 | 0.56 | 9.55 | 0.04 | 1.44 | 1.82 | 0.36 | 9.73 | 8.39 | 3.21 | 2.86 | 11.63 | 10.29 | ns |
| | –2 | 0.49 | 8.39 | 0.03 | 1.27 | 1.60 | 0.32 | 8.54 | 7.37 | 2.81 | 2.51 | 10.21 | 9.04 | ns |
| 6 mA | Std. | 0.66 | 10.45 | 0.04 | 1.70 | 2.14 | 0.43 | 10.65 | 9.24 | 3.84 | 3.55 | 12.88 | 11.48 | ns |
| | –1 | 0.56 | 8.89 | 0.04 | 1.44 | 1.82 | 0.36 | 9.06 | 7.86 | 3.27 | 3.02 | 10.96 | 9.76 | ns |
| | –2 | 0.49 | 7.81 | 0.03 | 1.27 | 1.60 | 0.32 | 7.95 | 6.90 | 2.87 | 2.65 | 9.62 | 8.57 | ns |
| 8 mA | Std. | 0.66 | 10.02 | 0.04 | 1.70 | 2.14 | 0.43 | 10.20 | 9.23 | 3.97 | 4.22 | 12.44 | 11.47 | ns |
| | –1 | 0.56 | 8.52 | 0.04 | 1.44 | 1.82 | 0.36 | 8.68 | 7.85 | 3.38 | 3.59 | 10.58 | 9.75 | ns |
| | –2 | 0.49 | 7.48 | 0.03 | 1.27 | 1.60 | 0.32 | 7.62 | 6.89 | 2.97 | 3.15 | 9.29 | 8.56 | ns |
| 12 mA | Std. | 0.66 | 10.02 | 0.04 | 1.70 | 2.14 | 0.43 | 10.20 | 9.23 | 3.97 | 4.22 | 12.44 | 11.47 | ns |
| | –1 | 0.56 | 8.52 | 0.04 | 1.44 | 1.82 | 0.36 | 8.68 | 7.85 | 3.38 | 3.59 | 10.58 | 9.75 | ns |
| | –2 | 0.49 | 7.48 | 0.03 | 1.27 | 1.60 | 0.32 | 7.62 | 6.89 | 2.97 | 3.15 | 9.29 | 8.56 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

## HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

***Table 2-63* • Minimum and Maximum DC Input and Output Levels**

| HSTL Class II | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL | IIH |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max., V | Min. V | mA | mA | Max. mA[1] | Max. mA[1] | µA[2] | µA[2] |
| 15 mA[3] | –0.3 | VREF – 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI – 0.4 | 15 | 15 | 55 | 66 | 10 | 10 |

*Notes:*

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

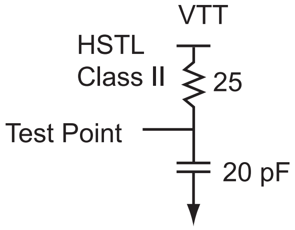

***Figure 2-17* • AC Loading**

***Table 2-64* • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|---|
| VREF – 0.1 | VREF + 0.1 | 0.75 | 0.75 | 0.75 | 20 |

*Note:* *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

### *Timing Characteristics*

***Table 2-65* • HSTL Class II**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V,**
**Worst-Case VCCI = 1.4 V, VREF = 0.75 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 3.02 | 0.04 | 2.12 | 0.43 | 3.08 | 2.71 | | | 5.32 | 4.95 | ns |
| –1 | 0.56 | 2.57 | 0.04 | 1.81 | 0.36 | 2.62 | 2.31 | | | 4.52 | 4.21 | ns |
| –2 | 0.49 | 2.26 | 0.03 | 1.59 | 0.32 | 2.30 | 2.03 | | | 3.97 | 3.70 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

**Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels**

| DC Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| VCCI | Supply Voltage | 2.375 | 2.5 | 2.625 | V |
| VOL | Output Low Voltage | 0.9 | 1.075 | 1.25 | V |
| VOH | Output High Voltage | 1.25 | 1.425 | 1.6 | V |
| IOL[1] | Output Lower Current | 0.65 | 0.91 | 1.16 | mA |
| IOH[1] | Output High Current | 0.65 | 0.91 | 1.16 | mA |
| VI | Input Voltage | 0 |  | 2.925 | V |
| IIH[2] | Input High Leakage Current |  |  | 10 | µA |
| IIL[2] | Input Low Leakage Current |  |  | 10 | µA |
| VODIFF | Differential Output Voltage | 250 | 350 | 450 | mV |
| VOCM | Output Common Mode Voltage | 1.125 | 1.25 | 1.375 | V |
| VICM | Input Common Mode Voltage | 0.05 | 1.25 | 2.35 | V |
| VIDIFF | Input Differential Voltage [2] | 100 | 350 |  | mV |

*Notes:*

1. *IOL/IOH defined by VODIFF/(Resistor Network).*
2. *Currents are measured at 85°C junction temperature.*

**Table 2-79 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) |
|---|---|---|---|
| 1.075 | 1.325 | Cross point | – |

*Note:* *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

*Table 2-85* • **Parameter Definition and Measuring Nodes**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | HH, DOUT |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | FF, HH |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | FF, HH |
| $t_{OSUE}$ | Enable Setup Time for the Output Data Register | GG, HH |
| $t_{OHE}$ | Enable Hold Time for the Output Data Register | GG, HH |
| $t_{OCLR2Q}$ | Asynchronous Clear-to-Q of the Output Data Register | LL, DOUT |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | LL, HH |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | LL, HH |
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | HH, EOUT |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | JJ, HH |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | JJ, HH |
| $t_{OESUE}$ | Enable Setup Time for the Output Enable Register | KK, HH |
| $t_{OEHE}$ | Enable Hold Time for the Output Enable Register | KK, HH |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | II, EOUT |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | II, HH |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | II, HH |
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | AA, EE |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | CC, AA |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | CC, AA |
| $t_{ISUE}$ | Enable Setup Time for the Input Data Register | BB, AA |
| $t_{IHE}$ | Enable Hold Time for the Input Data Register | BB, AA |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | DD, EE |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | DD, AA |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | DD, AA |

Note: *See Figure 2-26 on page 2-55 for more information.

## Output Enable Register

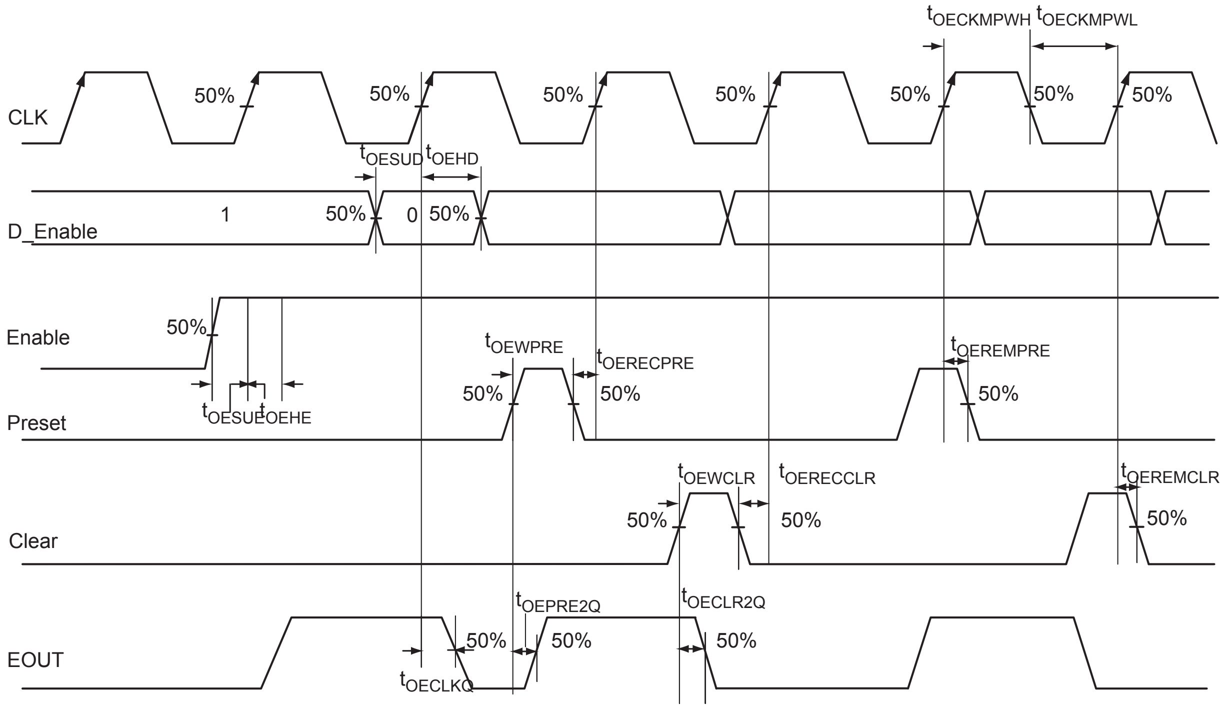

***Figure 2-29* • Output Enable Register Timing Diagram**

### Timing Characteristics

***Table 2-88* • Output Enable Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | 0.59 | 0.67 | 0.79 | ns |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | 0.31 | 0.36 | 0.42 | ns |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{OESUE}$ | Enable Setup Time for the Output Enable Register | 0.44 | 0.50 | 0.58 | ns |
| $t_{OEHE}$ | Enable Hold Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | 0.67 | 0.76 | 0.89 | ns |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | 0.67 | 0.76 | 0.89 | ns |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{OERECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OEWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OEWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OECKMPWH}$ | Clock Minimum Pulse Width High for the Output Enable Register | 0.36 | 0.41 | 0.48 | ns |
| $t_{OECKMPWL}$ | Clock Minimum Pulse Width Low for the Output Enable Register | 0.32 | 0.37 | 0.43 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

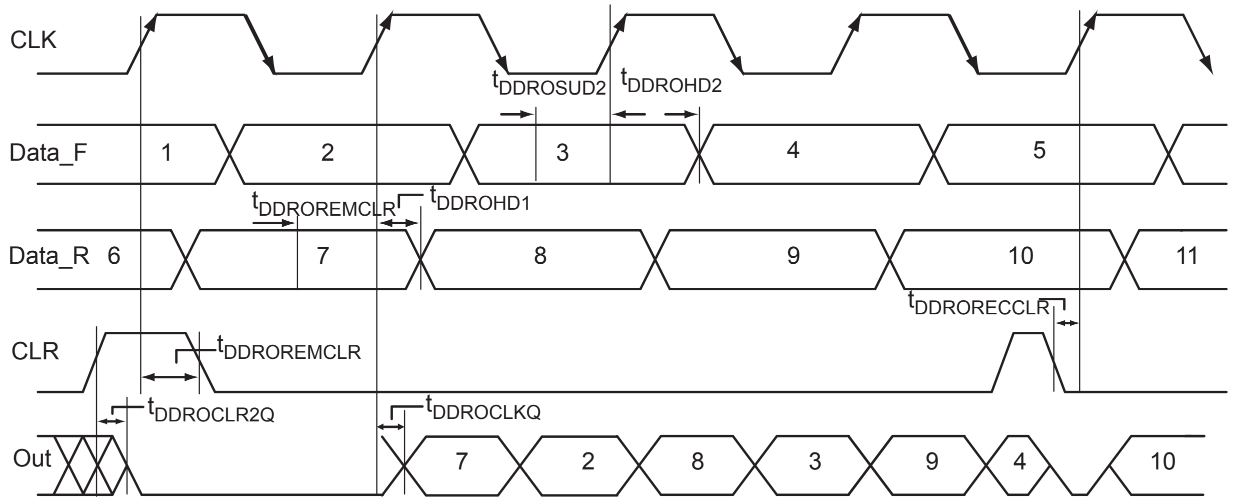

***Figure 2-33* • Output DDR Timing Diagram**

### Timing Characteristics

***Table 2-92* • Output DDR Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out of DDR for Output DDR | 0.70 | 0.80 | 0.94 | ns |
| $t_{DDROSUD1}$ | Data_F Data Setup for Output DDR | 0.38 | 0.43 | 0.51 | ns |
| $t_{DDROSUD2}$ | Data_R Data Setup for Output DDR | 0.38 | 0.43 | 0.51 | ns |
| $t_{DDROHD1}$ | Data_F Data Hold for Output DDR | 0.00 | 0.00 | 0.00 | ns |
| $t_{DDROHD2}$ | Data_R Data Hold for Output DDR | 0.00 | 0.00 | 0.00 | ns |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out for Output DDR | 0.80 | 0.91 | 1.07 | ns |
| $t_{DDROREMCLR}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | 0.00 | 0.00 | ns |
| $t_{DDRORECCLR}$ | Asynchronous Clear Recovery Time for Output DDR | 0.22 | 0.25 | 0.30 | ns |
| $t_{DDROWCLR1}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.22 | 0.25 | 0.30 | ns |
| $t_{DDROCKMPWH}$ | Clock Minimum Pulse Width High for the Output DDR | 0.36 | 0.41 | 0.48 | ns |
| $t_{DDROCKMPWL}$ | Clock Minimum Pulse Width Low for the Output DDR | 0.32 | 0.37 | 0.43 | ns |
| $F_{DDOMAX}$ | Maximum Frequency for the Output DDR | 1404 | 1232 | 1048 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

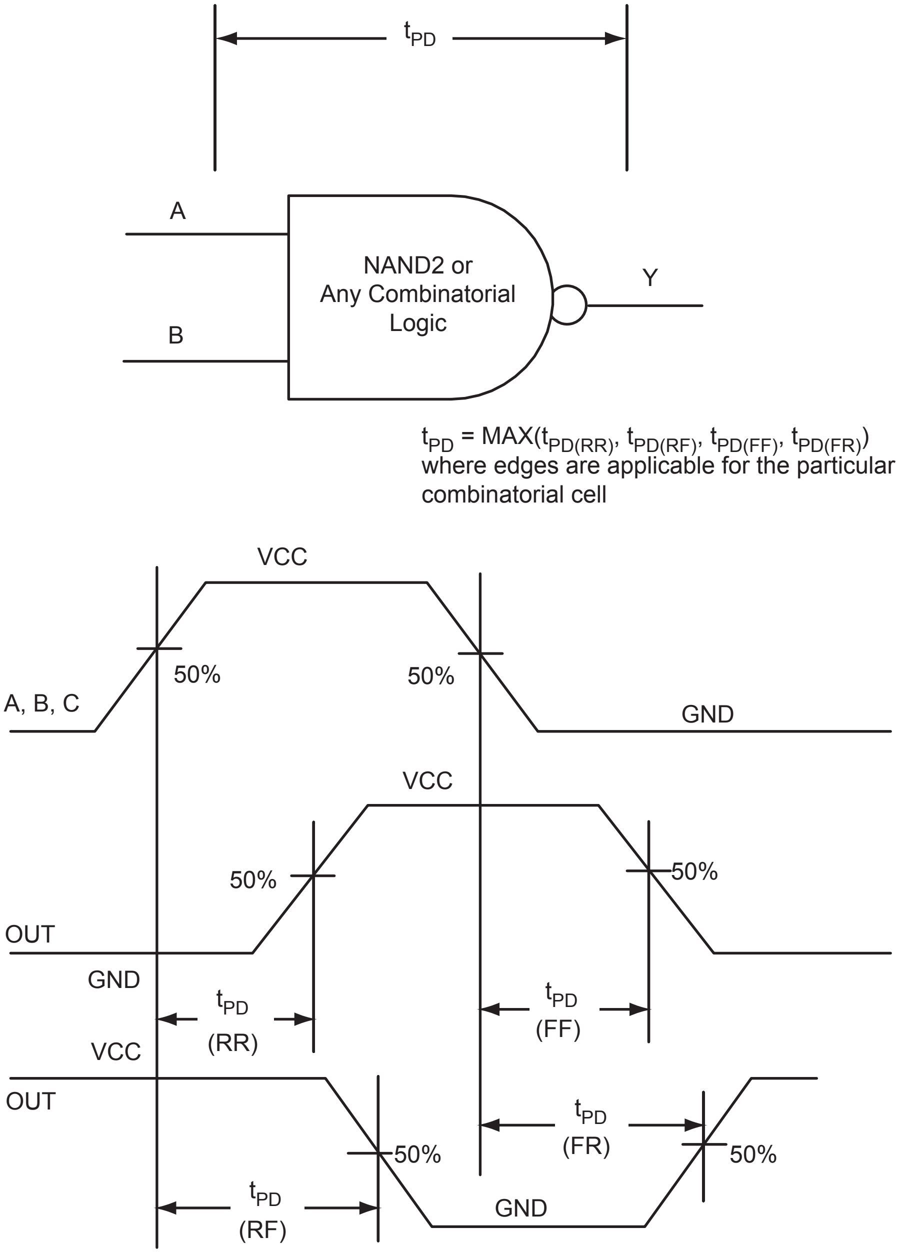

***Figure 2-35 •*** **Timing Model and Waveforms**

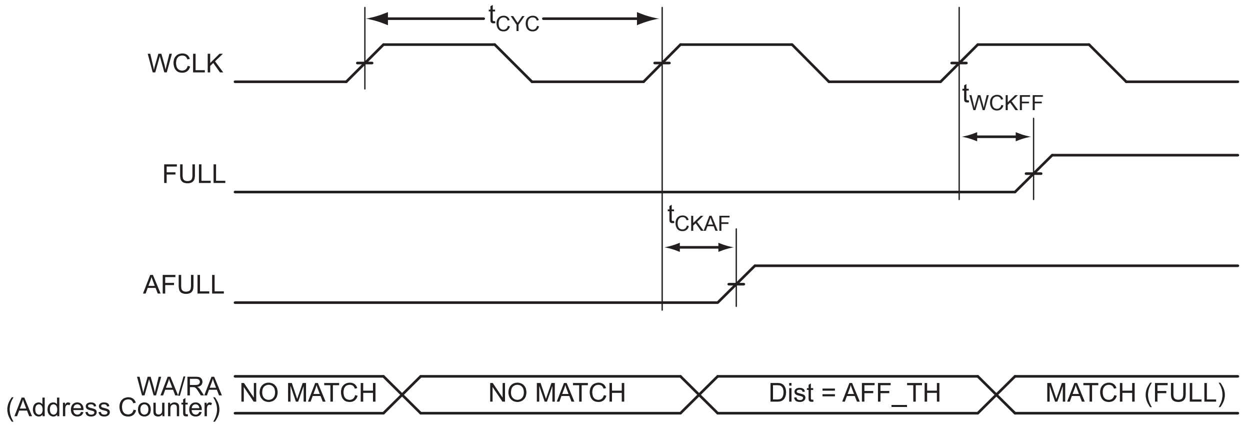

***Figure 2-51* • FIFO FULL Flag and AFULL Flag Assertion**

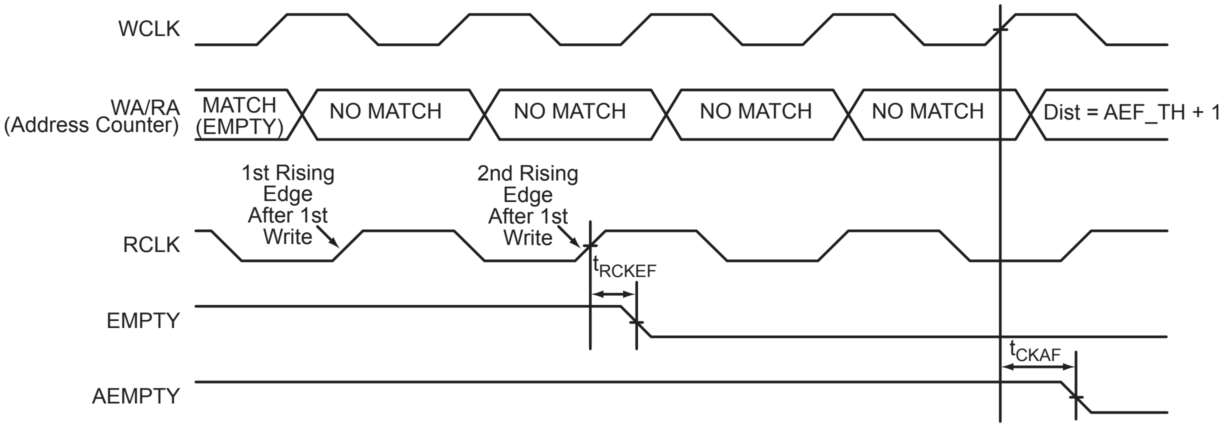

***Figure 2-52* • FIFO EMPTY Flag and AEMPTY Flag Deassertion**

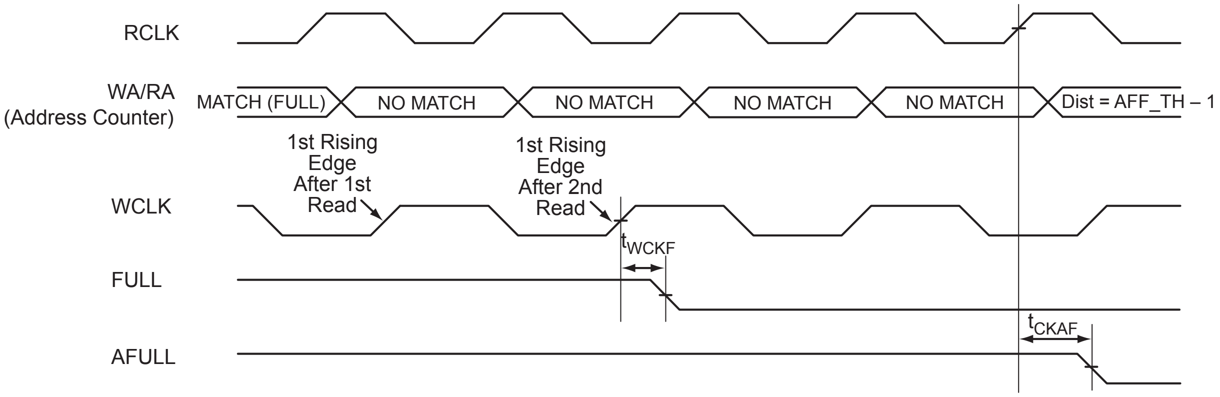

***Figure 2-53* • FIFO FULL Flag and AFULL Flag Deassertion**

### VJTAG JTAG Supply Voltage

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

### VPUMP Programming Supply Voltage

For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

## User-Defined Supply Pins

### VREF I/O Voltage Reference

Reference voltage for I/O minibanks. VREF pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, can be designated the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One VREF pin can support the number of I/Os available in its minibank.

## User Pins

### I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

### GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *ProASIC3E FPGA Fabric User's Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

| PQ208 | |
|---|---|
| **Pin Number** | **A3PE600 Function** |
| 108 | TDO |
| 109 | TRST |
| 110 | VJTAG |
| 111 | VMV3 |
| 112 | GDA0/IO67NPB3V1 |
| 113 | GDB0/IO66NPB3V1 |
| 114 | GDA1/IO67PPB3V1 |
| 115 | GDB1/IO66PPB3V1 |
| 116 | GDC0/IO65NDB3V1 |
| 117 | GDC1/IO65PDB3V1 |
| 118 | IO62NDB3V1 |
| 119 | IO62PDB3V1 |
| 120 | IO58NDB3V0 |
| 121 | IO58PDB3V0 |
| 122 | GND |
| 123 | VCCIB3 |
| 124 | GCC2/IO55PSB3V0 |
| 125 | GCB2/IO54PSB3V0 |
| 126 | NC |
| 127 | IO53NDB3V0 |
| 128 | GCA2/IO53PDB3V0 |
| 129 | GCA1/IO52PPB3V0 |
| 130 | GND |
| 131 | VCCPLC |
| 132 | GCA0/IO52NPB3V0 |
| 133 | VCOMPLC |
| 134 | GCB0/IO51NDB2V1 |
| 135 | GCB1/IO51PDB2V1 |
| 136 | GCC1/IO50PSB2V1 |
| 137 | IO49NDB2V1 |
| 138 | IO49PDB2V1 |
| 139 | IO48PSB2V1 |
| 140 | VCCIB2 |
| 141 | GND |
| 142 | VCC |
| 143 | IO47NDB2V1 |

| PQ208 | |
|---|---|
| **Pin Number** | **A3PE600 Function** |
| 144 | IO47PDB2V1 |
| 145 | IO44NDB2V1 |
| 146 | IO44PDB2V1 |
| 147 | IO43NDB2V0 |
| 148 | IO43PDB2V0 |
| 149 | IO40NDB2V0 |
| 150 | IO40PDB2V0 |
| 151 | GBC2/IO38PSB2V0 |
| 152 | GBA2/IO36PSB2V0 |
| 153 | GBB2/IO37PSB2V0 |
| 154 | VMV2 |
| 155 | GNDQ |
| 156 | GND |
| 157 | VMV1 |
| 158 | GNDQ |
| 159 | GBA1/IO35PDB1V1 |
| 160 | GBA0/IO35NDB1V1 |
| 161 | GBB1/IO34PDB1V1 |
| 162 | GND |
| 163 | GBB0/IO34NDB1V1 |
| 164 | GBC1/IO33PDB1V1 |
| 165 | GBC0/IO33NDB1V1 |
| 166 | IO31PDB1V1 |
| 167 | IO31NDB1V1 |
| 168 | IO27PDB1V0 |
| 169 | IO27NDB1V0 |
| 170 | VCCIB1 |
| 171 | VCC |
| 172 | IO23PPB1V0 |
| 173 | IO22PSB1V0 |
| 174 | IO23NPB1V0 |
| 175 | IO21PDB1V0 |
| 176 | IO21NDB1V0 |
| 177 | IO19PPB0V2 |
| 178 | GND |
| 179 | IO18PPB0V2 |

| PQ208 | |
|---|---|
| **Pin Number** | **A3PE600 Function** |
| 180 | IO19NPB0V2 |
| 181 | IO18NPB0V2 |
| 182 | IO17PPB0V2 |
| 183 | IO16PPB0V2 |
| 184 | IO17NPB0V2 |
| 185 | IO16NPB0V2 |
| 186 | VCCIB0 |
| 187 | VCC |
| 188 | IO15PDB0V2 |
| 189 | IO15NDB0V2 |
| 190 | IO13PDB0V2 |
| 191 | IO13NDB0V2 |
| 192 | IO11PSB0V1 |
| 193 | IO09PDB0V1 |
| 194 | IO09NDB0V1 |
| 195 | GND |
| 196 | IO07PDB0V1 |
| 197 | IO07NDB0V1 |
| 198 | IO05PDB0V0 |
| 199 | IO05NDB0V0 |
| 200 | VCCIB0 |
| 201 | GAC1/IO02PDB0V0 |
| 202 | GAC0/IO02NDB0V0 |
| 203 | GAB1/IO01PDB0V0 |
| 204 | GAB0/IO01NDB0V0 |
| 205 | GAA1/IO00PDB0V0 |
| 206 | GAA0/IO00NDB0V0 |
| 207 | GNDQ |
| 208 | VMV0 |

| FG484 | |
|---|---|
| **Pin Number** | **A3PE600 Function** |
| N17 | IO57NPB3V0 |
| N18 | IO55NPB3V0 |
| N19 | IO57PPB3V0 |
| N20 | NC |
| N21 | IO56NDB3V0 |
| N22 | IO58PDB3V0 |
| P1 | NC |
| P2 | IO111PDB6V1 |
| P3 | IO115NPB6V1 |
| P4 | IO113NPB6V1 |
| P5 | IO109PPB6V0 |
| P6 | IO108PDB6V0 |
| P7 | IO108NDB6V0 |
| P8 | VCCIB6 |
| P9 | GND |
| P10 | VCC |
| P11 | VCC |
| P12 | VCC |
| P13 | VCC |
| P14 | GND |
| P15 | VCCIB3 |
| P16 | GDB0/IO66NPB3V1 |
| P17 | IO60NDB3V1 |
| P18 | IO60PDB3V1 |
| P19 | IO61PDB3V1 |
| P20 | NC |
| P21 | IO59PDB3V0 |
| P22 | IO58NDB3V0 |
| R1 | NC |
| R2 | IO110PDB6V0 |
| R3 | VCC |
| R4 | IO109NPB6V0 |
| R5 | IO106NDB6V0 |
| R6 | IO106PDB6V0 |
| R7 | GEC0/IO104NPB6V0 |
| R8 | VMV5 |

| FG484 | |
|---|---|
| **Pin Number** | **A3PE600 Function** |
| R9 | VCCIB5 |
| R10 | VCCIB5 |
| R11 | IO84NDB5V0 |
| R12 | IO84PDB5V0 |
| R13 | VCCIB4 |
| R14 | VCCIB4 |
| R15 | VMV3 |
| R16 | VCCPLD |
| R17 | GDB1/IO66PPB3V1 |
| R18 | GDC1/IO65PDB3V1 |
| R19 | IO61NDB3V1 |
| R20 | VCC |
| R21 | IO59NDB3V0 |
| R22 | IO62PDB3V1 |
| T1 | NC |
| T2 | IO110NDB6V0 |
| T3 | NC |
| T4 | IO105PDB6V0 |
| T5 | IO105NDB6V0 |
| T6 | GEC1/IO104PPB6V0 |
| T7 | VCOMPLE |
| T8 | GNDQ |
| T9 | GEA2/IO101PPB5V2 |
| T10 | IO92NDB5V1 |
| T11 | IO90NDB5V1 |
| T12 | IO82NDB5V0 |
| T13 | IO74NDB4V1 |
| T14 | IO74PDB4V1 |
| T15 | GNDQ |
| T16 | VCOMPLD |
| T17 | VJTAG |
| T18 | GDC0/IO65NDB3V1 |
| T19 | GDA1/IO67PDB3V1 |
| T20 | NC |
| T21 | IO64PDB3V1 |
| T22 | IO62NDB3V1 |

| FG484 | |
|---|---|
| **Pin Number** | **A3PE600 Function** |
| U1 | NC |
| U2 | IO107PDB6V0 |
| U3 | IO107NDB6V0 |
| U4 | GEB1/IO103PDB6V0 |
| U5 | GEB0/IO103NDB6V0 |
| U6 | VMV6 |
| U7 | VCCPLE |
| U8 | IO101NPB5V2 |
| U9 | IO95PPB5V1 |
| U10 | IO92PDB5V1 |
| U11 | IO90PDB5V1 |
| U12 | IO82PDB5V0 |
| U13 | IO76NDB4V1 |
| U14 | IO76PDB4V1 |
| U15 | VMV4 |
| U16 | TCK |
| U17 | VPUMP |
| U18 | TRST |
| U19 | GDA0/IO67NDB3V1 |
| U20 | NC |
| U21 | IO64NDB3V1 |
| U22 | IO63PDB3V1 |
| V1 | NC |
| V2 | NC |
| V3 | GND |
| V4 | GEA1/IO102PDB6V0 |
| V5 | GEA0/IO102NDB6V0 |
| V6 | GNDQ |
| V7 | GEC2/IO99PDB5V2 |
| V8 | IO95NPB5V1 |
| V9 | IO91NDB5V1 |
| V10 | IO91PDB5V1 |
| V11 | IO83NDB5V0 |
| V12 | IO83PDB5V0 |
| V13 | IO77NDB4V1 |
| V14 | IO77PDB4V1 |

| FG484 | |
|---|---|
| **Pin Number** | **A3PE600 Function** |
| V15 | IO69NDB4V0 |
| V16 | GDB2/IO69PDB4V0 |
| V17 | TDI |
| V18 | GNDQ |
| V19 | TDO |
| V20 | GND |
| V21 | NC |
| V22 | IO63NDB3V1 |
| W1 | NC |
| W2 | NC |
| W3 | NC |
| W4 | GND |
| W5 | IO100NDB5V2 |
| W6 | GEB2/IO100PDB5V2 |
| W7 | IO99NDB5V2 |
| W8 | IO88NDB5V0 |
| W9 | IO88PDB5V0 |
| W10 | IO89NDB5V0 |
| W11 | IO80NDB4V1 |
| W12 | IO81NDB4V1 |
| W13 | IO81PDB4V1 |
| W14 | IO70NDB4V0 |
| W15 | GDC2/IO70PDB4V0 |
| W16 | IO68NDB4V0 |
| W17 | GDA2/IO68PDB4V0 |
| W18 | TMS |
| W19 | GND |
| W20 | NC |
| W21 | NC |
| W22 | NC |
| Y1 | VCCIB6 |
| Y2 | NC |
| Y3 | NC |
| Y4 | IO98NDB5V2 |
| Y5 | GND |
| Y6 | IO94NDB5V1 |

| FG484 | |
|---|---|
| **Pin Number** | **A3PE600 Function** |
| Y7 | IO94PDB5V1 |
| Y8 | VCC |
| Y9 | VCC |
| Y10 | IO89PDB5V0 |
| Y11 | IO80PDB4V1 |
| Y12 | IO78NPB4V1 |
| Y13 | NC |
| Y14 | VCC |
| Y15 | VCC |
| Y16 | NC |
| Y17 | NC |
| Y18 | GND |
| Y19 | NC |
| Y20 | NC |
| Y21 | NC |
| Y22 | VCCIB3 |

| FG676 | |
|---|---|
| **Pin Number** | **A3PE1500 Function** |
| R21 | IO89NDB3V0 |
| R22 | GCB2/IO89PDB3V0 |
| R23 | IO90NDB3V0 |
| R24 | GCC2/IO90PDB3V0 |
| R25 | IO91PDB3V0 |
| R26 | IO91NDB3V0 |
| T1 | IO186PDB6V2 |
| T2 | IO185NDB6V2 |
| T3 | GNDQ |
| T4 | IO180PDB6V1 |
| T5 | IO180NDB6V1 |
| T6 | IO188NDB6V2 |
| T7 | GFB2/IO188PDB6V2 |
| T8 | VCCIB6 |
| T9 | VCC |
| T10 | GND |
| T11 | GND |
| T12 | GND |
| T13 | GND |
| T14 | GND |
| T15 | GND |
| T16 | GND |
| T17 | GND |
| T18 | VCC |
| T19 | VCCIB3 |
| T20 | IO99PDB3V1 |
| T21 | IO99NDB3V1 |
| T22 | IO97PDB3V1 |
| T23 | IO97NDB3V1 |
| T24 | GNDQ |
| T25 | IO93PPB3V0 |
| T26 | NC |
| U1 | IO186NDB6V2 |
| U2 | IO184NDB6V2 |
| U3 | IO184PDB6V2 |
| U4 | IO182NDB6V1 |

| FG676 | |
|---|---|
| **Pin Number** | **A3PE1500 Function** |
| U5 | IO182PDB6V1 |
| U6 | IO178PDB6V1 |
| U7 | IO178NDB6V1 |
| U8 | VCCIB6 |
| U9 | VCC |
| U10 | GND |
| U11 | GND |
| U12 | GND |
| U13 | GND |
| U14 | GND |
| U15 | GND |
| U16 | GND |
| U17 | GND |
| U18 | VCC |
| U19 | VCCIB3 |
| U20 | NC |
| U21 | IO101NDB3V1 |
| U22 | IO101PDB3V1 |
| U23 | IO92NDB3V0 |
| U24 | IO92PDB3V0 |
| U25 | IO95PDB3V1 |
| U26 | IO93NPB3V0 |
| V1 | IO183PDB6V2 |
| V2 | IO183NDB6V2 |
| V3 | VMV6 |
| V4 | IO181PDB6V1 |
| V5 | IO181NDB6V1 |
| V6 | IO176PDB6V1 |
| V7 | IO176NDB6V1 |
| V8 | VCCIB6 |
| V9 | VCC |
| V10 | VCC |
| V11 | VCC |
| V12 | VCC |
| V13 | VCC |
| V14 | VCC |

| FG676 | |
|---|---|
| **Pin Number** | **A3PE1500 Function** |
| V15 | VCC |
| V16 | VCC |
| V17 | VCC |
| V18 | VCC |
| V19 | VCCIB3 |
| V20 | IO107PDB3V2 |
| V21 | IO107NDB3V2 |
| V22 | IO103NDB3V2 |
| V23 | IO103PDB3V2 |
| V24 | VMV3 |
| V25 | IO95NDB3V1 |
| V26 | IO94PDB3V0 |
| W1 | IO179NDB6V1 |
| W2 | IO179PDB6V1 |
| W3 | IO177NDB6V1 |
| W4 | IO177PDB6V1 |
| W5 | IO172PDB6V0 |
| W6 | IO172NDB6V0 |
| W7 | VCC |
| W8 | VCC |
| W9 | VCCIB5 |
| W10 | VCCIB5 |
| W11 | VCCIB5 |
| W12 | VCCIB5 |
| W13 | VCCIB5 |
| W14 | VCCIB4 |
| W15 | VCCIB4 |
| W16 | VCCIB4 |
| W17 | VCCIB4 |
| W18 | VCCIB4 |
| W19 | VCC |
| W20 | VCCIB3 |
| W21 | GDB0/IO109NDB3V2 |
| W22 | GDB1/IO109PDB3V2 |
| W23 | IO105NDB3V2 |
| W24 | IO105PDB3V2 |

| Revision | Changes | Page |
|---|---|---|
| **Revision 9 (Aug 2009)**<br>Product Brief v1.2 | All references to speed grade –F have been removed from this document. | N/A |
| | The "Pro I/Os with Advanced I/O Standards" section was revised to add definitions of hot-swap and cold-sparing. | 1-6 |
| DC and Switching Characteristics v1.3 | 3.3 V LVCMOS and 1.2 V LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained 3.3 V LVCMOS and 1.2 V LVCMOS data. | N/A |
| | IIL and IIH input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables. | N/A |
| | –F was removed from the datasheet. The speed grade is no longer supported. | N/A |
| | In the Table 2-2 • Recommended Operating Conditions[1] "3.0 V DC supply voltage" and note 4 are new. | 2-2 |
| | The Table 2-4 • Overshoot and Undershoot Limits[1] table was updated. | 2-3 |
| | The Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays table was updated. | 2-5 |
| | There are new parameters and data was updated in the Table 2-99 • RAM4K9 table. | 2-76 |
| | There are new parameters and data was updated in the Table 2-100 • RAM512X18 table. | 2-77 |
| **Revision 8 (Feb 2008)**<br>Product Brief v1.1 | Table 1-2 • ProASIC3E FPGAs Package Sizes Dimensions is new. | 1-II |
| **Revision 7 (Jun 2008)**<br>DC and Switching Characteristics v1.2 | The title of Table 2-4 • Overshoot and Undershoot Limits[1] was modified to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted. | 2-3 |
| | Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels was updated. | 2-50 |
| **Revision 6 (Jun 2008)** | The A3PE600 "FG484" table was missing G22. The pin and its function were added to the table. | 4-27 |
| **Revision 5 (Jun 2008)**<br>Packaging v1.4 | The naming conventions changed for the following pins in the "FG484" for the A3PE600:<br>**Pin Number** **New Function Name**<br>J19 IO45PPB2V1<br>K20 IO45NPB2V1<br>M2 IO114NPB6V1<br>N1 IO114PPB6V1<br>N4 GFC2/IO115PPB6V1<br>P3 IO115NPB6V1 | 4-22 |
| **Revision 4 (Apr 2008)**<br>Product Brief v1.0 | The product brief portion of the datasheet was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview. | N/A |
| Packaging v1.3 | The "FG324" package diagram was replaced. | 4-12 |