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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	516096
Number of I/O	221
Number of Gates	300000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	324-BGA
Supplier Device Package	324-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3pe3000-1fgg324

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Temperature Grade Offerings

Package	A3PE600	A3PE1500	A3PE3000
Cortex-M1 Devices		M1A3PE1500	M1A3PE3000
PQ208	C, I	C, I	C, I
FG256	C, I	-	-
FG324	-	_	C, I
FG484	C, I	C, I	C, I
FG676	-	C, I	_
FG896	-	-	C, I

Note: C = Commercial temperature range: 0°C to 70°C ambient temperature<math>I = Industrial temperature range: -40°C to 85°C ambient temperature

Speed Grade and Temperature Grade Matrix

Temperature Grade	Std.	-1	-2
C ¹	\checkmark	\checkmark	\checkmark
2	\checkmark	\checkmark	\checkmark

Notes:

1. C = Commercial temperature range: 0°C to 70°C ambient temperature

2. I = Industrial temperature range: -40°C to 85°C ambient temperature

References made to ProASIC3E devices also apply to ARM-enabled ProASIC3E devices. The ARM-enabled part numbers start with M1 (Cortex-M1).

Contact your local Microsemi SoC Products Group representative for device availability: www.microsemi.com/index.php?option=com_content&id=135&lang=en&view=article.



rom file Save to file			Show BSR D
Port Name	Macro Cell	Pin Number	1/O State (Output Only)
BIST	ADLIB:INBUF	T2	1
BYPASS_IO	ADLIB:INBUF	K1	1
CLK	ADLIB:INBUF	B1	1
ENOUT	ADLIB:INBUF	J16	1
LED	ADLIB:OUTBUF	M3	0
MONITOR[0]	ADLIB:OUTBUF	B5	0
MONITOR[1]	ADLIB:OUTBUF	C7	Z
MONITOR[2]	ADLIB:OUTBUF	D9	Z
MONITOR(3)	ADLIB:OUTBUF	D7	Z
MONITOR[4]	ADLIB:OUTBUF	A11	Z
OEa	ADLIB:INBUF	E4	Z
ОЕЬ	ADLIB:INBUF	F1	Z
OSC_EN	ADLIB:INBUF	К3	Z
PAD[10]	ADLIB:BIBUF_LVCMOS33U	M8	Z
PAD[11]	ADLIB:BIBUF_LVCMOS33D	R7	Z
PAD[12]	ADLIB:BIBUF_LVCMOS33U	D11	Z
PAD[13]	ADLIB:BIBUF_LVCMOS33D	C12	Z
PAD[14]	ADLIB:BIBUF_LVCMOS33U	R6	Z
			-

Figure 1-3 • I/O States During Programming Window

- 6. Click OK to return to the FlashPoint Programming File Generator window.
 - I/O States during programming are saved to the ADB and resulting programming files after completing programming file generation.

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ProASIC3E DC and Switching Characteristics

Symbol	Paran	neter	Commercial	Industrial	Units
T _A	Ambient temperature		0 to +70	-40 to +85	°C
TJ	Junction temperature		0 to +85	-40 to +100	°C
VCC	1.5 V DC core supply volta	ge	1.425 to 1.575	1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage	Programming Mode ²	3.15 to 3.45	3.15 to 3.45	V
		Operation ³	0 to 3.6	0 to 3.6	V
VCCPLL	Analog power supply (PLL))	1.425 to 1.575	1.425 to 1.575	V
VCCI and VMV ⁴	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	3.0 V DC supply voltage ⁵		2.7 to 3.6	2.7 to 3.6	V
	LVDS/B-LVDS/M-LVDS diff	ferential I/O	2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Table 2-2 • Recommended Operating Conditions¹

Notes:

1. All parameters representing voltages are measured with respect to GND unless otherwise specified.

2. The programming temperature range supported is $T_{ambient} = 0^{\circ}C$ to $85^{\circ}C$.

3. VPUMP can be left floating during normal operation (not programming mode).

- 4. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-13 on page 2-16. VMV and VCCI should be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information.
- 5. To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microsemi recommends that the user follow best design practices using Microsemi's timing and power simulation tools.
- 6. 3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.

Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature ¹

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T _{STG} (°C) ²	Maximum Operating Junction Temperature T _J (°C) ²
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. This is a stress rating only; functional operation at any condition other than those indicated is not implied.

2. These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.

	VMV (V)	Static Power PDC2 (mW) ¹	Dynamic Power PAC9 (µW/MHz) ²
HSTL (I)	1.5	0.17	2.03
HSTL (II)	1.5	0.17	2.03
SSTL2 (I)	2.5	1.38	4.48
SSTL2 (II)	2.5	1.38	4.48
SSTL3 (I)	3.3	3.21	9.26
SSTL3 (II)	3.3	3.21	9.26
Differential			-
LVDS/B-LVDS/M-LVDS	2.5	2.26	1.50
LVPECL	3.3	5.71	2.17

Table 2-8 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings (continued)

Notes:

1. PDC2 is the static power (where applicable) measured on VMV.

2. PAC9 is the total dynamic power measured on VCC and VMV.

3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.

Table 2-9 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings ¹

	C _{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW) ²	Dynamic Power PAC10 (µW/MHz) ³
Single-Ended			•	•
3.3 V LVTTL/LVCMOS	35	3.3	-	474.70
3.3 V LVTTL/LVCMOS Wide Range ⁴	35	3.3	-	474.70
2.5 V LVCMOS	35	2.5	-	270.73
1.8 V LVCMOS	35	1.8	-	151.78
1.5 V LVCMOS (JESD8-11)	35	1.5	-	104.55
3.3 V PCI	10	3.3	-	204.61
3.3 V PCI-X	10	3.3	-	204.61
Voltage-Referenced				
3.3 V GTL	10	3.3	-	24.08
2.5 V GTL	10	2.5	-	13.52
3.3 V GTL+	10	3.3	-	24.10
2.5 V GTL+	10	2.5	-	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.22
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.60

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.

2. PDC3 is the static power (where applicable) measured on VCCI.

3. PAC10 is the total dynamic power measured on VCC and VCCI.

4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

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ProASIC3E DC and Switching Characteristics

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

2.5 V LVCMOS	v	ΊL	v	н	VOL	VOH	IOL	юн	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max., V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
4 mA	-0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
8 mA	-0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	-0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	-0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	-0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10

Table 2-33 • Minimum and Maximum DC Input and Output Levels

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.

Test Point
Datapath
$$\xrightarrow{1}{1}$$
 35 pF
 $R = 1 k$
Test Point
Enable Path $\xrightarrow{1}{1}$ R to VCCI for $t_{LZ} / t_{ZL} / t_{ZLS}$
R to GND for $t_{HZ} / t_{ZH} / t_{ZHS}$
 $35 pF$ for $t_{ZH} / t_{ZHS} / t_{ZL} / t_{ZLS}$
 $35 pF$ for $t_{HZ} / t_{ZH} / t_{ZLS}$

Figure 2-8 • AC Loading

Table 2-34 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	2.5	1.2	_	35

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

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ProASIC3E DC and Switching Characteristics

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for generalpurpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

1.5 V LVCMOS		VIL	VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	-0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10
6 mA	-0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	6	6	39	32	10	10
8 mA	-0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	8	8	55	66	10	10
12 mA	-0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12	55	66	10	10

Table 2-41 • Minimum and Maximum DC Input and Output Levels

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V< VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.

Test Point
Datapath
$$\downarrow$$
 35 pF
$$R = 1 k$$
Test Point
Enable Path \downarrow

$$R to VCCI for t_{LZ} / t_{ZL} / t_{ZLS}$$

$$R to GND for t_{HZ} / t_{ZH} / t_{ZHS} / t_{ZL} / t_{ZLS}$$

$$35 pF for t_{ZH} / t_{ZHS} / t_{ZL} / t_{ZLS}$$

Figure 2-10 • AC Loading

Table 2-42 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	1.5	0.75	_	35

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Voltage-Referenced I/O Characteristics

3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-48 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL	VIL		VIH		VOL	VOH	IOL	ЮН	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA²	μA²
20 mA ³	-0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	-	20	20	181	268	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

2. Currents are measured at 85°C junction temperature.

3. Output drive strength is below JEDEC specification.



Figure 2-12 • AC Loading

Table 2-49 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.05	VREF + 0.05	0.8	0.8	1.2	10

Note: **Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-50 • 3.3 V GTL

```
Commercial-Case Conditions: T_J = 70^{\circ}C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V VREF = 0.8 V
```

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.60	2.08	0.04	2.93	0.43	2.04	2.08			4.27	4.31	ns
-1	0.51	1.77	0.04	2.50	0.36	1.73	1.77			3.63	3.67	ns
-2	0.45	1.55	0.03	2.19	0.32	1.52	1.55			3.19	3.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

|--|

HSTL Class I		VIL	VIH	VIH		VOH	IOL	ЮН	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA²	μA²
8 mA	-0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI - 0.4	8	8	39	32	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

2. Currents are measured at 85°C junction temperature.



Figure 2-16 • AC Loading

Table 2-61 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: **Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-62 • HSTL Class I

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = .4 V, VREF = 0.75 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.66	3.18	0.04	2.12	0.43	3.24	3.14			5.47	5.38	ns
-1	0.56	2.70	0.04	1.81	0.36	2.75	2.67			4.66	4.58	ns
-2	0.49	2.37	0.03	1.59	0.32	2.42	2.35			4.09	4.02	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

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ProASIC3E DC and Switching Characteristics

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-75 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class II	STL3 Class II VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA²	μA²
21 mA	-0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21	109	103	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

2. Currents are measured at 85°C junction temperature.



Figure 2-21 • AC Loading

Table 2-76 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-77 • SSTL3 Class II

```
Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 1.5 V
```

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.66	2.07	0.04	1.25	0.43	2.10	1.67			4.34	3.91	ns
-1	0.56	1.76	0.04	1.06	0.36	1.79	1.42			3.69	3.32	ns
-2	0.49	1.54	0.03	0.93	0.32	1.57	1.25			3.24	2.92	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Timing Characteristics

Table 2-80 • LVDS

Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	Units
Std.	0.66	1.87	0.04	1.82	ns
-1	0.56	1.59	0.04	1.55	ns
-2	0.49	1.40	0.03	1.36	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-23. The input and output buffer delays are available in the LVDS section in Table 2-80.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: $R_S = 60 \Omega$ and $R_T = 70 \Omega$, given $Z_0 = 50 \Omega$ (2") and $Z_{stub} = 50 \Omega$ (~1.5").



Figure 2-23 • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers

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ProASIC3E DC and Switching Characteristics

Table 2-85 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t _{oclkq}	Clock-to-Q of the Output Data Register	HH, DOUT
tosud	Data Setup Time for the Output Data Register	FF, HH
t _{OHD}	Data Hold Time for the Output Data Register	FF, HH
tosue	Enable Setup Time for the Output Data Register	GG, HH
t _{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t _{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
t _{OREMCLR}	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
t _{ORECCLR}	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t _{oeclkq}	Clock-to-Q of the Output Enable Register	HH, EOUT
t _{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t _{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t _{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t _{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
t _{OECLR2Q}	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
t _{OEREMCLR}	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
t _{OERECCLR}	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t _{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t _{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t _{IHD}	Data Hold Time for the Input Data Register	CC, AA
t _{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t _{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t _{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
t _{IREMCLR}	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
t _{IRECCLR}	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

Note: *See Figure 2-26 on page 2-55 for more information.



Figure 2-35 • Timing Model and Waveforms

Global Resource Characteristics

A3PE600 Clock Tree Topology

Clock delays are device-specific. Figure 2-38 is an example of a global tree used for clock routing. The global tree presented in Figure 2-38 is driven by a CCC located on the west side of the A3PE600 device. It is used to drive all D-flip-flops in the device.



Figure 2-38 • Example of Global Tree Use in an A3PE600 Device for Clock Routing

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-70. Table 2-95 on page 2-69, Table 2-96 on page 2-69, and Table 2-97 on page 2-69 present minimum and maximum global clock delays within the device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Waveforms







Figure 2-42 • RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.



Figure 2-45 • RAM Reset. Applicable to Both RAM4K9 and RAM512x18.



FG256



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/products/fpga-soc/solutions*.

🌜 Microsemi.

Package Pin Assignments

	FG676	FG676		FG676		
Pin Number	A3PE1500 Function	Pin Number	A3PE1500 Function	Pin Number	A3PE1500 Function	
AD5	IO162PDB5V3	AE15	IO134NDB4V2	AF25	GND	
AD6	IO160NDB5V3	AE16	IO133NDB4V2	AF26	GND	
AD7	IO161NDB5V3	AE17	IO127NDB4V2	B1	GND	
AD8	IO154NDB5V2	AE18	IO130NDB4V2	B2	GND	
AD9	IO148PDB5V1	AE19	IO126NDB4V1	B3	GND	
AD10	IO151PDB5V2	AE20	IO124NDB4V1	B4	GND	
AD11	IO144PDB5V1	AE21	IO120NDB4V1	B5	IO06PDB0V0	
AD12	IO140PDB5V0	AE22	IO116PDB4V0	B6	IO04NDB0V0	
AD13	IO143PDB5V1	AE23	GDC2/IO113PDB4V0	B7	IO07NDB0V0	
AD14	IO141PDB5V0	AE24	GDA2/IO111PDB4V0	B8	IO11NDB0V1	
AD15	IO134PDB4V2	AE25	GND	B9	IO10NDB0V1	
AD16	IO133PDB4V2	AE26	GND	B10	IO16NDB0V2	
AD17	IO127PDB4V2	AF1	GND	B11	IO20NDB0V2	
AD18	IO130PDB4V2	AF2	GND	B12	IO24NDB0V3	
AD19	IO126PDB4V1	AF3	GND	B13	IO23NDB0V2	
AD20	IO124PDB4V1	AF4	GND	B14	IO28NDB0V3	
AD21	IO120PDB4V1	AF5	IO158NPB5V2	B15	IO31NDB0V3	
AD22	IO114NPB4V0	AF6	IO157NPB5V2	B16	IO32PDB1V0	
AD23	TDI	AF7	IO152NPB5V2	B17	IO36PDB1V0	
AD24	GNDQ	AF8	IO146NDB5V1	B18	IO37PDB1V0	
AD25	GDA0/IO110NDB3V2	AF9	IO146PDB5V1	B19	IO42NPB1V1	
AD26	GDA1/IO110PDB3V2	AF10	IO149NDB5V1	B20	IO41NDB1V1	
AE1	GND	AF11	IO149PDB5V1	B21	IO44NDB1V1	
AE2	GND	AF12	IO145NDB5V1	B22	IO49NDB1V2	
AE3	GND	AF13	IO145PDB5V1	B23	IO50NDB1V2	
AE4	IO164NDB5V3	AF14	IO136NDB5V0	B24	GBC0/IO55NDB1V3	
AE5	IO162NDB5V3	AF15	IO136PDB5V0	B25	GND	
AE6	IO158PPB5V2	AF16	IO131NDB4V2	B26	GND	
AE7	IO157PPB5V2	AF17	IO131PDB4V2	C1	GND	
AE8	IO152PPB5V2	AF18	IO128NDB4V2	C2	GND	
AE9	IO148NDB5V1	AF19	IO128PDB4V2	C3	GND	
AE10	IO151NDB5V2	AF20	IO122NDB4V1	C4	GND	
AE11	IO144NDB5V1	AF21	IO122PDB4V1	C5	GAA2/IO221PDB7V3	
AE12	IO140NDB5V0	AF22	IO116NDB4V0	C6	IO04PDB0V0	
AE13	IO143NDB5V1	AF23	IO113NDB4V0	C7	IO07PDB0V0	
AE14	IO141NDB5V0	AF24	IO111NDB4V0	C8	IO11PDB0V1	



Package Pin Assignments

FG896		FG896		FG896		
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	
T11	VCC	U17	GND	V23	IO128NDB3V1	
T12	GND	U18	GND	V24	IO132PDB3V2	
T13	GND	U19	GND	V25	IO130PPB3V2	
T14	GND	U20	VCC	V26	IO126NDB3V1	
T15	GND	U21	VCCIB3	V27	IO129NDB3V1	
T16	GND	U22	IO120PDB3V0	V28	IO127NDB3V1	
T17	GND	U23	IO128PDB3V1	V29	IO125NDB3V1	
T18	GND	U24	IO124PDB3V1	V30	IO123PDB3V1	
T19	GND	U25	IO124NDB3V1	W1	IO266NDB6V4	
T20	VCC	U26	IO126PDB3V1	W2	IO262NDB6V3	
T21	VCCIB3	U27	IO129PDB3V1	W3	IO260NDB6V3	
T22	IO109NPB2V3	U28	IO127PDB3V1	W4	IO252NDB6V2	
T23	IO116NDB3V0	U29	IO125PDB3V1	W5	IO251NDB6V2	
T24	IO118NDB3V0	U30	IO121NDB3V0	W6	IO251PDB6V2	
T25	IO122NPB3V1	V1	IO268NDB6V4	W7	IO255NDB6V2	
T26	GCA1/IO114PPB3V0	V2	IO262PDB6V3	W8	IO249PPB6V1	
T27	GCB0/IO113NPB2V3	V3	IO260PDB6V3	W9	IO253PDB6V2	
T28	GCA2/IO115PPB3V0	V4	IO252PDB6V2	W10	VCCIB6	
T29	VCCPLC	V5	IO257NPB6V2	W11	VCC	
T30	IO121PDB3V0	V6	IO261NPB6V3	W12	GND	
U1	IO268PDB6V4	V7	IO255PDB6V2	W13	GND	
U2	IO264NDB6V3	V8	IO259PDB6V3	W14	GND	
U3	IO264PDB6V3	V9	IO259NDB6V3	W15	GND	
U4	IO258PDB6V3	V10	VCCIB6	W16	GND	
U5	IO258NDB6V3	V11	VCC	W17	GND	
U6	IO257PPB6V2	V12	GND	W18	GND	
U7	IO261PPB6V3	V13	GND	W19	GND	
U8	IO265NDB6V3	V14	GND	W20	VCC	
U9	IO263NDB6V3	V15	GND	W21	VCCIB3	
U10	VCCIB6	V16	GND	W22	IO134PDB3V2	
U11	VCC	V17	GND	W23	IO138PDB3V3	
U12	GND	V18	GND	W24	IO132NDB3V2	
U13	GND	V19	GND	W25	IO136NPB3V2	
U14	GND	V20	VCC	W26	IO130NPB3V2	
U15	GND	V21	VCCIB3	W27	IO141PDB3V3	
U16	GND	V22	IO120NDB3V0	W28	IO135PDB3V2	



FG896				
Pin Number	A3PE3000 Function			
W29	IO131PDB3V2			
W30	IO123NDB3V1			
Y1	IO266PDB6V4			
Y2	IO250PDB6V2			
Y3	IO250NDB6V2			
Y4	IO246PDB6V1			
Y5	IO247NDB6V1			
Y6	IO247PDB6V1			
Y7	IO249NPB6V1			
Y8	IO245PDB6V1			
Y9	IO253NDB6V2			
Y10	GEB0/IO235NPB6V0			
Y11	VCC			
Y12	VCC			
Y13	VCC			
Y14	VCC			
Y15	VCC			
Y16	VCC			
Y17	VCC			
Y18	VCC			
Y19	VCC			
Y20	VCC			
Y21	IO142PPB3V3			
Y22	IO134NDB3V2			
Y23	IO138NDB3V3			
Y24	IO140NDB3V3			
Y25	IO140PDB3V3			
Y26	IO136PPB3V2			
Y27	IO141NDB3V3			
Y28	IO135NDB3V2			
Y29	IO131NDB3V2			
Y30	IO133PDB3V2			



Revision	Changes				
Revision 9 (Aug 2009)	All references to speed grade –F have been removed from this document.		N/A		
Product Brief v1.2					
	The "Pro I/Os with Advance definitions of hot-swap and co	ed I/O Standards" section was revised to add Id-sparing.	1-6		
DC and Switching Characteristics v1.3	$3.3~\rm V$ LVCMOS and 1.2 V LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained 3.3 V LVCMOS and 1.2 V LVCMOS data.				
	IIL and IIH input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables.				
	-F was removed from the datasheet. The speed grade is no longer supported.				
	In the Table 2-2 • Recommended Operating Conditions ¹ "3.0 V DC su voltage" and note 4 are new.		2-2		
	The Table 2-4 • Overshoot and Undershoot Limits ¹ table was updated.				
	The Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays table was updated.				
	There are new parameters and data was updated in the Table 2-99 • RAM4K9 table.				
	There are new parameters and data was updated in the Table 2-100 • RAM512X18 table.				
Revision 8 (Feb 2008)	Table 1-2 • ProASIC3E FPGAs Package Sizes Dimensions is new.				
Product Brief v1.1					
Revision 7 (Jun 2008) DC and Switching	The title of Table 2-4 • Overshoot and Undershoot Limits ¹ was modified to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles " Table note 3 was deleted				
	Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels was updated.				
Revision 6 (Jun 2008)	The A3PE600 "FG484" table was missing G22. The pin and its function were added to the table.		4-27		
Revision 5 (Jun 2008) Packaging v1.4	The naming conventions changed for the following pins in the "FG484" for the A3PE600:		4-22		
	Pin Number	New Function Name			
	J19	IO45PPB2V1			
	K20	IO45NPB2V1			
	M2	IO114NPB6V1			
	N1	IO114PPB6V1			
	N4	GFC2/IO115PPB6V1			
	P3	IO115NPB6V1			
Revision 4 (Apr 2008) Product Brief v1.0	The product brief portion of the datasheet was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.				
Packaging v1.3	The "FG324" package diagram was replaced.				