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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	
Total RAM Bits	516096
Number of I/O	620
Number of Gates	300000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3pe3000-1fgg896

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Temperature Grade Offerings

Package	A3PE600	A3PE1500	A3PE3000
Cortex-M1 Devices		M1A3PE1500	M1A3PE3000
PQ208	C, I	C, I	C, I
FG256	C, I	-	-
FG324	-	_	C, I
FG484	C, I	C, I	C, I
FG676	-	C, I	_
FG896	-	-	C, I

Note: C = Commercial temperature range: 0°C to 70°C ambient temperature<math>I = Industrial temperature range: -40°C to 85°C ambient temperature

Speed Grade and Temperature Grade Matrix

Temperature Grade	Std.	-1	-2
C ¹	\checkmark	\checkmark	\checkmark
2	\checkmark	\checkmark	\checkmark

Notes:

1. C = Commercial temperature range: 0°C to 70°C ambient temperature

2. I = Industrial temperature range: -40°C to 85°C ambient temperature

References made to ProASIC3E devices also apply to ARM-enabled ProASIC3E devices. The ARM-enabled part numbers start with M1 (Cortex-M1).

Contact your local Microsemi SoC Products Group representative for device availability: www.microsemi.com/index.php?option=com_content&id=135&lang=en&view=article.



ProASIC3E Device Family Overview

Pro I/Os with Advanced I/O Standards

The ProASIC3E family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). ProASIC3E FPGAs support 19 different I/O standards, including single-ended, differential, and voltage-referenced. The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported. Each I/O bank is subdivided into VREF minibanks, which are used by voltage-referenced I/Os. VREF minibanks contain 8 to 18 I/Os. All the I/Os in a given minibank share a common VREF line. Therefore, if any I/O in a given VREF minibank is configured as a VREF pin, the remaining I/Os in that minibank will be able to use that reference voltage.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications (e.g., PCI 66 MHz, bidirectional SSTL 2 and 3, Class I and II)
- Double-Data-Rate applications (e.g., DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications, and DDR 200 MHz SRAM using bidirectional HSTL Class II)

ProASIC3E banks support M-LVDS with 20 multi-drop points.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

- Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.
 - 1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
 - From the FlashPro GUI, click PDB Configuration. A FlashPoint Programming File Generator window appears.
 - 3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
 - 4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-3 on page 1-7).
 - Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

1 - I/O is set to drive out logic High

0 - I/O is set to drive out logic Low

Last Known State - I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

Z -Tri-State: I/O is tristated

VCCI and VMV	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle ²	Maximum Overshoot/ Undershoot ²
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Table 2-4 • Overshoot and Undershoot Limits ¹

Notes:

1. Based on reliability requirements at 85°C.

2. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.

3. This table does not provide PCI overshoot/undershoot limits.

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC[®]3E device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4.

There are five regions to consider during power-up.

ProASIC3E I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 on page 2-4).

- 2. VCCI > VCC 0.75 V (typical)
- 3. Chip is in the operating mode.

VCCI Trip Point:

Ramping up: 0.6 V < trip_point_up < 1.2 V Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC Trip Point:

Ramping up: 0.6 V < trip_point_up < 1.1 V Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.



Table 2-17 • Summary of I/O Timing Characteristics—Software Default Settings -2 Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option) ¹	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t _{bour} (ns)	t _{DP} (ns)	t _{DIN} (ns)	t _{PY} (ns)	t _{PYS} (ns)	t _{EOUT} (ns)	t _{ZL} (ns)	t _{ZH} (ns)	t _{LZ} (ns)	t _{HZ} (ns)	t _{ZLS} (ns)	t _{ZHS} (ns)
3.3 V LVTTL / 3.3 V LVCMOS	12	12	High	35	-	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81
3.3 V LVCMOS Wide Range ²	100 µA	12	High	35	-	0.49	4.24	0.03	1.36	1.78	0.32	4.24	3.25	3.78	4.17	6.77	5.79
2.5 V LVCMOS	12	12	High	35	_	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28
1.8 V LVCMOS	12	12	High	35	_	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98
1.5 V LVCMOS	12	12	High	35	_	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37
3.3 V PCI	Per PCI spec	-	High	10	25 ³	0.49	2.09	0.03	0.78	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16
3.3 V PCI-X	Per PCI-X spec	-	High	10	25 ³	0.49	2.09	0.03	0.78	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16
3.3 V GTL	20 ⁴	-	High	10	25	0.45	1.55	0.03	2.19	-	0.32	1.52	1.55	-	-	3.19	3.22
2.5 V GTL	20 ⁴	-	High	10	25	0.45	1.59	0.03	1.83	-	0.32	1.61	1.59	-	-	3.28	3.26
3.3 V GTL+	35	-	High	10	25	0.45	1.53	0.03	1.19	-	0.32	1.56	1.53	-	-	3.23	3.20
2.5 V GTL+	33	-	High	10	25	0.45	1.65	0.03	1.13	-	0.32	1.68	1.57	-	-	3.35	3.24
HSTL (I)	8	-	High	20	50	0.49	2.37	0.03	1.59	-	0.32	2.42	2.35	-	-	4.09	4.02
HSTL (II)	15 ⁴	-	High	20	25	0.49	2.26	0.03	1.59	-	0.32	2.30	2.03	-	-	3.97	3.70
SSTL2 (I)	15	-	High	30	50	0.49	1.59	0.03	1.00	-	0.32	1.62	1.38	-	-	3.29	3.05
SSTL2 (II)	18	-	High	30	25	0.49	1.62	0.03	1.00	-	0.32	1.65	1.32	-	-	3.32	2.99
SSTL3 (I)	14	_	High	30	50	0.49	1.72	0.03	0.93	-	0.32	1.75	1.37	-	-	3.42	3.04
SSTL3 (II)	21	-	High	30	25	0.49	1.54	0.03	0.93	-	0.32	1.57	1.25	-	-	3.24	2.92
LVDS/B-LVDS/ M-LVDS	24	-	High	-	-	0.49	1.40	0.03	1.36	-	_	-	_	_	_	—	_
LVPECL	24	_	High	_	_	0.49	1.36	0.03	1.22	-	_	-	-	-	-	—	-

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100 \ \mu$ A. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2. All LVCMOS 3.3 V software macros support LVCMOS 3.3V wide range as specified in the JESD8b specification.

3. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-38 for connectivity. This resistor is not required during normal operation.

4. Output drive strength is below JEDEC specification.

5. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5.

static Microsemi.

ProASIC3E DC and Switching Characteristics

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTL support.

3.3 V LVTTL / 3.3 V LVCMOS	v	ΊL	v	н	VOL	VОН	IOL	юн	IOSL	IOSH	IIL¹	IIH ²
Drive Strength	Min. V	Max. V	Min., V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	-0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	-0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	-0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Table 2-25 • Minimum and Maximum DC Input and Output Levels

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V< VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN< VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.



Figure 2-6 • AC Loading

Table 2-26 • 3.3 V LVTTL / 3.3 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	3.3	1.4	-	35

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

3.3 V LVCMOS Wide Range

3.3 V LVCMOS Wide Range	Equivalent Software Default Drive	v	IL	v	Ŧ	VOL	VOH	IOL	юн	IOSL	IOSH	IIL ²	IIH ³
Drive Strength	Strength Option ¹	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	μA	μA	Max. mA ⁴	Max. mA ⁴	μA ⁵	μA ⁵
100 µA	2 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	27	25	10	10
100 µA	4 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	27	25	10	10
100 µA	6 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	54	51	10	10
100 µA	8 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	54	51	10	10
100 µA	12 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	109	103	10	10
100 µA	16 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	127	132	10	10
100 µA	24 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	181	268	10	10

Table 2-29 • Minimum and Maximum DC Input and Output Levels

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

3. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN< VCCI. Input current is larger when operating outside recommended ranges.

4. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

5. Currents are measured at 85°C junction temperature.

6. Software default selection highlighted in gray.



Figure 2-7 • AC Loading

Table 2-30 • 3.3 V LVCMOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	3.3	1.4	_	35

Note: **Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

1.8 V LVCMOS

Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

1.8 V LVCMOS		VIL	VIH		VOL	VOH	IOL	ЮН	IOSL	IOSH	IIL¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	2	2	11	9	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	4	4	22	17	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	6	6	44	35	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	8	8	51	45	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	12	12	74	91	10	10
16 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	16	16	74	91	10	10

Table 2-37 • Minimum and Maximum DC Input and Output Levels

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

- 4. Currents are measured at 85°C junction temperature.
- 5. Software default selection highlighted in gray.

Figure 2-9 • AC Loading

Table 2-38 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	1.8	0.9	_	35

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

ProASIC3E DC and Switching Characteristics

Timing Characteristics

Table 2-39 • 1.8 V LVCMOS High Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive	Speed													
Strength	Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
2 mA	Std.	0.66	12.10	0.04	1.45	1.91	0.43	9.59	12.10	2.78	1.64	11.83	14.34	ns
	-1	0.56	10.30	0.04	1.23	1.62	0.36	8.16	10.30	2.37	1.39	10.06	12.20	ns
	-2	0.49	9.04	0.03	1.08	1.42	0.32	7.16	9.04	2.08	1.22	8.83	10.71	ns
4 mA	Std.	0.66	7.05	0.04	1.45	1.91	0.43	6.20	7.05	3.25	2.86	8.44	9.29	ns
	-1	0.56	6.00	0.04	1.23	1.62	0.36	5.28	6.00	2.76	2.44	7.18	7.90	ns
	-2	0.49	5.27	0.03	1.08	1.42	0.32	4.63	5.27	2.43	2.14	6.30	6.94	ns
6 mA	Std.	0.66	4.52	0.04	1.45	1.91	0.43	4.47	4.52	3.57	3.47	6.70	6.76	ns
	-1	0.56	3.85	0.04	1.23	1.62	0.36	3.80	3.85	3.04	2.95	5.70	5.75	ns
	-2	0.49	3.38	0.03	1.08	1.42	0.32	3.33	3.38	2.66	2.59	5.00	5.05	ns
8 mA	Std.	0.66	4.12	0.04	1.45	1.91	0.43	4.20	3.99	3.63	3.62	6.43	6.23	ns
	-1	0.56	3.51	0.04	1.23	1.62	0.36	3.57	3.40	3.09	3.08	5.47	5.30	ns
	-2	0.49	3.08	0.03	1.08	1.42	0.32	3.14	2.98	2.71	2.71	4.81	4.65	ns
12 mA	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	-1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	-2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns
16 mA	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	-1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	-2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

ProASIC3E DC and Switching Characteristics

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-51 • Minimum and Maximum DC Input and Output Levels

2.5 GTL	.5 GTL VIL		VIL VIH		VOL	VOH	IOL	ЮН	IOSL	IOSH	IIL	IIH
Drive Strength	Min., V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA²	μA²
20 mA ³	-0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	_	20	20	124	169	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

2. Currents are measured at 85°C junction temperature.

3. Output drive strength is below JEDEC specification.



Figure 2-13 • AC Loading

Table 2-52 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.05	VREF + 0.05	0.8	0.8	1.2	10

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-53 • 2.5 V GTL

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V VREF = 0.8 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.60	2.13	0.04	2.46	0.43	2.16	2.13			4.40	4.36	ns
-1	0.51	1.81	0.04	2.09	0.36	1.84	1.81			3.74	3.71	ns
-2	0.45	1.59	0.03	1.83	0.32	1.61	1.59			3.28	3.26	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

I/O Register Specifications



Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Figure 2-25 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

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ProASIC3E DC and Switching Characteristics

Table 2-85 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t _{oclkq}	Clock-to-Q of the Output Data Register	HH, DOUT
tosud	Data Setup Time for the Output Data Register	FF, HH
t _{OHD}	Data Hold Time for the Output Data Register	FF, HH
tosue	Enable Setup Time for the Output Data Register	GG, HH
t _{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t _{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
t _{OREMCLR}	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
t _{ORECCLR}	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t _{oeclkq}	Clock-to-Q of the Output Enable Register	HH, EOUT
t _{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t _{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t _{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t _{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
t _{OECLR2Q}	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
t _{OEREMCLR}	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
t _{OERECCLR}	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t _{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t _{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t _{IHD}	Data Hold Time for the Input Data Register	CC, AA
t _{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t _{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t _{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
t _{IREMCLR}	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
t _{IRECCLR}	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

Note: *See Figure 2-26 on page 2-55 for more information.





Figure 2-39 • Peak-to-Peak Jitter Definition

Embedded SRAM and FIFO Characteristics



SRAM

Figure 2-40 • RAM Models



	PQ208		PQ208	PQ208	
Pin Number	A3PE1500 Function	Pin Number	A3PE1500 Function	Pin Number	A3PE1500 Function
109	TRST	145	IO71NDB2V2	181	IO29NDB0V3
110	VJTAG	146	IO71PDB2V2	182	IO27PDB0V3
111	VMV3	147	IO67NDB2V1	183	IO27NDB0V3
112	GDA0/IO110NPB3V2	148	IO67PDB2V1	184	IO23PDB0V2
113	GDB0/IO109NPB3V2	149	IO65NDB2V1	185	IO23NDB0V2
114	GDA1/IO110PPB3V2	150	IO65PDB2V1	186	VCCIB0
115	GDB1/IO109PPB3V2	151	GBC2/IO60PSB2V0	187	VCC
116	GDC0/IO108NDB3V2	152	GBA2/IO58PSB2V0	188	IO18PDB0V2
117	GDC1/IO108PDB3V2	153	GBB2/IO59PSB2V0	189	IO18NDB0V2
118	IO105NDB3V2	154	VMV2	190	IO15PDB0V1
119	IO105PDB3V2	155	GNDQ	191	IO15NDB0V1
120	IO101NDB3V1	156	GND	192	IO12PSB0V1
121	IO101PDB3V1	157	VMV1	193	IO11PDB0V1
122	GND	158	GNDQ	194	IO11NDB0V1
123	VCCIB3	159	GBA1/IO57PDB1V3	195	GND
124	GCC2/IO90PSB3V0	160	GBA0/IO57NDB1V3	196	IO08PDB0V1
125	GCB2/IO89PSB3V0	161	GBB1/IO56PDB1V3	197	IO08NDB0V1
126	NC	162	GND	198	IO05PDB0V0
127	IO88NDB3V0	163	GBB0/IO56NDB1V3	199	IO05NDB0V0
128	GCA2/IO88PDB3V0	164	GBC1/IO55PDB1V3	200	VCCIB0
129	GCA1/IO87PPB3V0	165	GBC0/IO55NDB1V3	201	GAC1/IO02PDB0V0
130	GND	166	IO51PDB1V2	202	GAC0/IO02NDB0V0
131	VCCPLC	167	IO51NDB1V2	203	GAB1/IO01PDB0V0
132	GCA0/IO87NPB3V0	168	IO47PDB1V1	204	GAB0/IO01NDB0V0
133	VCOMPLC	169	IO47NDB1V1	205	GAA1/IO00PDB0V0
134	GCB0/IO86NDB2V3	170	VCCIB1	206	GAA0/IO00NDB0V0
135	GCB1/IO86PDB2V3	171	VCC	207	GNDQ
136	GCC1/IO85PSB2V3	172	IO43PSB1V1	208	VMV0
137	IO83NDB2V3	173	IO41PDB1V1		
138	IO83PDB2V3	174	IO41NDB1V1		
139	IO81PSB2V3	175	IO35PDB1V0		
140	VCCIB2	176	IO35NDB1V0		
141	GND	177	IO31PDB0V3		
142	VCC	178	GND		
143	IO73NDB2V2	179	IO31NDB0V3		
144	IO73PDB2V2	180	IO29PDB0V3		

Package Pin Assignments

	FG484		FG484	FG484	
Pin Number	A3PE1500 Function	Pin Number	A3PE1500 Function	Pin Number	A3PE1500 Function
A1	GND	AA15	NC	B7	IO10PDB0V1
A2	GND	AA16	IO117NDB4V0	B8	IO15NDB0V1
A3	VCCIB0	AA17	IO117PDB4V0	B9	IO17NDB0V2
A4	IO05NDB0V0	AA18	IO115NDB4V0	B10	IO20PDB0V2
A5	IO05PDB0V0	AA19	IO115PDB4V0	B11	IO29PDB0V3
A6	IO11NDB0V1	AA20	NC	B12	IO32NDB1V0
A7	IO11PDB0V1	AA21	VCCIB3	B13	IO43NDB1V1
A8	IO15PDB0V1	AA22	GND	B14	NC
A9	IO17PDB0V2	AB1	GND	B15	NC
A10	IO27NDB0V3	AB2	GND	B16	IO53NDB1V2
A11	IO27PDB0V3	AB3	VCCIB5	B17	IO53PDB1V2
A12	IO32PDB1V0	AB4	IO159NDB5V3	B18	IO54PDB1V3
A13	IO43PDB1V1	AB5	IO159PDB5V3	B19	NC
A14	IO47NDB1V1	AB6	IO149NDB5V1	B20	NC
A15	IO47PDB1V1	AB7	IO149PDB5V1	B21	VCCIB2
A16	IO51NDB1V2	AB8	IO138NDB5V0	B22	GND
A17	IO51PDB1V2	AB9	IO138PDB5V0	C1	VCCIB7
A18	IO54NDB1V3	AB10	NC	C2	NC
A19	NC	AB11	NC	C3	NC
A20	VCCIB1	AB12	IO127NDB4V2	C4	NC
A21	GND	AB13	IO127PDB4V2	C5	GND
A22	GND	AB14	IO125NDB4V1	C6	IO07NDB0V0
AA1	GND	AB15	IO125PDB4V1	C7	IO07PDB0V0
AA2	VCCIB6	AB16	IO122NDB4V1	C8	VCC
AA3	NC	AB17	IO122PDB4V1	C9	VCC
AA4	IO161PDB5V3	AB18	NC	C10	IO20NDB0V2
AA5	IO155NDB5V2	AB19	NC	C11	IO29NDB0V3
AA6	IO155PDB5V2	AB20	VCCIB4	C12	NC
AA7	IO154NDB5V2	AB21	GND	C13	NC
AA8	IO154PDB5V2	AB22	GND	C14	VCC
AA9	IO143PDB5V1	B1	GND	C15	VCC
AA10	IO143NDB5V1	B2	VCCIB7	C16	NC
AA11	IO131PPB4V2	B3	NC	C17	NC
AA12	IO129NDB4V2	B4	IO03NDB0V0	C18	GND
AA13	IO129PDB4V2	B5	IO03PDB0V0	C19	NC
AA14	NC	B6	IO10NDB0V1	C20	NC

	FG676	
Pin Number	A3PE1500 Function	Pin N
A1	GND	A/
A2	GND	AA
A3	GAA0/IO00NDB0V0	AA
A4	GAA1/IO00PDB0V0	AA
A5	IO06NDB0V0	AA
A6	IO09NDB0V1	AA
A7	IO09PDB0V1	AA
A8	IO14NDB0V1	AA
A9	IO14PDB0V1	AA
A10	IO22NDB0V2	AA
A11	IO22PDB0V2	AA
A12	IO26NDB0V3	AA
A13	IO26PDB0V3	AA
A14	IO30NDB0V3	AA
A15	IO30PDB0V3	AA
A16	IO34NDB1V0	AA
A17	IO34PDB1V0	A
A18	IO38NDB1V0	A
A19	IO38PDB1V0	A
A20	IO41PDB1V1	A
A21	IO44PDB1V1	A
A22	IO49PDB1V2	A
A23	IO50PDB1V2	A
A24	GBC1/IO55PDB1V3	A
A25	GND	A
A26	GND	AE
AA1	IO174PDB6V0	A
AA2	IO171PDB6V0	AE
AA3	GEA1/IO167PPB6V0	AE
AA4	GEC0/IO169NPB6V0	AE
AA5	VCOMPLE	AE
AA6	GND	AE
AA7	IO165NDB5V3	AE
AA8	GEB2/IO165PDB5V3	A
AA9	IO163PDB5V3	AE
AA10	IO159NDB5V3	AE

FG676						
Pin Number	A3PE1500 Function					
AA11	IO153NDB5V2					
AA12	IO147NDB5V1					
AA13	IO139NDB5V0					
AA14	IO137NDB5V0					
AA15	IO123NDB4V1					
AA16	IO123PDB4V1					
AA17	IO117NDB4V0					
AA18	IO117PDB4V0					
AA19	GDB2/IO112PDB4V0					
AA20	GNDQ					
AA21	TDO					
AA22	GND					
AA23	GND					
AA24	IO102NDB3V1					
AA25	IO102PDB3V1					
AA26	IO98NDB3V1					
AB1	IO174NDB6V0					
AB2	IO171NDB6V0					
AB3	GEB1/IO168PPB6V0					
AB4	GEA0/IO167NPB6V0					
AB5	VCCPLE					
AB6	GND					
AB7	GND					
AB8	IO156NDB5V2					
AB9	IO156PDB5V2					
AB10	IO150PDB5V1					
AB11	IO155PDB5V2					
AB12	IO142PDB5V0					
AB13	IO135NDB5V0					
AB14	IO135PDB5V0					
AB15	IO132PDB4V2					
AB16	IO129PDB4V2					
AB17	IO121PDB4V1					
AB18	IO119NDB4V1					
AB19	IO112NDB4V0					
AB20	VMV4					

FG676					
Pin Number	A3PE1500 Function				
AB21	TCK				
AB22	TRST				
AB23	GDC0/IO108NDB3V2				
AB24	GDC1/IO108PDB3V2				
AB25	IO104NDB3V2				
AB26	IO104PDB3V2				
AC1	IO170PDB6V0				
AC2	GEB0/IO168NPB6V0				
AC3	IO166NPB5V3				
AC4	GNDQ				
AC5	GND				
AC6	IO160PDB5V3				
AC7	IO161PDB5V3				
AC8	IO154PDB5V2				
AC9	GND				
AC10	IO150NDB5V1				
AC11	IO155NDB5V2				
AC12	IO142NDB5V0				
AC13	IO138NDB5V0				
AC14	IO138PDB5V0				
AC15	IO132NDB4V2				
AC16	IO129NDB4V2				
AC17	IO121NDB4V1				
AC18	IO119PDB4V1				
AC19	IO118NDB4V0				
AC20	IO118PDB4V0				
AC21	IO114PPB4V0				
AC22	TMS				
AC23	VJTAG				
AC24	VMV3				
AC25	IO106NDB3V2				
AC26	IO106PDB3V2				
AD1	IO170NDB6V0				
AD2	GEA2/IO166PPB5V3				
AD3	VMV5				
AD4	GEC2/IO164PDB5V3				

Package Pin Assignments

	FG676	FG676		FG676	
Pin Number	A3PE1500 Function	Pin Number	A3PE1500 Function	Pin Number	A3PE1500 Function
AD5	IO162PDB5V3	AE15	IO134NDB4V2	AF25	GND
AD6	IO160NDB5V3	AE16	IO133NDB4V2	AF26	GND
AD7	IO161NDB5V3	AE17	IO127NDB4V2	B1	GND
AD8	IO154NDB5V2	AE18	IO130NDB4V2	B2	GND
AD9	IO148PDB5V1	AE19	IO126NDB4V1	B3	GND
AD10	IO151PDB5V2	AE20	IO124NDB4V1	B4	GND
AD11	IO144PDB5V1	AE21	IO120NDB4V1	B5	IO06PDB0V0
AD12	IO140PDB5V0	AE22	IO116PDB4V0	B6	IO04NDB0V0
AD13	IO143PDB5V1	AE23	GDC2/IO113PDB4V0	B7	IO07NDB0V0
AD14	IO141PDB5V0	AE24	GDA2/IO111PDB4V0	B8	IO11NDB0V1
AD15	IO134PDB4V2	AE25	GND	B9	IO10NDB0V1
AD16	IO133PDB4V2	AE26	GND	B10	IO16NDB0V2
AD17	IO127PDB4V2	AF1	GND	B11	IO20NDB0V2
AD18	IO130PDB4V2	AF2	GND	B12	IO24NDB0V3
AD19	IO126PDB4V1	AF3	GND	B13	IO23NDB0V2
AD20	IO124PDB4V1	AF4	GND	B14	IO28NDB0V3
AD21	IO120PDB4V1	AF5	IO158NPB5V2	B15	IO31NDB0V3
AD22	IO114NPB4V0	AF6	IO157NPB5V2	B16	IO32PDB1V0
AD23	TDI	AF7	IO152NPB5V2	B17	IO36PDB1V0
AD24	GNDQ	AF8	IO146NDB5V1	B18	IO37PDB1V0
AD25	GDA0/IO110NDB3V2	AF9	IO146PDB5V1	B19	IO42NPB1V1
AD26	GDA1/IO110PDB3V2	AF10	IO149NDB5V1	B20	IO41NDB1V1
AE1	GND	AF11	IO149PDB5V1	B21	IO44NDB1V1
AE2	GND	AF12	IO145NDB5V1	B22	IO49NDB1V2
AE3	GND	AF13	IO145PDB5V1	B23	IO50NDB1V2
AE4	IO164NDB5V3	AF14	IO136NDB5V0	B24	GBC0/IO55NDB1V3
AE5	IO162NDB5V3	AF15	IO136PDB5V0	B25	GND
AE6	IO158PPB5V2	AF16	IO131NDB4V2	B26	GND
AE7	IO157PPB5V2	AF17	IO131PDB4V2	C1	GND
AE8	IO152PPB5V2	AF18	IO128NDB4V2	C2	GND
AE9	IO148NDB5V1	AF19	IO128PDB4V2	C3	GND
AE10	IO151NDB5V2	AF20	IO122NDB4V1	C4	GND
AE11	IO144NDB5V1	AF21	IO122PDB4V1	C5	GAA2/IO221PDB7V3
AE12	IO140NDB5V0	AF22	IO116NDB4V0	C6	IO04PDB0V0
AE13	IO143NDB5V1	AF23	IO113NDB4V0	C7	IO07PDB0V0
AE14	IO141NDB5V0	AF24	IO111NDB4V0	C8	IO11PDB0V1

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the ProASIC3E datasheet.

Revision	Changes	Page
Revision 15 (June 2015)	Updated "ProASIC3E Ordering Information". Interchanged the positions of Y-Security Feature and I- Application (Temperature Range) (SAR 67296).	1-111
	Added Note "Only devices with package size greater than or equal to 5x5 are supported".	
	Updated Commercial and Industrial Junction Temperatures (SAR 67588).	
	Added the A3PE3000 package to Table 2-5 (SARs 52320 and 58737).	2-5
	Updated "VCCIBx I/O Supply Voltage" (SAR 43323).	3-1
Revision 14 (May 2014)	Added 2 mA and 6 mA I/O short currents values in"I/O Short Currents IOSH/IOSL" (SAR 56295).	2-22 2-24
(Added 2 mA and 6 mA minimum and maximum DC input and output levels in "Minimum and Maximum DC Input and Output Levels" (SAR 56295).	2-25 2-25
	Added 3.3 V LVTTL / 3.3 V LVCMOS High Slew Commercial-Case Conditions for 2 mA and 6 mA in "3.3 V LVTTL / 3.3 V LVCMOS High Slew" (SAR 56295).	
	Added 3.3 V LVTTL / 3.3 V LVCMOS Low Slew Commercial-Case Conditions for 2 mA and 6 mA in "3.3 V LVTTL / 3.3 V LVCMOS Low Slew" (SAR 56295).	
Revision 13 (January 2013)	In the "Features and Benefits" section, updated the Clock Conditioning Circuit (CCC) and PLL Wide Input Frequency Range from '1.5 MHz to 200 MHz' to '1.5MHz to 350 MHz' based on Table 2-98 (SAR 22196).	1-1
	The "ProASIC3E Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43220).	1-111
	Added a note to "Recommended Operating Conditions ¹ " table (SAR 42716): The programming temperature range supported is $T_{ambient} = 0^{\circ}C$ to 85°C.	2-2
	The note in "ProASIC3E CCC/PLL Specification" table referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42571).	2-70
	Libero Integrated Design Environment (IDE) was changed to Libero System-on- Chip (SoC) throughout the document (SAR 40285).	NA
	Live at Power-Up (LAPU) has been replaced with 'Instant On'.	
Revision 12 (September 2012)	The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data.	1-1



Datasheet Information

Revision	Changes	Page					
Revision 11 (August 2012)	Added a Note stating "VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information." to Table 2-1 • Absolute Maximum Ratings and Table 2-2 • Recommended Operating Conditions ¹ (SAR 38322).						
	The drive strength, IOL, and IOH value for 3.3 V GTL and 2.5 V GTL was changed from 25 mA to 20 mA in the following tables (SAR 31924):						
	"Summary of Maximum and Minimum DC Input and Output Levels" table						
	"Summary of I/O Timing Characteristics—Software Default Settings" table	2-19					
	"I/O Output Buffer Maximum Resistances ¹ " table	2-20					
	"Minimum and Maximum DC Input and Output Levels" table)	2-39					
	"Minimum and Maximum DC Input and Output Levels" table	2-40					
	Also added note stating "Output drive strength is below JEDEC specification" for Tables 2-17 and 2-19.						
	Additionally, the IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected from 51 to 35 (for 3.3 V GTL+) and from 40 to 33 (for 2.5 V GTL+) in table Table 2-13 (SAR 39714).						
	"Duration of Short Circuit Event Before Failure" table was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 37934).						
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34796):	2-30					
	"It uses a 5 V–tolerant input buffer and push-pull output buffer." This change was made in revision 10 and omitted from the change table in error.						
Revision 11 (continued)	Figure 2-11 was updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34889).	2-38					
	In Table 2-81 VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 37222).	2-52					
	Figure 2-47and Figure 2-48 are new (SAR 34848).	2-79					
	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions and Packaging" chapter: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38322). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1					



Revision		Changes	Page
Revision 9 (Aug 2009)	All references to speed grade –F have been removed from this document.		N/A
Product Brief v1.2			
	The "Pro I/Os with Advance definitions of hot-swap and col	ed I/O Standards" section was revised to add Id-sparing.	1-6
DC and Switching Characteristics v1.3	3.3 V LVCMOS and 1.2 V L datasheet. This affects all ta LVCMOS data.	VCMOS Wide Range support was added to the ables that contained 3.3 V LVCMOS and 1.2 V	N/A
	IIL and IIH input leakage current information was added to all "Minin Maximum DC Input and Output Levels" tables.		N/A
	–F was removed from the data	asheet. The speed grade is no longer supported.	N/A
	In the Table 2-2 • Recommended Operating Conditions ¹ "3.0 V DC supply voltage" and note 4 are new.		2-2
	The Table 2-4 • Overshoot and	d Undershoot Limits ¹ table was updated.	2-3
	The Table 2-6 • Temperature and Voltage Derating Factors for Timing Delay table was updated.		2-5
	There are new parameters and data was updated in the Table 2-99 • RAM4K9 table.		2-76
	There are new parameters and data was updated in the Table 2-100 • RAM512X18 table.		2-77
Revision 8 (Feb 2008)	Table 1-2 • ProASIC3E FPGAs Package Sizes Dimensions is new.		1-II
Product Brief v1.1			
Revision 7 (Jun 2008) DC and Switching	The title of Table 2-4 • Overshoot and Undershoot Limits ¹ was modified to remove "as measured on quiet I/Os." Table note 2 was revised to remove		2-3
Characteristics v1.2	"estimated SSO density over cycles." Table note 3 was deleted.		
	Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels was updated.		2-50
Revision 6 (Jun 2008)	The A3PE600 "FG484" table was missing G22. The pin and its function were added to the table.		4-27
Revision 5 (Jun 2008) Packaging v1.4	The naming conventions changed for the following pins in the "FG484" for the A3PE600:		4-22
	Pin Number	New Function Name	
	J19	IO45PPB2V1	
	K20	IO45NPB2V1	
	M2	IO114NPB6V1	
	N1	IO114PPB6V1	
	N4	GFC2/IO115PPB6V1	
	P3	IO115NPB6V1	
Revision 4 (Apr 2008) Product Brief v1.0	The product brief portion of the datasheet was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.		N/A
Packaging v1.3	The "FG324" package diagram was replaced.		4-12