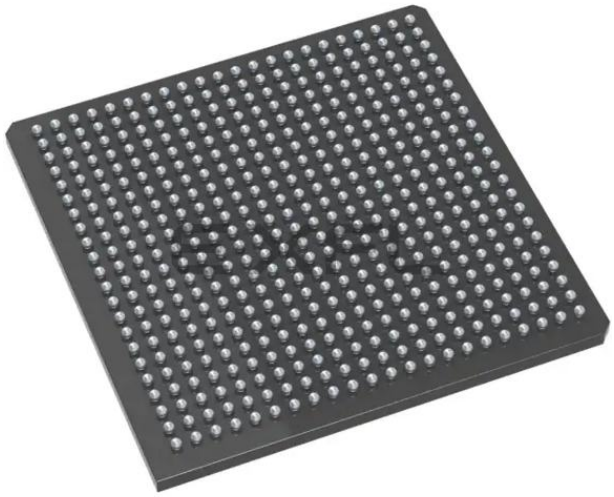

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 516096 |
| Number of I/O | 341 |
| Number of Gates | 3000000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a3pe3000-2fg484i |

## Advanced Architecture

The proprietary ProASIC3E architecture provides granularity comparable to standard-cell ASICs. The ProASIC3E device consists of five distinct and programmable architectural features (Figure 1-1 on page 3):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- Pro I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the ProASIC3E core tile as either a three-input lookup table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC family of third-generation architecture Flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

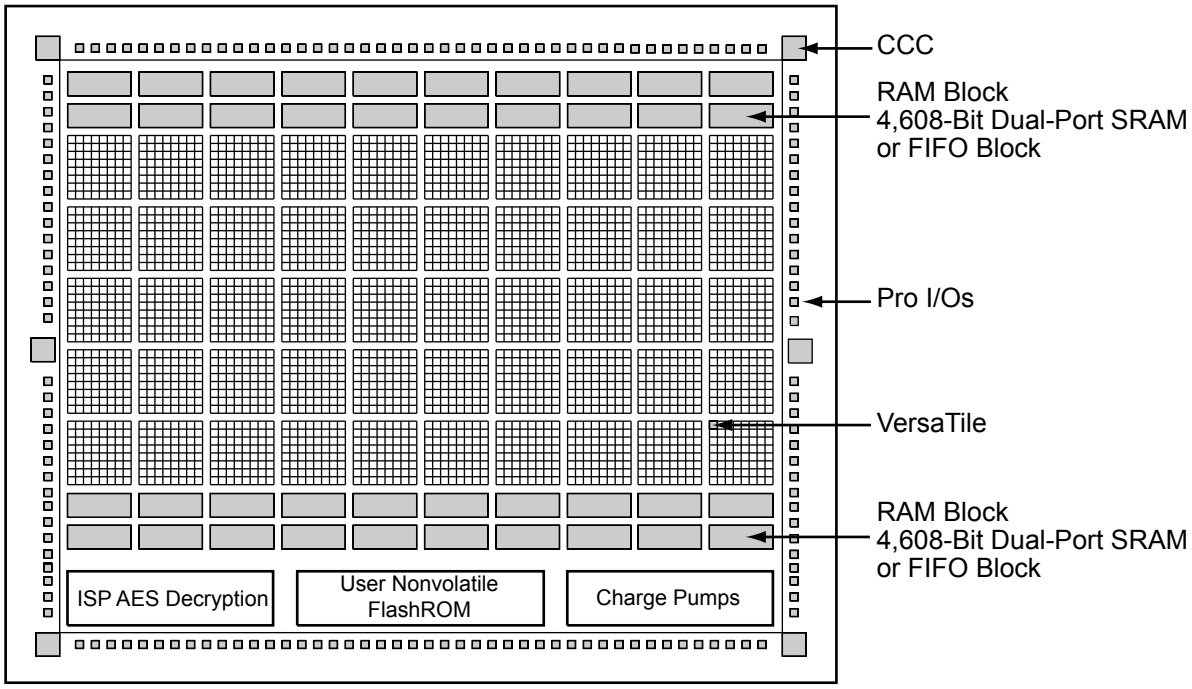



***Figure 1-1 •*** **ProASIC3E Device Architecture Overview**

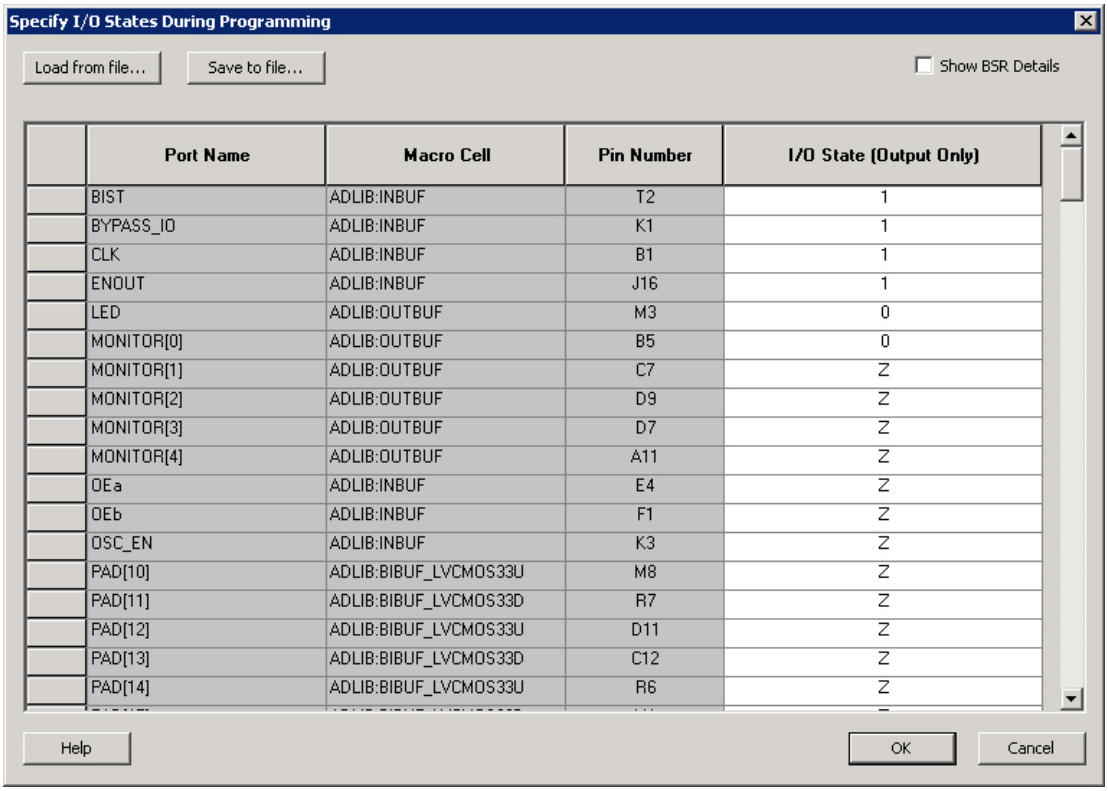



***Figure 1-3 •*** **I/O States During Programming Window**

6. Click OK to return to the FlashPoint – Programming File Generator window.

   I/O States during programming are saved to the ADB and resulting programming files after completing programming file generation.

## PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLXL exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-1 on page 2-4 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *ProASIC3E FPGA Fabric User's Guide* for information on clock and lock recovery.

## Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

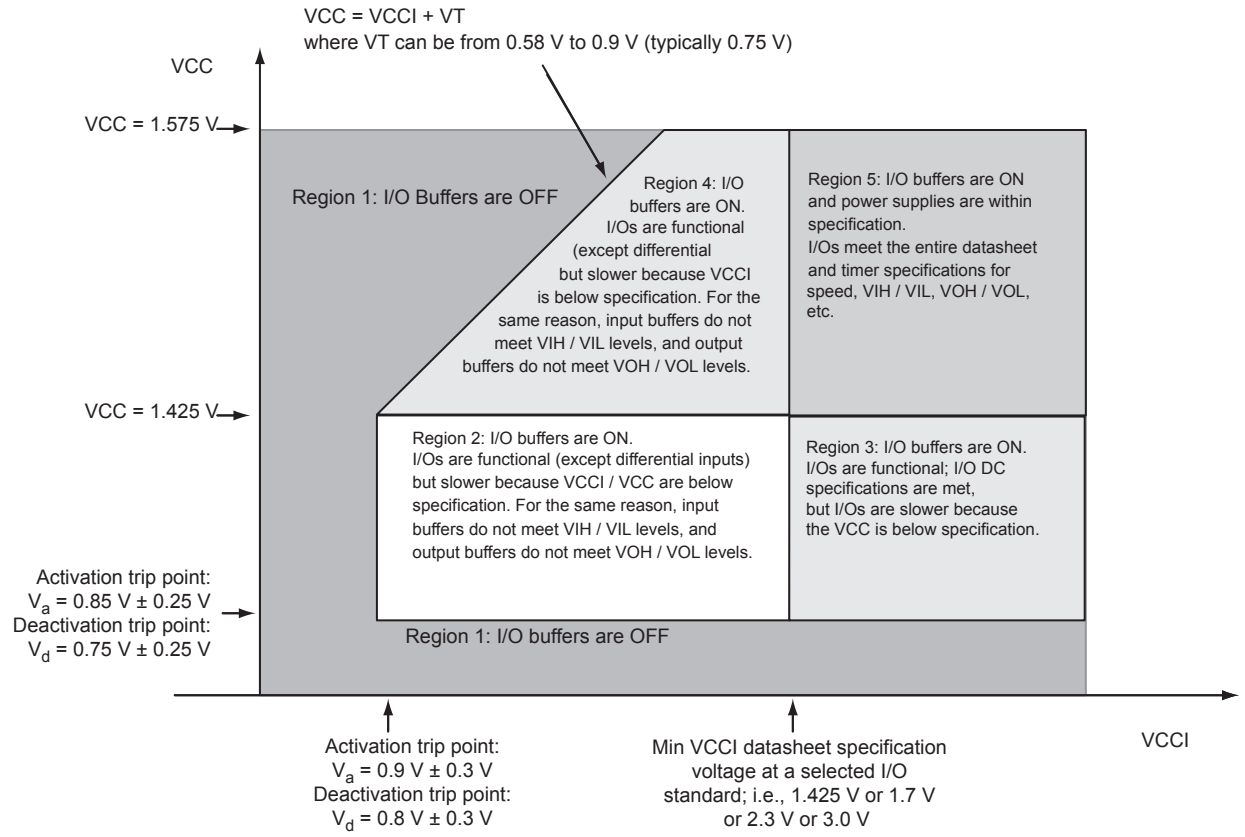



***Figure 2-1 •*** **I/O State as a Function of VCCI and VCC Voltage Levels**

# Thermal Characteristics

## Introduction

The temperature variable in Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$T_J$ = Junction Temperature = $\Delta T + T_A$

*EQ 1*

where:

$T_A$ = Ambient Temperature

$\Delta T$ = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

$\theta_{ja}$ = Junction-to-ambient of the package. $\theta_{ja}$ numbers are located in Table 2-5.

P = Power dissipation

## Package Thermal Characteristics

The device junction-to-case thermal resistivity is $\theta_{jc}$ and the junction-to-ambient air thermal resistivity is $\theta_{ja}$. The thermal characteristics for $\theta_{ja}$ are shown for two air flow rates. The absolute maximum junction temperature is 110°C. EQ 2 shows a sample calculation of the absolute maximum power dissipation allowed for an 896-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. } (°C) - \text{Max. ambient temp. } (°C)}{\theta_{ja}(°C/W)} = \frac{110°C - 70°C}{13.6°C/W} = 5.88\ W$$

*EQ 2*

***Table 2-5 •*** **Package Thermal Resistivities**

| Package Type | Pin Count | $\theta_{jc}$ | $\theta_{ja}$ | | | Units |
|---|---|---|---|---|---|---|
| | | | Still Air | 200 ft./min. | 500 ft./min. | |
| Plastic Quad Flat Package (PQFP) | 208 | 8.0 | 26.1 | 22.5 | 20.8 | C/W |
| Plastic Quad Flat Package (PQFP) with embedded heat spreader in A3PE3000 | 208 | 3.8 | 16.2 | 13.3 | 11.9 | C/W |
| Fine Pitch Ball Grid Array (FBGA) | 256 | 3.8 | 26.9 | 22.8 | 21.5 | C/W |
| | 484 | 3.2 | 20.5 | 17.0 | 15.9 | C/W |
| | 676 | 3.2 | 16.4 | 13.0 | 12.0 | C/W |
| | 896 | 2.4 | 13.6 | 10.4 | 9.4 | C/W |

## Temperature and Voltage Derating Factors

***Table 2-6 •*** **Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J$ = 70°C, VCC = 1.425 V)**

| Array Voltage VCC (V) | Junction Temperature (°C) | | | | | |
|---|---|---|---|---|---|---|
| | –40°C | 0°C | 25°C | 70°C | 85°C | 100°C |
| 1.425 | 0.87 | 0.92 | 0.95 | 1.00 | 1.02 | 1.04 |
| 1.500 | 0.83 | 0.88 | 0.90 | 0.95 | 0.97 | 0.98 |
| 1.575 | 0.80 | 0.85 | 0.87 | 0.92 | 0.93 | 0.95 |

**Table 2-8 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings (continued)**

| | VMV (V) | Static Power PDC2 (mW)[1] | Dynamic Power PAC9 (µW/MHz)[2] |
|---|---|---|---|
| HSTL (I) | 1.5 | 0.17 | 2.03 |
| HSTL (II) | 1.5 | 0.17 | 2.03 |
| SSTL2 (I) | 2.5 | 1.38 | 4.48 |
| SSTL2 (II) | 2.5 | 1.38 | 4.48 |
| SSTL3 (I) | 3.3 | 3.21 | 9.26 |
| SSTL3 (II) | 3.3 | 3.21 | 9.26 |
| **Differential** | | | |
| LVDS/B-LVDS/M-LVDS | 2.5 | 2.26 | 1.50 |
| LVPECL | 3.3 | 5.71 | 2.17 |

*Notes:*

1. *PDC2 is the static power (where applicable) measured on VMV.*
2. *PAC9 is the total dynamic power measured on VCC and VMV.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.*

**Table 2-9 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1]**

| | $C_{LOAD}$ (pF) | VCCI (V) | Static Power PDC3 (mW)[2] | Dynamic Power PAC10 (µW/MHz)[3] |
|---|---|---|---|---|
| **Single-Ended** | | | | |
| 3.3 V LVTTL/LVCMOS | 35 | 3.3 | – | 474.70 |
| 3.3 V LVTTL/LVCMOS Wide Range[4] | 35 | 3.3 | – | 474.70 |
| 2.5 V LVCMOS | 35 | 2.5 | – | 270.73 |
| 1.8 V LVCMOS | 35 | 1.8 | – | 151.78 |
| 1.5 V LVCMOS (JESD8-11) | 35 | 1.5 | – | 104.55 |
| 3.3 V PCI | 10 | 3.3 | – | 204.61 |
| 3.3 V PCI-X | 10 | 3.3 | – | 204.61 |
| **Voltage-Referenced** | | | | |
| 3.3 V GTL | 10 | 3.3 | – | 24.08 |
| 2.5 V GTL | 10 | 2.5 | – | 13.52 |
| 3.3 V GTL+ | 10 | 3.3 | – | 24.10 |
| 2.5 V GTL+ | 10 | 2.5 | – | 13.54 |
| HSTL (I) | 20 | 1.5 | 7.08 | 26.22 |
| HSTL (II) | 20 | 1.5 | 13.88 | 27.22 |
| SSTL2 (I) | 30 | 2.5 | 16.69 | 105.56 |
| SSTL2 (II) | 30 | 2.5 | 25.91 | 116.60 |

*Notes:*

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PDC3 is the static power (where applicable) measured on VCCI.*
3. *PAC10 is the total dynamic power measured on VCC and VCCI.*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

## Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-11 on page 2-11.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-12 on page 2-11.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-12 on page 2-11. The calculation should be repeated for each clock domain defined in the design.

### Methodology

#### Total Power Consumption—$P_{TOTAL}$

$P_{TOTAL} = P_{STAT} + P_{DYN}$

$P_{STAT}$ is the total static power consumption.

$P_{DYN}$ is the total dynamic power consumption.

#### Total Static Power Consumption—$P_{STAT}$

$P_{STAT} = PDC1 + N_{INPUTS} * PDC2 + N_{OUTPUTS} * PDC3$

$N_{INPUTS}$ is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

#### Total Dynamic Power Consumption—$P_{DYN}$

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

#### Global Clock Contribution—$P_{CLOCK}$

$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S\text{-}CELL} * PAC4) * F_{CLK}$

$N_{SPINE}$ is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3E FPGA Fabric User's Guide*.

$N_{ROW}$ is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3E FPGA Fabric User's Guide*.

$F_{CLK}$ is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

#### Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-11 on page 2-11.

$F_{CLK}$ is the global clock signal frequency.

## Summary of I/O Timing Characteristics – Default I/O Software Settings

**Table 2-15 • Summary of AC Measuring Points**

| Standard | Input Reference Voltage (VREF_TYP) | Board Termination Voltage (VTT_REF) | Measuring Trip Point (Vtrip) |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | – | – | 1.4 V |
| 3.3 V LVCMOS Wide Range | – | – | 1.4 V |
| 2.5 V LVCMOS | – | – | 1.2 V |
| 1.8 V LVCMOS | – | – | 0.90 V |
| 1.5 V LVCMOS | – | – | 0.75 V |
| 3.3 V PCI | – | – | 0.285 * VCCI (RR)<br>0.615 * VCCI (FF)) |
| 3.3 V PCI-X | – | – | 0.285 * VCCI (RR)<br>0.615 * VCCI (FF) |
| 3.3 V GTL | 0.8 V | 1.2 V | VREF |
| 2.5 V GTL | 0.8 V | 1.2 V | VREF |
| 3.3 V GTL+ | 1.0 V | 1.5 V | VREF |
| 2.5 V GTL+ | 1.0 V | 1.5 V | VREF |
| HSTL (I) | 0.75 V | 0.75 V | VREF |
| HSTL (II) | 0.75 V | 0.75 V | VREF |
| SSTL2 (I) | 1.25 V | 1.25 V | VREF |
| SSTL2 (II) | 1.25 V | 1.25 V | VREF |
| SSTL3 (I) | 1.5 V | 1.485 V | VREF |
| SSTL3 (II) | 1.5 V | 1.485 V | VREF |
| LVDS | – | – | Cross point |
| LVPECL | – | – | Cross point |

**Table 2-16 • I/O AC Parameter Definitions**

| Parameter | Definition |
|---|---|
| $t_{DP}$ | Data to Pad delay through the Output Buffer |
| $t_{PY}$ | Pad to Data delay through the Input Buffer with Schmitt trigger disabled |
| $t_{DOUT}$ | Data to Output Buffer delay through the I/O interface |
| $t_{EOUT}$ | Enable to Output Buffer Tristate Control delay through the I/O interface |
| $t_{DIN}$ | Input Buffer to Data delay through the I/O interface |
| $t_{PYS}$ | Pad to Data delay through the Input Buffer with Schmitt trigger enabled |
| $t_{HZ}$ | Enable to Pad delay through the Output Buffer—High to Z |
| $t_{ZH}$ | Enable to Pad delay through the Output Buffer—Z to High |
| $t_{LZ}$ | Enable to Pad delay through the Output Buffer—Low to Z |
| $t_{ZL}$ | Enable to Pad delay through the Output Buffer—Z to Low |
| $t_{ZHS}$ | Enable to Pad delay through the Output Buffer with delayed enable—Z to High |
| $t_{ZLS}$ | Enable to Pad delay through the Output Buffer with delayed enable—Z to Low |

## Detailed I/O DC Characteristics

***Table 2-18* • Input Capacitance**

| Symbol | Definition | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | VIN = 0, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on the clock pin | VIN = 0, f = 1.0 MHz | | 8 | pF |

***Table 2-19* • I/O Output Buffer Maximum Resistances[1]**

| Standard | Drive Strength | $R_{PULL\text{-}DOWN}$ (Ω)[2] | $R_{PULL\text{-}UP}$ (Ω)[3] |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 4 mA | 100 | 300 |
| | 8 mA | 50 | 150 |
| | 12 mA | 25 | 75 |
| | 16 mA | 17 | 50 |
| | 24 mA | 11 | 33 |
| 3.3 V LVCMOS Wide Range | 100 µA | Same as regular 3.3 V LVCMOS | Same as regular 3.3 V LVCMOS |
| 2.5 V LVCMOS | 4 mA | 100 | 200 |
| | 8 mA | 50 | 100 |
| | 12 mA | 25 | 50 |
| | 16 mA | 20 | 40 |
| | 24 mA | 11 | 22 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| | 6 mA | 50 | 56 |
| | 8 mA | 50 | 56 |
| | 12 mA | 20 | 22 |
| | 16 mA | 20 | 22 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |
| | 4 mA | 100 | 112 |
| | 6 mA | 67 | 75 |
| | 8 mA | 33 | 37 |
| | 12 mA | 33 | 37 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 25 | 75 |
| 3.3 V GTL | 20 mA[4] | 11 | – |
| 2.5 V GTL | 20 mA[4] | 14 | – |

*Notes:*

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website at www.microsemi.com/index.php?option=com_content&id=1671&lang=en&view=article.*
2. *$R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / IOLspec*
3. *$R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / IOHspec*
4. *Output drive strength is below JEDEC specification.*

### 3.3 V LVCMOS Wide Range

**Table 2-29 • Minimum and Maximum DC Input and Output Levels**

| 3.3 V LVCMOS Wide Range | Equivalent Software Default Drive Strength Option[1] | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[2] | IIH[3] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | µA | µA | Max. mA[4] | Max. mA[4] | µA[5] | µA[5] |
| 100 µA | 2 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 27 | 25 | 10 | 10 |
| 100 µA | 4 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 27 | 25 | 10 | 10 |
| 100 µA | 6 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 54 | 51 | 10 | 10 |
| 100 µA | 8 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 54 | 51 | 10 | 10 |
| 100 µA | 12 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 109 | 103 | 10 | 10 |
| 100 µA | 16 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 127 | 132 | 10 | 10 |
| 100 µA | 24 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 181 | 268 | 10 | 10 |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN< VCCI. Input current is larger when operating outside recommended ranges.*
4. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

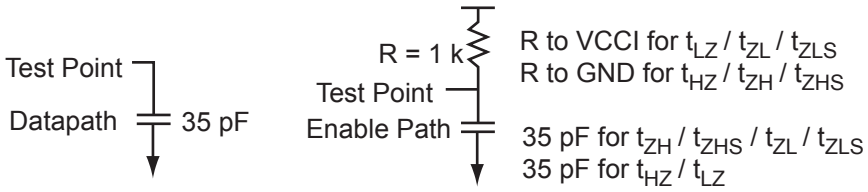



**Figure 2-7 • AC Loading**

**Table 2-30 • 3.3 V LVCMOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|
| 0 | 3.3 | 1.4 | – | 35 |

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

### 2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

**Table 2-33 • Minimum and Maximum DC Input and Output Levels**

| 2.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max., V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 4 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 4 | 4 | 18 | 16 | 10 | 10 |
| 8 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 | 37 | 32 | 10 | 10 |
| 12 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 12 | 12 | 74 | 65 | 10 | 10 |
| 16 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 16 | 16 | 87 | 83 | 10 | 10 |
| 24 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 24 | 24 | 124 | 169 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

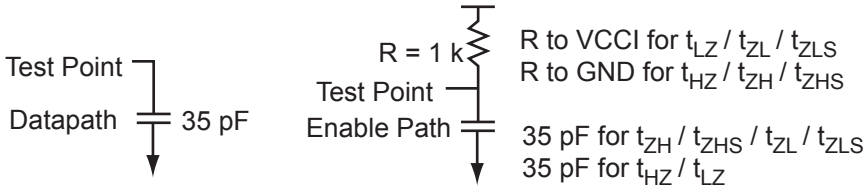



**Figure 2-8 • AC Loading**

**Table 2-34 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|
| 0 | 2.5 | 1.2 | – | 35 |

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

**Table 2-40 • 1.8 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 15.84 | 0.04 | 1.45 | 1.91 | 0.43 | 15.65 | 15.84 | 2.78 | 1.58 | 17.89 | 18.07 | ns |
| | –1 | 0.56 | 13.47 | 0.04 | 1.23 | 1.62 | 0.36 | 13.31 | 13.47 | 2.37 | 1.35 | 15.22 | 15.37 | ns |
| | –2 | 0.49 | 11.83 | 0.03 | 1.08 | 1.42 | 0.32 | 11.69 | 11.83 | 2.08 | 1.18 | 13.36 | 13.50 | ns |
| 4 mA | Std. | 0.66 | 11.39 | 0.04 | 1.45 | 1.91 | 0.43 | 11.60 | 10.76 | 3.26 | 2.77 | 13.84 | 12.99 | ns |
| | –1 | 0.56 | 9.69 | 0.04 | 1.23 | 1.62 | 0.36 | 9.87 | 9.15 | 2.77 | 2.36 | 11.77 | 11.05 | ns |
| | –2 | 0.49 | 8.51 | 0.03 | 1.08 | 1.42 | 0.32 | 8.66 | 8.03 | 2.43 | 2.07 | 10.33 | 9.70 | ns |
| 6 mA | Std. | 0.66 | 8.97 | 0.04 | 1.45 | 1.91 | 0.43 | 9.14 | 8.10 | 3.57 | 3.36 | 11.37 | 10.33 | ns |
| | –1 | 0.56 | 7.63 | 0.04 | 1.23 | 1.62 | 0.36 | 7.77 | 6.89 | 3.04 | 2.86 | 9.67 | 8.79 | ns |
| | –2 | 0.49 | 6.70 | 0.03 | 1.08 | 1.42 | 0.32 | 6.82 | 6.05 | 2.66 | 2.51 | 8.49 | 7.72 | ns |
| 8 mA | Std. | 0.66 | 8.35 | 0.04 | 1.45 | 1.91 | 0.43 | 8.50 | 7.59 | 3.64 | 3.52 | 10.74 | 9.82 | ns |
| | –1 | 0.56 | 7.10 | 0.04 | 1.23 | 1.62 | 0.36 | 7.23 | 6.45 | 3.10 | 3.00 | 9.14 | 8.35 | ns |
| | –2 | 0.49 | 6.24 | 0.03 | 1.08 | 1.42 | 0.32 | 6.35 | 5.66 | 2.72 | 2.63 | 8.02 | 7.33 | ns |
| 12 mA | Std. | 0.66 | 7.94 | 0.04 | 1.45 | 1.91 | 0.43 | 8.09 | 7.56 | 3.74 | 4.11 | 10.32 | 9.80 | ns |
| | –1 | 0.56 | 6.75 | 0.04 | 1.23 | 1.62 | 0.36 | 6.88 | 6.43 | 3.18 | 3.49 | 8.78 | 8.33 | ns |
| | –2 | 0.49 | 5.93 | 0.03 | 1.08 | 1.42 | 0.32 | 6.04 | 5.65 | 2.79 | 3.07 | 7.71 | 7.32 | ns |
| 16 mA | Std. | 0.66 | 7.94 | 0.04 | 1.45 | 1.91 | 0.43 | 8.09 | 7.56 | 3.74 | 4.11 | 10.32 | 9.80 | ns |
| | –1 | 0.56 | 6.75 | 0.04 | 1.23 | 1.62 | 0.36 | 6.88 | 6.43 | 3.18 | 3.49 | 8.78 | 8.33 | ns |
| | –2 | 0.49 | 5.93 | 0.03 | 1.08 | 1.42 | 0.32 | 6.04 | 5.65 | 2.79 | 3.07 | 7.71 | 7.32 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

# Differential I/O Characteristics

## Physical Implementation

Configuration of the I/O modules as a differential pair is handled by the Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and DDR. However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

## LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-22. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3E also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

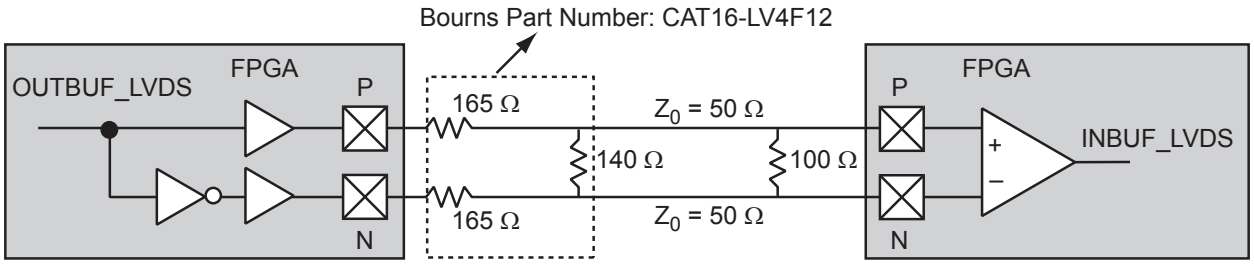



***Figure 2-22 •*** **LVDS Circuit Diagram and Board-Level Implementation**

## DDR Module Specifications

### *Input DDR Module*

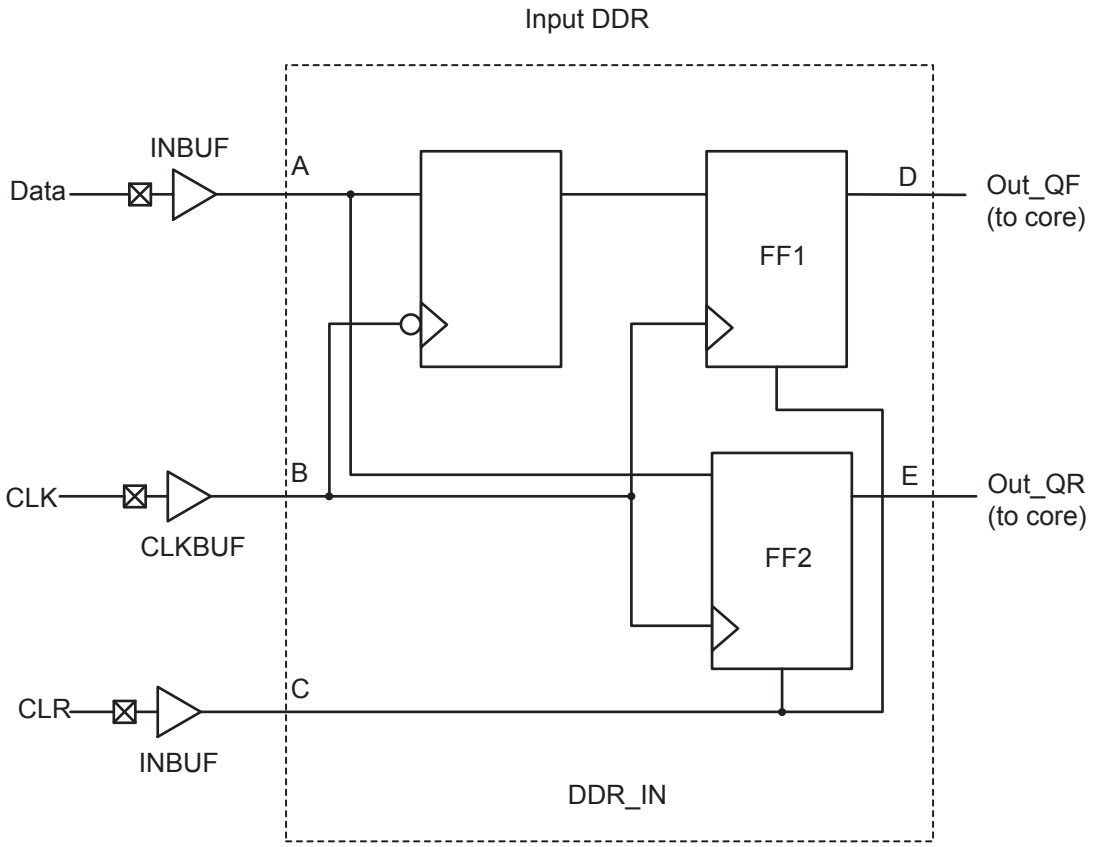



***Figure 2-30 •*** **Input DDR Timing Model**

***Table 2-89 •*** **Parameter Definitions**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|---|---|---|
| $t_{DDRICLKQ1}$ | Clock-to-Out Out_QR | B, D |
| $t_{DDRICLKQ2}$ | Clock-to-Out Out_QF | B, E |
| $t_{DDRISUD}$ | Data Setup Time of DDR input | A, B |
| $t_{DDRIHD}$ | Data Hold Time of DDR input | A, B |
| $t_{DDRICLR2Q1}$ | Clear-to-Out Out_QR | C, D |
| $t_{DDRICLR2Q2}$ | Clear-to-Out Out_QF | C, E |
| $t_{DDRIREMCLR}$ | Clear Removal | C, B |
| $t_{DDRIRECCLR}$ | Clear Recovery | C, B |

## Output DDR Module

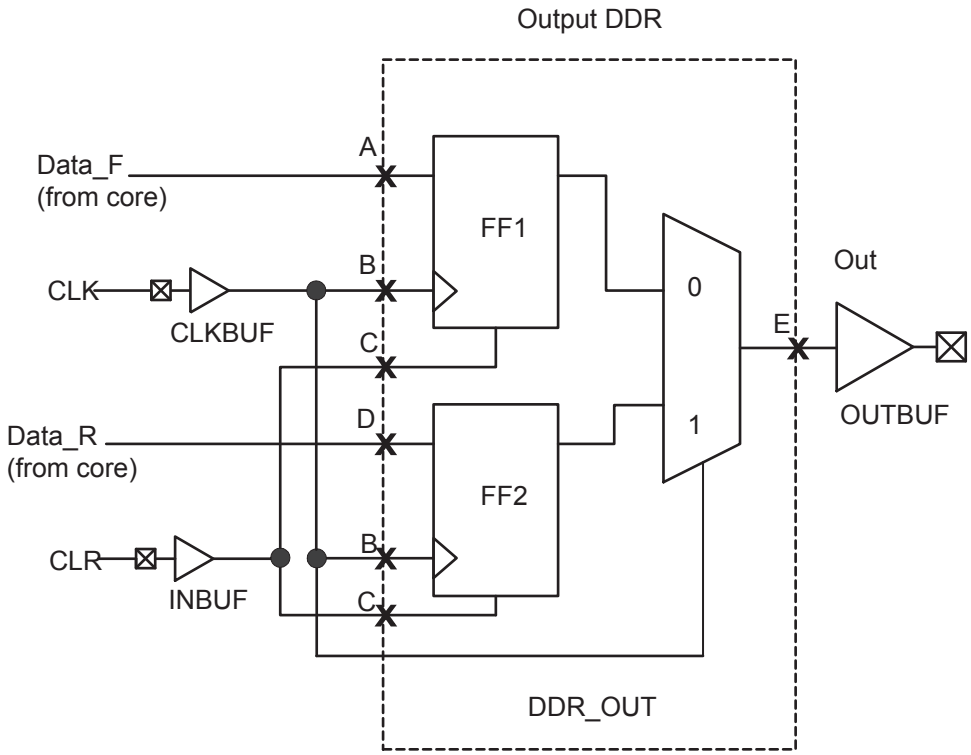



***Figure 2-32 •*** **Output DDR Timing Model**

***Table 2-91 •*** **Parameter Definitions**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out | B, E |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out | C, E |
| $t_{DDROREMCLR}$ | Clear Removal | C, B |
| $t_{DDRORECCLR}$ | Clear Recovery | C, B |
| $t_{DDROSUD1}$ | Data Setup Data_F | A, B |
| $t_{DDROSUD2}$ | Data Setup Data_R | D, B |
| $t_{DDROHD1}$ | Data Hold Data_F | A, B |
| $t_{DDROHD2}$ | Data Hold Data_R | D, B |

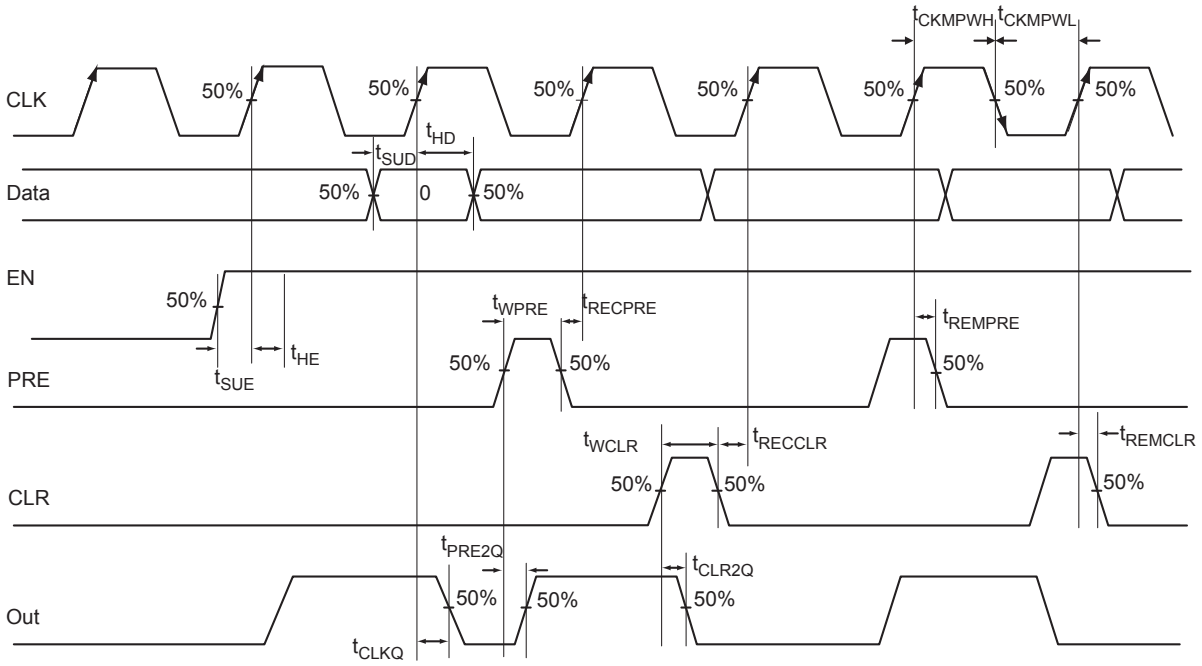



***Figure 2-37 •*** **Timing Model and Waveforms**

## Timing Characteristics

***Table 2-94 •*** **Register Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{CLKQ}$ | Clock-to-Q of the Core Register | 0.55 | 0.63 | 0.74 | ns |
| $t_{SUD}$ | Data Setup Time for the Core Register | 0.43 | 0.49 | 0.57 | ns |
| $t_{HD}$ | Data Hold Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{SUE}$ | Enable Setup Time for the Core Register | 0.45 | 0.52 | 0.61 | ns |
| $t_{HE}$ | Enable Hold Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{CLR2Q}$ | Asynchronous Clear-to-Q of the Core Register | 0.40 | 0.45 | 0.53 | ns |
| $t_{PRE2Q}$ | Asynchronous Preset-to-Q of the Core Register | 0.40 | 0.45 | 0.53 | ns |
| $t_{REMCLR}$ | Asynchronous Clear Removal Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{RECCLR}$ | Asynchronous Clear Recovery Time for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{REMPRE}$ | Asynchronous Preset Removal Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{RECPRE}$ | Asynchronous Preset Recovery Time for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{WCLR}$ | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{WPRE}$ | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{CKMPWH}$ | Clock Minimum Pulse Width High for the Core Register | 0.32 | 0.37 | 0.43 | ns |
| $t_{CKMPWL}$ | Clock Minimum Pulse Width Low for the Core Register | 0.36 | 0.41 | 0.48 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

| PQ208 | |
|---|---|
| **Pin Number** | **A3PE600 Function** |
| 1 | GND |
| 2 | GNDQ |
| 3 | VMV7 |
| 4 | GAB2/IO133PSB7V1 |
| 5 | GAA2/IO134PDB7V1 |
| 6 | IO134NDB7V1 |
| 7 | GAC2/IO132PDB7V1 |
| 8 | IO132NDB7V1 |
| 9 | IO130PDB7V1 |
| 10 | IO130NDB7V1 |
| 11 | IO127PDB7V1 |
| 12 | IO127NDB7V1 |
| 13 | IO126PDB7V0 |
| 14 | IO126NDB7V0 |
| 15 | IO124PSB7V0 |
| 16 | VCC |
| 17 | GND |
| 18 | VCCIB7 |
| 19 | IO122PPB7V0 |
| 20 | IO121PSB7V0 |
| 21 | IO122NPB7V0 |
| 22 | GFC1/IO120PSB7V0 |
| 23 | GFB1/IO119PDB7V0 |
| 24 | GFB0/IO119NDB7V0 |
| 25 | VCOMPLF |
| 26 | GFA0/IO118NPB6V1 |
| 27 | VCCPLF |
| 28 | GFA1/IO118PPB6V1 |
| 29 | GND |
| 30 | GFA2/IO117PDB6V1 |
| 31 | IO117NDB6V1 |
| 32 | GFB2/IO116PPB6V1 |
| 33 | GFC2/IO115PPB6V1 |
| 34 | IO116NPB6V1 |
| 35 | IO115NPB6V1 |
| 36 | VCC |

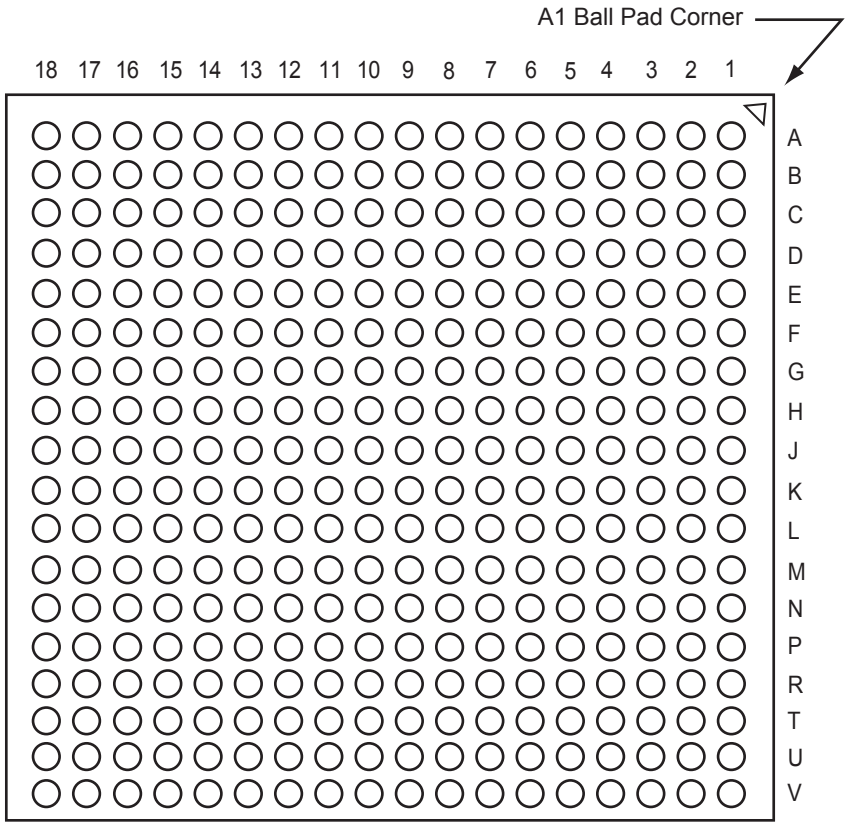
| PQ208 | |
|---|---|
| **Pin Number** | **A3PE600 Function** |
| 37 | IO112PDB6V1 |
| 38 | IO112NDB6V1 |
| 39 | IO108PSB6V0 |
| 40 | VCCIB6 |
| 41 | GND |
| 42 | IO106PDB6V0 |
| 43 | IO106NDB6V0 |
| 44 | GEC1/IO104PDB6V0 |
| 45 | GEC0/IO104NDB6V0 |
| 46 | GEB1/IO103PPB6V0 |
| 47 | GEA1/IO102PPB6V0 |
| 48 | GEB0/IO103NPB6V0 |
| 49 | GEA0/IO102NPB6V0 |
| 50 | VMV6 |
| 51 | GNDQ |
| 52 | GND |
| 53 | VMV5 |
| 54 | GNDQ |
| 55 | IO101NDB5V2 |
| 56 | GEA2/IO101PDB5V2 |
| 57 | IO100NDB5V2 |
| 58 | GEB2/IO100PDB5V2 |
| 59 | IO99NDB5V2 |
| 60 | GEC2/IO99PDB5V2 |
| 61 | IO98PSB5V2 |
| 62 | VCCIB5 |
| 63 | IO96PSB5V2 |
| 64 | IO94NDB5V1 |
| 65 | GND |
| 66 | IO94PDB5V1 |
| 67 | IO92NDB5V1 |
| 68 | IO92PDB5V1 |
| 69 | IO88NDB5V0 |
| 70 | IO88PDB5V0 |
| 71 | VCC |

| PQ208 | |
|---|---|
| **Pin Number** | **A3PE600 Function** |
| 72 | VCCIB5 |
| 73 | IO85NPB5V0 |
| 74 | IO84NPB5V0 |
| 75 | IO85PPB5V0 |
| 76 | IO84PPB5V0 |
| 77 | IO83NPB5V0 |
| 78 | IO82NPB5V0 |
| 79 | IO83PPB5V0 |
| 80 | IO82PPB5V0 |
| 81 | GND |
| 82 | IO80NDB4V1 |
| 83 | IO80PDB4V1 |
| 84 | IO79NPB4V1 |
| 85 | IO78NPB4V1 |
| 86 | IO79PPB4V1 |
| 87 | IO78PPB4V1 |
| 88 | VCC |
| 89 | VCCIB4 |
| 90 | IO76NDB4V1 |
| 91 | IO76PDB4V1 |
| 92 | IO72NDB4V0 |
| 93 | IO72PDB4V0 |
| 94 | IO70NDB4V0 |
| 95 | GDC2/IO70PDB4V0 |
| 96 | IO68NDB4V0 |
| 97 | GND |
| 98 | GDA2/IO68PDB4V0 |
| 99 | GDB2/IO69PSB4V0 |
| 100 | GNDQ |
| 101 | TCK |
| 102 | TDI |
| 103 | TMS |
| 104 | VMV4 |
| 105 | GND |
| 106 | VPUMP |
| 107 | GNDQ |

| FG256 | |
|---|---|
| **Pin Number** | **A3PE600 Function** |
| P9 | IO82PDB5V0 |
| P10 | IO76NDB4V1 |
| P11 | IO76PDB4V1 |
| P12 | VMV4 |
| P13 | TCK |
| P14 | VPUMP |
| P15 | TRST |
| P16 | GDA0/IO67NDB3V1 |
| R1 | GEA1/IO102PDB6V0 |
| R2 | GEA0/IO102NDB6V0 |
| R3 | GNDQ |
| R4 | GEC2/IO99PDB5V2 |
| R5 | IO95NPB5V1 |
| R6 | IO91NDB5V1 |
| R7 | IO91PDB5V1 |
| R8 | IO83NDB5V0 |
| R9 | IO83PDB5V0 |
| R10 | IO77NDB4V1 |
| R11 | IO77PDB4V1 |
| R12 | IO69NDB4V0 |
| R13 | GDB2/IO69PDB4V0 |
| R14 | TDI |
| R15 | GNDQ |
| R16 | TDO |
| T1 | GND |
| T2 | IO100NDB5V2 |
| T3 | GEB2/IO100PDB5V2 |
| T4 | IO99NDB5V2 |
| T5 | IO88NDB5V0 |
| T6 | IO88PDB5V0 |
| T7 | IO89NSB5V0 |
| T8 | IO80NSB4V1 |
| T9 | IO81NDB4V1 |
| T10 | IO81PDB4V1 |
| T11 | IO70NDB4V0 |
| T12 | GDC2/IO70PDB4V0 |

| FG256 | |
|---|---|
| **Pin Number** | **A3PE600 Function** |
| T13 | IO68NDB4V0 |
| T14 | GDA2/IO68PDB4V0 |
| T15 | TMS |
| T16 | GND |

# FG324




*Note: This is the bottom view of the package.*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/products/fpga-soc/solutions*.

| FG896 | |
|---|---|
| Pin Number | A3PE3000 Function |
| A2 | GND |
| A3 | GND |
| A4 | IO14NPB0V1 |
| A5 | GND |
| A6 | IO07NPB0V0 |
| A7 | GND |
| A8 | IO09NDB0V1 |
| A9 | IO17NDB0V2 |
| A10 | IO17PDB0V2 |
| A11 | IO21NDB0V2 |
| A12 | IO21PDB0V2 |
| A13 | IO33NDB0V4 |
| A14 | IO33PDB0V4 |
| A15 | IO35NDB0V4 |
| A16 | IO35PDB0V4 |
| A17 | IO41NDB1V0 |
| A18 | IO43NDB1V0 |
| A19 | IO43PDB1V0 |
| A20 | IO45NDB1V0 |
| A21 | IO45PDB1V0 |
| A22 | IO57NDB1V2 |
| A23 | IO57PDB1V2 |
| A24 | GND |
| A25 | IO69PPB1V3 |
| A26 | GND |
| A27 | GBC1/IO79PPB1V4 |
| A28 | GND |
| A29 | GND |
| AA1 | IO256PDB6V2 |
| AA2 | IO248PDB6V1 |
| AA3 | IO248NDB6V1 |
| AA4 | IO246NDB6V1 |
| AA5 | GEA1/IO234PDB6V0 |
| AA6 | GEA0/IO234NDB6V0 |
| AA7 | IO243PPB6V1 |
| AA8 | IO245NDB6V1 |

| FG896 | |
|---|---|
| Pin Number | A3PE3000 Function |
| AA9 | GEB1/IO235PPB6V0 |
| AA10 | VCC |
| AA11 | IO226PPB5V4 |
| AA12 | VCCIB5 |
| AA13 | VCCIB5 |
| AA14 | VCCIB5 |
| AA15 | VCCIB5 |
| AA16 | VCCIB4 |
| AA17 | VCCIB4 |
| AA18 | VCCIB4 |
| AA19 | VCCIB4 |
| AA20 | IO174PDB4V2 |
| AA21 | VCC |
| AA22 | IO142NPB3V3 |
| AA23 | IO144NDB3V3 |
| AA24 | IO144PDB3V3 |
| AA25 | IO146NDB3V4 |
| AA26 | IO146PDB3V4 |
| AA27 | IO147PDB3V4 |
| AA28 | IO139NDB3V3 |
| AA29 | IO139PDB3V3 |
| AA30 | IO133NDB3V2 |
| AB1 | IO256NDB6V2 |
| AB2 | IO244PDB6V1 |
| AB3 | IO244NDB6V1 |
| AB4 | IO241PDB6V0 |
| AB5 | IO241NDB6V0 |
| AB6 | IO243NPB6V1 |
| AB7 | VCCIB6 |
| AB8 | VCCPLE |
| AB9 | VCC |
| AB10 | IO222PDB5V3 |
| AB11 | IO218PPB5V3 |
| AB12 | IO206NDB5V1 |
| AB13 | IO206PDB5V1 |
| AB14 | IO198NDB5V0 |

| FG896 | |
|---|---|
| Pin Number | A3PE3000 Function |
| AB15 | IO198PDB5V0 |
| AB16 | IO192NDB4V4 |
| AB17 | IO192PDB4V4 |
| AB18 | IO178NDB4V3 |
| AB19 | IO178PDB4V3 |
| AB20 | IO174NDB4V2 |
| AB21 | IO162NPB4V1 |
| AB22 | VCC |
| AB23 | VCCPLD |
| AB24 | VCCIB3 |
| AB25 | IO150PDB3V4 |
| AB26 | IO148PDB3V4 |
| AB27 | IO147NDB3V4 |
| AB28 | IO145PDB3V3 |
| AB29 | IO143PDB3V3 |
| AB30 | IO137PDB3V2 |
| AC1 | IO254PDB6V2 |
| AC2 | IO254NDB6V2 |
| AC3 | IO240PDB6V0 |
| AC4 | GEC1/IO236PDB6V0 |
| AC5 | IO237PDB6V0 |
| AC6 | IO237NDB6V0 |
| AC7 | VCOMPLE |
| AC8 | GND |
| AC9 | IO226NPB5V4 |
| AC10 | IO222NDB5V3 |
| AC11 | IO216NPB5V2 |
| AC12 | IO210NPB5V2 |
| AC13 | IO204NDB5V1 |
| AC14 | IO204PDB5V1 |
| AC15 | IO194NDB5V0 |
| AC16 | IO188NDB4V4 |
| AC17 | IO188PDB4V4 |
| AC18 | IO182PPB4V3 |
| AC19 | IO170NPB4V2 |
| AC20 | IO164NDB4V1 |

| Revision | Changes | Page |
|---|---|---|
| v2.0 (continued) | Table 3-6 • Temperature and Voltage Derating Factors for Timing Delays was updated. | 3-5 |
| | Table 3-5 • Package Thermal Resistivities was updated. | 3-5 |
| | Table 3-10 • Different Components Contributing to the Dynamic Power Consumption in ProASIC3E Devices was updated. | 3-8 |
| | $t_{WRO}$ and $t_{CCKH}$ were added to Table 3-94 • RAM4K9 and Table 3-95 • RAM512X18. | 3-74 to 3-74 |
| | The note in Table 3-24 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was updated. | 3-23 |
| | Figure 3-43 • Write Access After Write onto Same Address, Figure 3-44 • Read Access After Write onto Same Address, and Figure 3-45 • Write Access After Read onto Same Address are new. | 3-71 to 3-73 |
| | Figure 3-53 • Timing Diagram was updated. | 3-80 |
| | Notes were added to the package diagrams identifying if they were top or bottom view. | N/A |
| | The A3PE1500 "208-Pin PQFP" table is new. | 4-4 |
| | The A3PE1500 "484-Pin FBGA" table is new. | 4-18 |
| | The A3PE1500 "A3PE1500 Function" table is new. | 4-24 |
| Advance v0.6 (January 2007) | In the "Packaging Tables" table, the number of I/Os for the A3PE1500 was changed for the FG484 and FG676 packages. | ii |
| Advance v0.5 (April 2006) | B-LVDS and M-LDVS are new I/O standards added to the datasheet. | N/A |
| | The term flow-through was changed to pass-through. | N/A |
| | Figure 2-8 • Very-Long-Line Resources was updated. | 2-8 |
| | The footnotes in Figure 2-27 • CCC/PLL Macro were updated. | 2-28 |
| | The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options. | 2-24 |
| | The "SRAM and FIFO" section was updated. | 2-21 |
| | The "RESET" section was updated. | 2-25 |
| | The "WCLK and RCLK" section was updated. | 2-25 |
| | The "RESET" section was updated. | 2-25 |
| | The "RESET" section was updated. | 2-27 |
| | B-LVDS and M-LDVS are new I/O standards added to the datasheet. | N/A |
| | The term flow-through was changed to pass-through. | N/A |
| | Figure 2-8 • Very-Long-Line Resources was updated. | 2-8 |
| | The footnotes in Figure 2-27 • CCC/PLL Macro were updated. | 2-28 |
| | The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options. | 2-24 |
| | The "SRAM and FIFO" section was updated. | 2-21 |
| | The "RESET" section was updated. | 2-25 |
| | The "WCLK and RCLK" section was updated. | 2-25 |