Microchip Technology - A3PE3000-2FG896 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	516096
Number of I/O	620
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3pe3000-2fg896

VersaTiles

The ProASIC3E core consists of VersaTiles, which have been enhanced beyond the ProASIC<u>PLUS</u>® core tiles. The ProASIC3E VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-2 for VersaTile configurations.

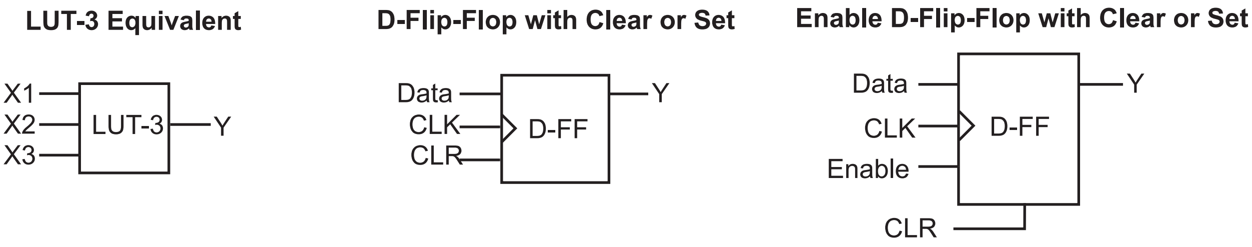

Figure 1-2 • **VersaTile Configurations**

User Nonvolatile FlashROM

ProASIC3E devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3E IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC3E development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

Table 2-17 • **Summary of I/O Timing Characteristics—Software Default Settings**
–2 Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option)[1]	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)
3.3 V LVTTL / 3.3 V LVCMOS	12	12	High	35	–	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81
3.3 V LVCMOS Wide Range[2]	100 µA	12	High	35	–	0.49	4.24	0.03	1.36	1.78	0.32	4.24	3.25	3.78	4.17	6.77	5.79
2.5 V LVCMOS	12	12	High	35	–	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28
1.8 V LVCMOS	12	12	High	35	–	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98
1.5 V LVCMOS	12	12	High	35	–	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37
3.3 V PCI	Per PCI spec	–	High	10	25 [3]	0.49	2.09	0.03	0.78	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16
3.3 V PCI-X	Per PCI-X spec	–	High	10	25[3]	0.49	2.09	0.03	0.78	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16
3.3 V GTL	20 [4]	–	High	10	25	0.45	1.55	0.03	2.19	–	0.32	1.52	1.55	–	–	3.19	3.22
2.5 V GTL	20 [4]	–	High	10	25	0.45	1.59	0.03	1.83	–	0.32	1.61	1.59	–	–	3.28	3.26
3.3 V GTL+	35	–	High	10	25	0.45	1.53	0.03	1.19	–	0.32	1.56	1.53	–	–	3.23	3.20
2.5 V GTL+	33	–	High	10	25	0.45	1.65	0.03	1.13	–	0.32	1.68	1.57	–	–	3.35	3.24
HSTL (I)	8	–	High	20	50	0.49	2.37	0.03	1.59	–	0.32	2.42	2.35	–	–	4.09	4.02
HSTL (II)	15 [4]	–	High	20	25	0.49	2.26	0.03	1.59	–	0.32	2.30	2.03	–	–	3.97	3.70
SSTL2 (I)	15	–	High	30	50	0.49	1.59	0.03	1.00	–	0.32	1.62	1.38	–	–	3.29	3.05
SSTL2 (II)	18	–	High	30	25	0.49	1.62	0.03	1.00	–	0.32	1.65	1.32	–	–	3.32	2.99
SSTL3 (I)	14	–	High	30	50	0.49	1.72	0.03	0.93	–	0.32	1.75	1.37	–	–	3.42	3.04
SSTL3 (II)	21	–	High	30	25	0.49	1.54	0.03	0.93	–	0.32	1.57	1.25	–	–	3.24	2.92
LVDS/B-LVDS/ M-LVDS	24	–	High	–	–	0.49	1.40	0.03	1.36	–	–	–	–	–	–	–	–
LVPECL	24	–	High	–	–	0.49	1.36	0.03	1.22	–	–	–	–	–	–	–	–

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3V wide range as specified in the JESD8b specification.*
3. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-38 for connectivity. This resistor is not required during normal operation.*
4. *Output drive strength is below JEDEC specification.*
5. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5.*

Table 2-22 • **Duration of Short Circuit Event Before Failure (continued)**

Temperature	Time before Failure
85°C	2 years
100°C	6 months

Table 2-23 • **Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

Table 2-24 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability***

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns *	20 years (110°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis.	20 years (110°C)
HSTL/SSTL/GTL	No requirement	10 ns *	10 years (100°C)
LVDS/B-LVDS/M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

*Note: *For clock signals and similar edge-generating signals, refer to the "ProASIC3/E SSO and Pin Placement Guidelines" chapter of the ProASIC3E FPGA Fabric User's Guide. The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

Timing Characteristics

Table 2-27 **• 3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	7.88	0.04	1.20	1.57	0.43	8.03	6.70	2.69	2.59	10.26	8.94	ns
	–1	0.56	6.71	0.04	1.02	1.33	0.36	6.83	5.70	2.29	2.20	8.73	7.60	ns
	–2	0.49.	5.89	0.03	0.90	1.17	0.32	6.00	5.01	2.01	1.93	7.67	6.67	ns
4 mA	Std.	0.66	7.88	0.04	1.20	1.57	0.43	8.03	6.70	2.69	2.59	10.26	8.94	ns
	–1	0.56	6.71	0.04	1.02	1.33	0.36	6.83	5.70	2.29	2.20	8.73	7.60	ns
	–2	0.49	5.89	0.03	0.90	1.17	0.32	6.00	5.01	2.01	1.93	7.67	6.67	ns
6 mA	Std.	0.66	5.08	0.04	1.20	1.57	0.43	5.17	4.14	3.05	3.21	7.41	6.38	ns
	–1	0.56	4.32	0.04	1.02	1.33	0.36	4.40	3.52	2.59	2.73	6.30	5.43	ns
	–2	0.49	3.79	0.03	0.90	1.17	0.32	3.86	3.09	2.28	2.40	5.53	4.76	ns
8 mA	Std.	0.66	5.08	0.04	1.20	1.57	0.43	5.17	4.14	3.05	3.21	7.41	6.38	ns
	–1	0.56	4.32	0.04	1.02	1.33	0.36	4.40	3.52	2.59	2.73	6.30	5.43	ns
	–2	0.49	3.79	0.03	0.90	1.17	0.32	3.86	3.09	2.28	2.40	5.53	4.76	ns
12 mA	Std.	0.66	3.67	0.04	1.20	1.57	0.43	3.74	2.87	3.28	3.61	5.97	5.11	ns
	–1	0.56	3.12	0.04	1.02	1.33	0.36	3.18	2.44	2.79	3.07	5.08	4.34	ns
	–2	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81	ns
16 mA	Std.	0.66	3.46	0.04	1.20	1.57	0.43	3.53	2.61	3.33	3.72	5.76	4.84	ns
	–1	0.56	2.95	0.04	1.02	1.33	0.36	3.00	2.22	2.83	3.17	4.90	4.12	ns
	–2	0.49	2.59	0.03	0.90	1.17	0.32	2.63	1.95	2.49	2.78	4.30	3.62	ns
24 mA	Std.	0.66	3.21	0.04	1.20	1.57	0.43	3.27	2.16	3.39	4.13	5.50	4.39	ns
	–1	0.56	2.73	0.04	1.02	1.33	0.36	2.78	1.83	2.88	3.51	4.68	3.74	ns
	–2	0.49	2.39	0.03	0.90	1.17	0.32	2.44	1.61	2.53	3.08	4.11	3.28	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

Table 2-28 **• 3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	11.01	0.04	1.20	1.57	0.43	11.21	9.05	2.69	2.44	13.45	11.29	ns
	–1	0.56	9.36	0.04	1.02	1.33	0.36	9.54	7.70	2.29	2.08	11.44	9.60	ns
	–2	0.49	8.22	0.03	0.90	1.17	0.32	8.37	6.76	2.01	1.82	10.04	8.43	ns
4 mA	Std.	0.66	11.01	0.04	1.20	1.57	0.43	11.21	9.05	2.69	2.44	13.45	11.29	ns
	–1	0.56	9.36	0.04	1.02	1.33	0.36	9.54	7.70	2.29	2.08	11.44	9.60	ns
	–2	0.49	8.22	0.03	0.90	1.17	0.32	8.37	6.76	2.01	1.82	10.04	8.43	ns
6 mA	Std.	0.66	7.86	0.04	1.20	1.57	0.43	8.01	6.44	3.04	3.06	10.24	8.68	ns
	–1	0.56	6.69	0.04	1.02	1.33	0.36	6.81	5.48	2.58	2.61	8.71	7.38	ns
	–2	0.49	5.87	0.03	0.90	1.17	0.32	5.98	4.81	2.27	2.29	7.65	6.48	ns
8 mA	Std.	0.66	7.86	0.04	1.20	1.57	0.43	8.01	6.44	3.04	3.06	10.24	8.68	ns
	–1	0.56	6.69	0.04	1.02	1.33	0.36	6.81	5.48	2.58	2.61	8.71	7.38	ns
	–2	0.49	5.87	0.03	0.90	1.17	0.32	5.98	4.81	2.27	2.29	7.65	6.48	ns

Timing Characteristics

Table 2-31 **• 3.3 V LVCMOS Wide Range High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	4 mA	Std.	0.66	12.19	0.04	1.83	2.38	0.43	12.19	10.17	4.16	4.00	15.58	13.57	ns
		–1	0.56	10.37	0.04	1.55	2.02	0.36	10.37	8.66	3.54	3.41	13.26	11.54	ns
		–2	0.49	9.10	0.03	1.36	1.78	0.32	9.10	7.60	3.11	2.99	11.64	10.13	ns
100 µA	8 mA	Std.	0.66	7.85	0.04	1.83	2.38	0.43	7.85	6.29	4.71	4.97	11.24	9.68	ns
		–1	0.56	6.68	0.04	1.55	2.02	0.36	6.68	5.35	4.01	4.22	9.57	8.24	ns
		–2	0.49	5.86	0.03	1.36	1.78	0.32	5.86	4.70	3.52	3.71	8.40	7.23	ns
100 µA	12 mA	Std.	0.66	5.67	0.04	1.83	2.38	0.43	5.67	4.36	5.06	5.59	9.07	7.75	ns
		–1	0.56	4.82	0.04	1.55	2.02	0.36	4.82	3.71	4.31	4.75	7.71	6.59	ns
		–2	0.49	4.24	0.03	1.36	1.78	0.32	4.24	3.25	3.78	4.17	6.77	5.79	ns
100 µA	16 mA	Std.	0.66	5.35	0.04	1.83	2.38	0.43	5.35	3.96	5.15	5.76	8.75	7.35	ns
		–1	0.56	4.55	0.04	1.55	2.02	0.36	4.55	3.36	4.38	4.90	7.44	6.25	ns
		–2	0.49	4.00	0.03	1.36	1.78	0.32	4.00	2.95	3.85	4.30	6.53	5.49	ns
100 µA	24 mA	Std.	0.66	4.96	0.04	1.83	2.38	0.43	4.96	3.27	5.23	6.38	8.35	6.67	ns
		–1	0.56	4.22	0.04	1.55	2.02	0.36	4.22	2.78	4.45	5.43	7.11	5.67	ns
		–2	0.49	3.70	0.03	1.36	1.78	0.32	3.70	2.44	3.91	4.76	6.24	4.98	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *Software default selection highlighted in gray.*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

***Table 2-32* • 3.3 V LVCMOS Wide Range Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	4 mA	Std.	0.66	17.02	0.04	1.83	2.38	0.43	17.02	13.74	4.16	3.78	20.42	17.14	ns
		–1	0.56	14.48	0.04	1.55	2.02	0.36	14.48	11.69	3.54	3.21	17.37	14.58	ns
		–2	0.49	12.71	0.03	1.36	1.78	0.32	12.71	10.26	3.11	2.82	15.25	12.80	ns
100 µA	8 mA	Std.	0.66	12.16	0.04	1.83	2.38	0.43	12.16	9.78	4.70	4.74	15.55	13.17	ns
		–1	0.56	10.34	0.04	1.55	2.02	0.36	10.34	8.32	4.00	4.03	13.23	11.20	ns
		–2	0.49	9.08	0.03	1.36	1.78	0.32	9.08	7.30	3.51	3.54	11.61	9.84	ns
100µA	12 mA	Std.	0.66	9.32	0.04	1.83	2.38	0.43	9.32	7.62	5.06	5.36	12.71	11.02	ns
		–1	0.56	7.93	0.04	1.55	2.02	0.36	7.93	6.48	4.31	4.56	10.81	9.37	ns
		–2	0.49	6.96	0.03	1.36	1.78	0.32	6.96	5.69	3.78	4.00	9.49	8.23	ns
100 µA	16 mA	Std.	0.66	8.69	0.04	1.83	2.38	0.43	8.69	7.17	5.14	5.53	12.08	10.57	ns
		–1	0.56	7.39	0.04	1.55	2.02	0.36	7.39	6.10	4.37	4.71	10.28	8.99	ns
		–2	0.49	6.49	0.03	1.36	1.78	0.32	6.49	5.36	3.83	4.13	9.02	7.89	ns
100 µA	24 mA	Std.	0.66	8.11	0.04	1.83	2.38	0.43	8.11	7.13	5.23	6.13	11.50	10.52	ns
		–1	0.56	6.90	0.04	1.55	2.02	0.36	6.90	6.06	4.45	5.21	9.78	8.95	ns
		–2	0.49	6.05	0.03	1.36	1.78	0.32	6.05	5.32	3.91	4.57	8.59	7.86	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *Software default selection highlighted in gray.*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

Timing Characteristics

***Table 2-35* • 2.5 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	8.82	0.04	1.51	1.66	0.43	8.13	8.82	2.72	2.29	10.37	11.05	ns
	–1	0.56	7.50	0.04	1.29	1.41	0.36	6.92	7.50	2.31	1.95	8.82	9.40	ns
	–2	0.49	6.58	0.03	1.13	1.24	0.32	6.07	6.58	2.03	1.71	7.74	8.25	ns
8 mA	Std.	0.66	5.27	0.04	1.51	1.66	0.43	5.27	5.27	3.10	3.03	7.50	7.51	ns
	–1	0.56	4.48	0.04	1.29	1.41	0.36	4.48	4.48	2.64	2.58	6.38	6.38	ns
	–2	0.49	3.94	0.03	1.13	1.24	0.32	3.93	3.94	2.32	2.26	5.60	5.61	ns
12 mA	Std.	0.66	3.74	0.04	1.51	1.66	0.43	3.81	3.49	3.37	3.49	6.05	5.73	ns
	–1	0.56	3.18	0.04	1.29	1.41	0.36	3.24	2.97	2.86	2.97	5.15	4.87	ns
	–2	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28	ns
16 mA	Std.	0.66	3.53	0.04	1.51	1.66	0.43	3.59	3.12	3.42	3.62	5.83	5.35	ns
	–1	0.56	3.00	0.04	1.29	1.41	0.36	3.06	2.65	2.91	3.08	4.96	4.55	ns
	–2	0.49	2.63	0.03	1.13	1.24	0.32	2.68	2.33	2.56	2.71	4.35	4.00	ns
24 mA	Std.	0.66	3.26	0.04	1.51	1.66	0.43	3.32	2.48	3.49	4.11	5.56	4.72	ns
	–1	0.56	2.77	0.04	1.29	1.41	0.36	2.83	2.11	2.97	3.49	4.73	4.01	ns
	–2	0.49	2.44	0.03	1.13	1.24	0.32	2.48	1.85	2.61	3.07	4.15	3.52	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

1.8 V LVCMOS

Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

***Table 2-37* • Minimum and Maximum DC Input and Output Levels**

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	11	9	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	22	17	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	6	6	44	35	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8	51	45	10	10
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12	74	91	10	10
16 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	16	16	74	91	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

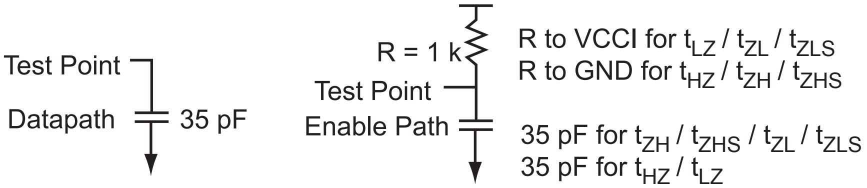

***Figure 2-9* • AC Loading**

***Table 2-38* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	1.8	0.9	–	35

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-43 • 1.5 V LVCMOS High Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	8.53	0.04	1.70	2.14	0.43	7.26	8.53	3.39	2.79	9.50	10.77	ns
	–1	0.56	7.26	0.04	1.44	1.82	0.36	6.18	7.26	2.89	2.37	8.08	9.16	ns
	–2	0.49	6.37	0.03	1.27	1.60	0.32	5.42	6.37	2.53	2.08	7.09	8.04	ns
4 mA	Std.	0.66	5.41	0.04	1.70	2.14	0.43	5.22	5.41	3.75	3.48	7.45	7.65	ns
	–1	0.56	4.60	0.04	1.44	1.82	0.36	4.44	4.60	3.19	2.96	6.34	6.50	ns
	–2	0.49	4.04	0.03	1.27	1.60	0.32	3.89	4.04	2.80	2.60	5.56	5.71	ns
6 mA	Std.	0.66	4.80	0.04	1.70	2.14	0.43	4.89	4.75	3.83	3.67	7.13	6.98	ns
	–1	0.56	4.09	0.04	1.44	1.82	0.36	4.16	4.04	3.26	3.12	6.06	5.94	ns
	–2	0.49	3.59	0.03	1.27	1.60	0.32	3.65	3.54	2.86	2.74	5.32	5.21	ns
8 mA	Std.	0.66	4.42	0.04	1.70	2.14	0.43	4.50	3.62	3.96	4.37	6.74	5.86	ns
	–1	0.56	3.76	0.04	1.44	1.82	0.36	3.83	3.08	3.37	3.72	5.73	4.98	ns
	–2	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns
12 mA	Std.	0.66	4.42	0.04	1.70	2.14	0.43	4.50	3.62	3.96	4.37	6.74	5.86	ns
	–1	0.56	3.76	0.04	1.44	1.82	0.36	3.83	3.08	3.37	3.72	5.73	4.98	ns
	–2	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

Table 2-44 • 1.5 V LVCMOS Low Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	14.11	0.04	1.70	2.14	0.43	14.37	13.14	3.40	2.68	16.61	15.37	ns
	–1	0.56	12.00	0.04	1.44	1.82	0.36	12.22	11.17	2.90	2.28	14.13	13.08	ns
	–2	0.49	10.54	0.03	1.27	1.60	0.32	10.73	9.81	2.54	2.00	12.40	11.48	ns
4 mA	Std.	0.66	11.23	0.04	1.70	2.14	0.43	11.44	9.87	3.77	3.36	13.68	12.10	ns
	–1	0.56	9.55	0.04	1.44	1.82	0.36	9.73	8.39	3.21	2.86	11.63	10.29	ns
	–2	0.49	8.39	0.03	1.27	1.60	0.32	8.54	7.37	2.81	2.51	10.21	9.04	ns
6 mA	Std.	0.66	10.45	0.04	1.70	2.14	0.43	10.65	9.24	3.84	3.55	12.88	11.48	ns
	–1	0.56	8.89	0.04	1.44	1.82	0.36	9.06	7.86	3.27	3.02	10.96	9.76	ns
	–2	0.49	7.81	0.03	1.27	1.60	0.32	7.95	6.90	2.87	2.65	9.62	8.57	ns
8 mA	Std.	0.66	10.02	0.04	1.70	2.14	0.43	10.20	9.23	3.97	4.22	12.44	11.47	ns
	–1	0.56	8.52	0.04	1.44	1.82	0.36	8.68	7.85	3.38	3.59	10.58	9.75	ns
	–2	0.49	7.48	0.03	1.27	1.60	0.32	7.62	6.89	2.97	3.15	9.29	8.56	ns
12 mA	Std.	0.66	10.02	0.04	1.70	2.14	0.43	10.20	9.23	3.97	4.22	12.44	11.47	ns
	–1	0.56	8.52	0.04	1.44	1.82	0.36	8.68	7.85	3.38	3.59	10.58	9.75	ns
	–2	0.49	7.48	0.03	1.27	1.60	0.32	7.62	6.89	2.97	3.15	9.29	8.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

***Table 2-66* • Minimum and Maximum DC Input and Output Levels**

SSTL2 Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
15 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15	87	83	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

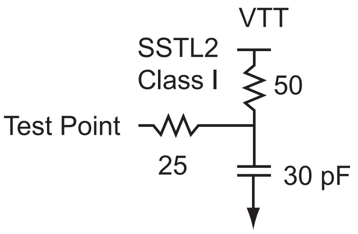

***Figure 2-18* • AC Loading**

***Table 2-67* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

***Table 2-68* • SSTL 2 Class I**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.13	0.04	1.33	0.43	2.17	1.85			4.40	4.08	ns
–1	0.56	1.81	0.04	1.14	0.36	1.84	1.57			3.74	3.47	ns
–2	0.49	1.59	0.03	1.00	0.32	1.62	1.38			3.29	3.05	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

Table 2-85 **• Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

Note: *See Figure 2-26 on page 2-55 for more information.

Input Register

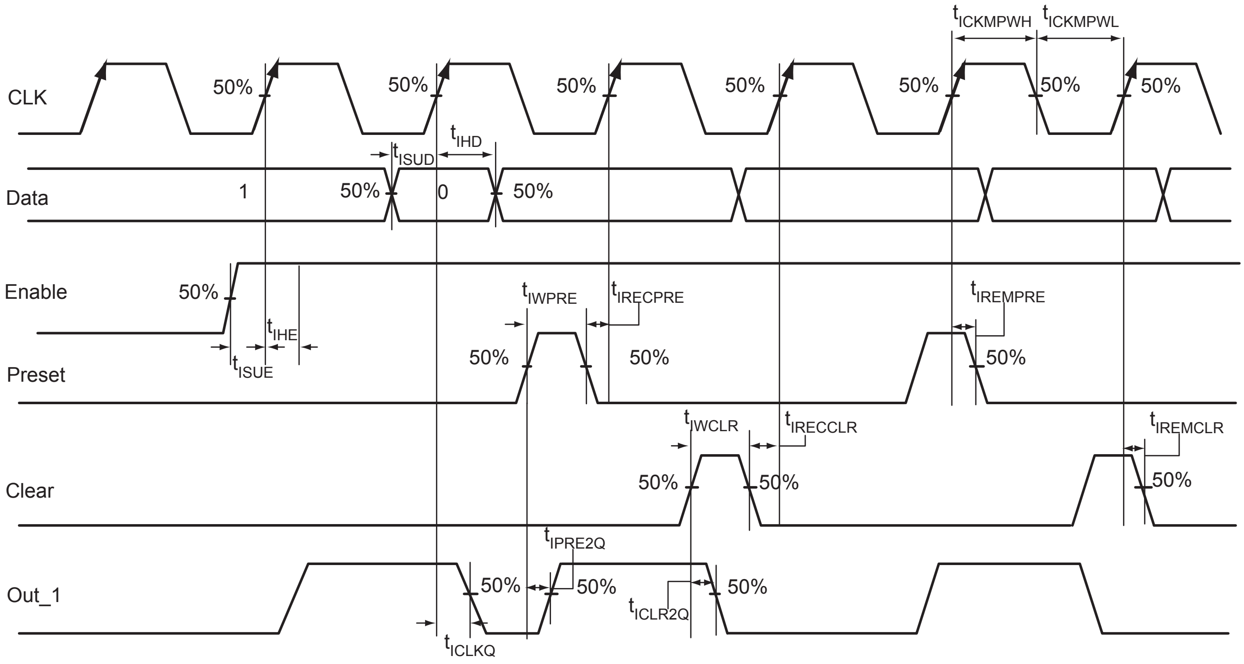

Figure 2-27 • **Input Register Timing Diagram**

Timing Characteristics

Table 2-86 • **Input Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.27	0.32	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.26	0.30	0.35	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.37	0.42	0.50	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.45	0.52	0.61	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.45	0.52	0.61	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.41	0.48	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.32	0.37	0.43	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

DDR Module Specifications

Input DDR Module

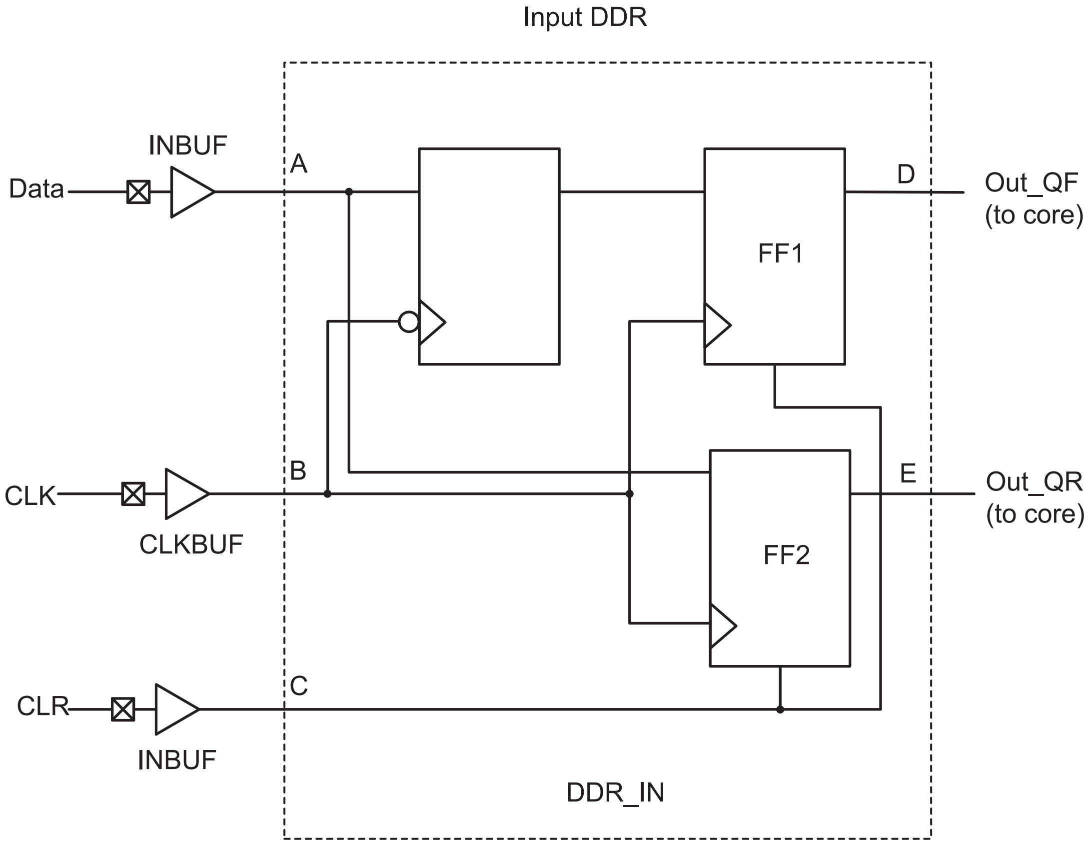

***Figure 2-30* • Input DDR Timing Model**

***Table 2-89* • Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

Timing Waveforms

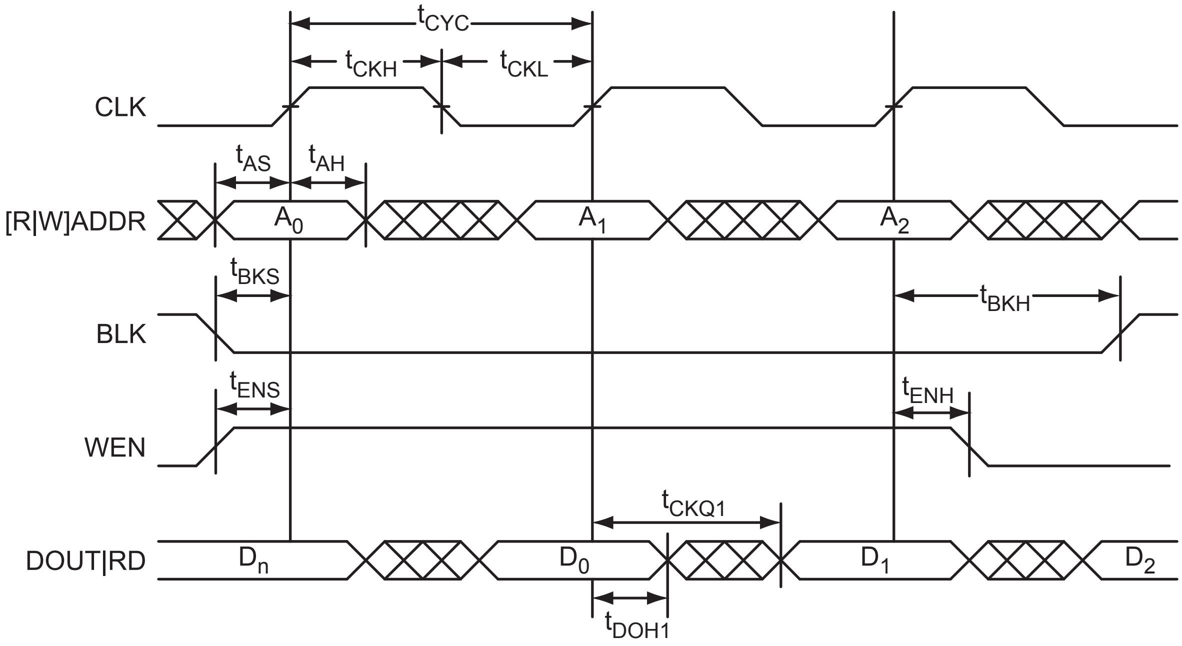

Figure 2-41 • **RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.**

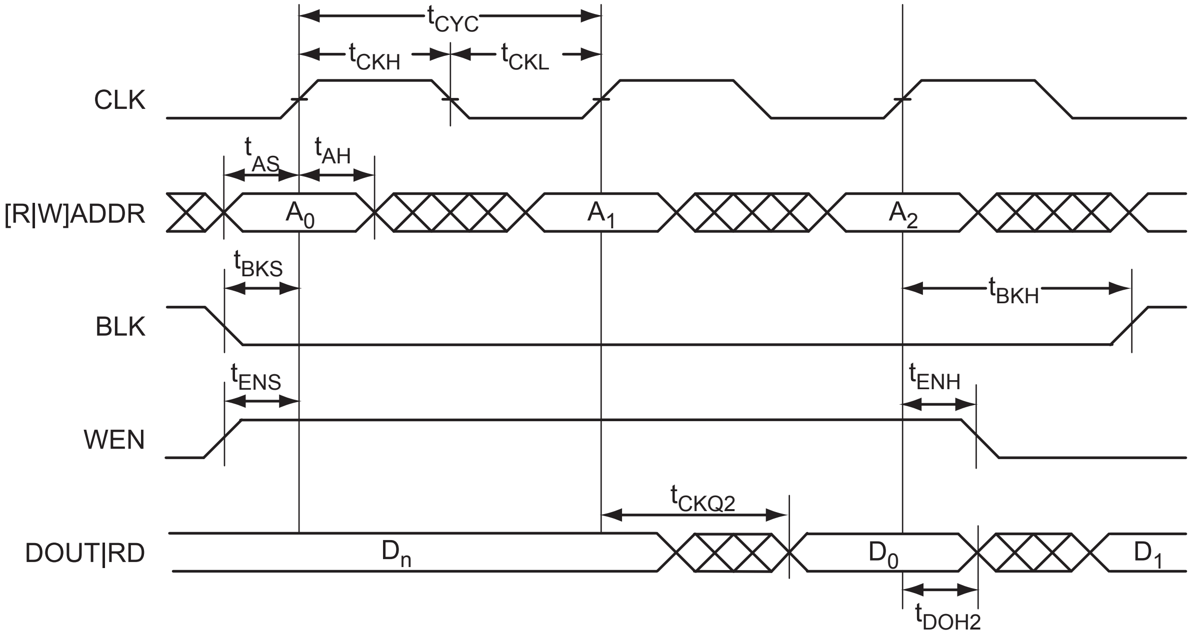

Figure 2-42 • **RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.**

Timing Waveforms

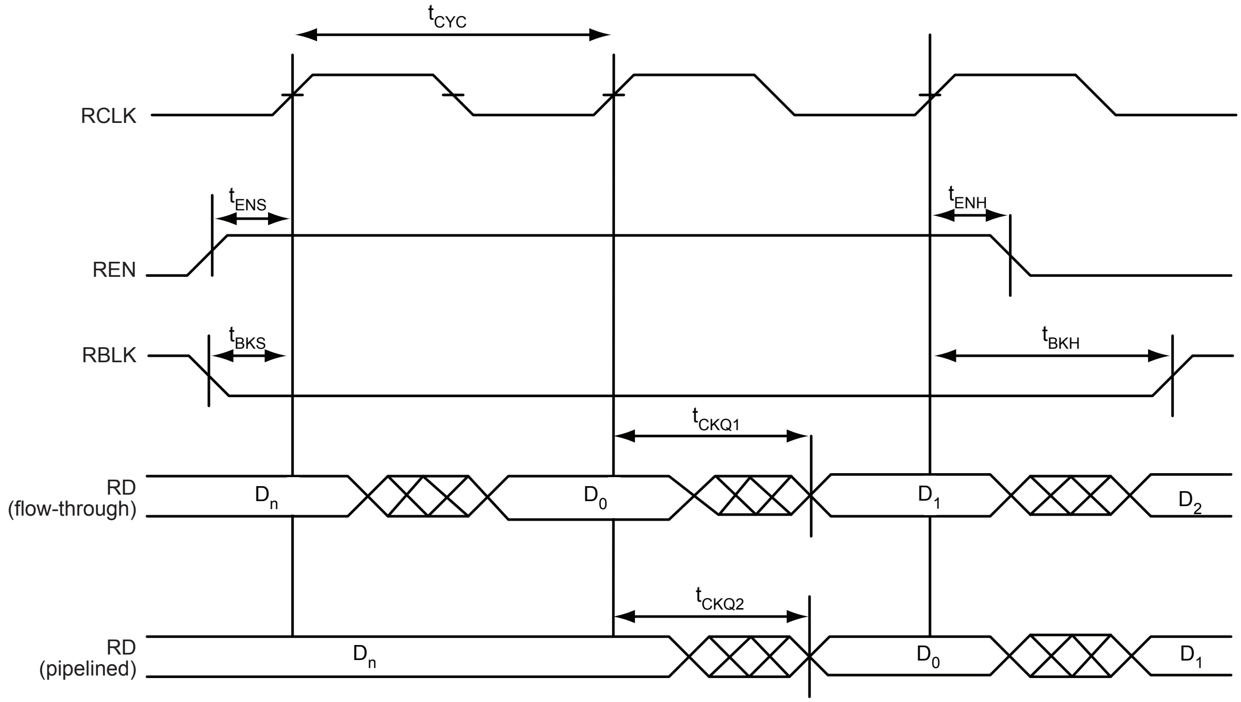

Figure 2-47 • **FIFO Read**

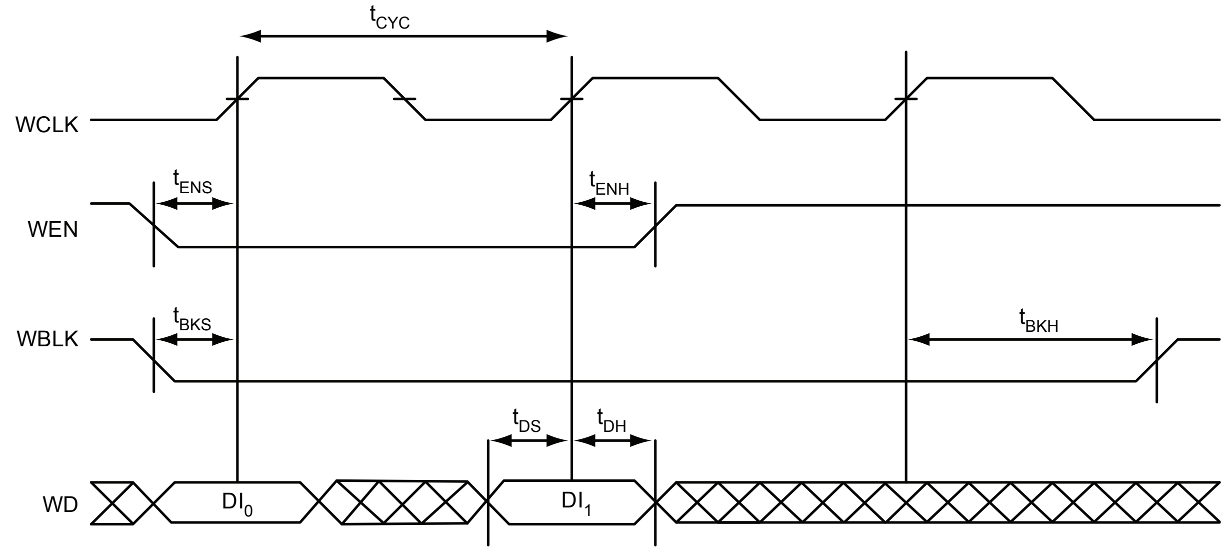

Figure 2-48 • **FIFO Write**

3 – Pin Descriptions and Packaging

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

VCCIBx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. In general, unused I/O banks should have their corresponding VCCIX pins tied to GND. If an output pad is terminated to ground through any resistor and if the corresponding VCCIX is left floating, then the leakage current to ground is ~ 0uA. However, if an output pad is terminated to ground through any resistor and the corresponding VCCIX grounded, then the leakage current to ground is ~ 3 uA. For unused banks the aforementioned behavior is to be taken into account while deciding if it's better to float VCCIX of unused bank or tie it to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V.

When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *ProASIC3E FPGA Fabric User's Guide* for a complete board solution for the PLL analog power supply and ground.

There are six VCCPLX pins on ProASIC3E devices.

VCOMPLA/B/C/D/E/F **PLL Ground**

Ground to analog PLL power supplies. When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There are six VCOMPL pins (PLL ground) on ProASIC3E devices.

FG324	
Pin Number	**A3PE3000 FBGA**
N1	IO247NDB6V1
N2	IO247PDB6V1
N3	IO251NPB6V2
N4	GEC0/IO236NDB6V0
N5	VCOMPLE
N6	IO212NDB5V2
N7	IO212PDB5V2
N8	IO192NPB4V4
N9	IO174PDB4V2
N10	IO170PDB4V2
N11	GDA2/IO154PPB4V0
N12	GDB2/IO155PPB4V0
N13	GDA1/IO153PPB3V4
N14	VCOMPLD
N15	GDB0/IO152NDB3V4
N16	GDB1/IO152PDB3V4
N17	IO138NDB3V3
N18	IO138PDB3V3
P1	IO245PDB6V1
P2	GNDQ
P3	VMV6
P4	GEC1/IO236PDB6V0
P5	VCCPLE
P6	IO214PDB5V2
P7	VCCIB5
P8	GND
P9	IO174NDB4V2
P10	IO170NDB4V2
P11	GND
P12	VCCIB4
P13	IO155NPB4V0
P14	VCCPLD
P15	VJTAG
P16	GDC0/IO151NDB3V4
P17	GDC1/IO151PDB3V4
P18	IO142PDB3V3

FG324	
Pin Number	**A3PE3000 FBGA**
R1	IO245NDB6V1
R2	VCCIB6
R3	GEA1/IO234PPB6V0
R4	IO232NDB5V4
R5	GEB2/IO232PDB5V4
R6	IO214NDB5V2
R7	IO202PDB5V1
R8	IO194PDB5V0
R9	IO186PDB4V4
R10	IO178PDB4V3
R11	IO168NSB4V1
R12	IO164PDB4V1
R13	GDC2/IO156PDB4V0
R14	TCK
R15	VPUMP
R16	TRST
R17	VCCIB3
R18	IO142NDB3V3
T1	IO241PDB6V0
T2	GEA0/IO234NPB6V0
T3	IO233NPB5V4
T4	IO231NPB5V4
T5	VMV5
T6	IO208NDB5V1
T7	IO202NDB5V1
T8	IO194NDB5V0
T9	IO186NDB4V4
T10	IO178NDB4V3
T11	IO166NPB4V1
T12	IO164NDB4V1
T13	IO156NDB4V0
T14	VMV4
T15	TDI
T16	GNDQ
T17	TDO
T18	IO146PDB3V4

FG324	
Pin Number	**A3PE3000 FBGA**
U1	IO241NDB6V0
U2	GEA2/IO233PPB5V4
U3	GEC2/IO231PPB5V4
U4	VCCIB5
U5	GNDQ
U6	IO208PDB5V1
U7	IO198PPB5V0
U8	VCCIB5
U9	IO182NPB4V3
U10	IO180NPB4V3
U11	VCCIB4
U12	IO166PPB4V1
U13	IO162PDB4V1
U14	GNDQ
U15	VCCIB4
U16	TMS
U17	VMV3
U18	IO146NDB3V4
V1	GND
V2	IO218NDB5V3
V3	IO218PDB5V3
V4	IO206NDB5V1
V5	IO206PDB5V1
V6	IO198NPB5V0
V7	GND
V8	IO190NDB4V4
V9	IO190PDB4V4
V10	IO182PPB4V3
V11	IO180PPB4V3
V12	GND
V13	IO162NDB4V1
V14	IO160NDB4V0
V15	IO160PDB4V0
V16	IO158NDB4V0
V17	IO158PDB4V0
V18	GND

FG484	
Pin Number	**A3PE600 Function**
N17	IO57NPB3V0
N18	IO55NPB3V0
N19	IO57PPB3V0
N20	NC
N21	IO56NDB3V0
N22	IO58PDB3V0
P1	NC
P2	IO111PDB6V1
P3	IO115NPB6V1
P4	IO113NPB6V1
P5	IO109PPB6V0
P6	IO108PDB6V0
P7	IO108NDB6V0
P8	VCCIB6
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB3
P16	GDB0/IO66NPB3V1
P17	IO60NDB3V1
P18	IO60PDB3V1
P19	IO61PDB3V1
P20	NC
P21	IO59PDB3V0
P22	IO58NDB3V0
R1	NC
R2	IO110PDB6V0
R3	VCC
R4	IO109NPB6V0
R5	IO106NDB6V0
R6	IO106PDB6V0
R7	GEC0/IO104NPB6V0
R8	VMV5

FG484	
Pin Number	**A3PE600 Function**
R9	VCCIB5
R10	VCCIB5
R11	IO84NDB5V0
R12	IO84PDB5V0
R13	VCCIB4
R14	VCCIB4
R15	VMV3
R16	VCCPLD
R17	GDB1/IO66PPB3V1
R18	GDC1/IO65PDB3V1
R19	IO61NDB3V1
R20	VCC
R21	IO59NDB3V0
R22	IO62PDB3V1
T1	NC
T2	IO110NDB6V0
T3	NC
T4	IO105PDB6V0
T5	IO105NDB6V0
T6	GEC1/IO104PPB6V0
T7	VCOMPLE
T8	GNDQ
T9	GEA2/IO101PPB5V2
T10	IO92NDB5V1
T11	IO90NDB5V1
T12	IO82NDB5V0
T13	IO74NDB4V1
T14	IO74PDB4V1
T15	GNDQ
T16	VCOMPLD
T17	VJTAG
T18	GDC0/IO65NDB3V1
T19	GDA1/IO67PDB3V1
T20	NC
T21	IO64PDB3V1
T22	IO62NDB3V1

FG484	
Pin Number	**A3PE600 Function**
U1	NC
U2	IO107PDB6V0
U3	IO107NDB6V0
U4	GEB1/IO103PDB6V0
U5	GEB0/IO103NDB6V0
U6	VMV6
U7	VCCPLE
U8	IO101NPB5V2
U9	IO95PPB5V1
U10	IO92PDB5V1
U11	IO90PDB5V1
U12	IO82PDB5V0
U13	IO76NDB4V1
U14	IO76PDB4V1
U15	VMV4
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO67NDB3V1
U20	NC
U21	IO64NDB3V1
U22	IO63PDB3V1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO102PDB6V0
V5	GEA0/IO102NDB6V0
V6	GNDQ
V7	GEC2/IO99PDB5V2
V8	IO95NPB5V1
V9	IO91NDB5V1
V10	IO91PDB5V1
V11	IO83NDB5V0
V12	IO83PDB5V0
V13	IO77NDB4V1
V14	IO77PDB4V1

FG896	
Pin Number	**A3PE3000 Function**
M23	IO104PPB2V2
M24	IO102PDB2V2
M25	IO102NDB2V2
M26	IO95PDB2V1
M27	IO97NDB2V1
M28	IO101NDB2V2
M29	IO103NDB2V2
M30	IO119PDB3V0
N1	IO276PDB7V0
N2	IO278PDB7V0
N3	IO280PDB7V0
N4	IO284PDB7V1
N5	IO279PDB7V0
N6	IO285NDB7V1
N7	IO287NDB7V1
N8	IO281NDB7V0
N9	IO281PDB7V0
N10	VCCIB7
N11	VCC
N12	GND
N13	GND
N14	GND
N15	GND
N16	GND
N17	GND
N18	GND
N19	GND
N20	VCC
N21	VCCIB2
N22	IO106NDB2V3
N23	IO106PDB2V3
N24	IO108PDB2V3
N25	IO108NDB2V3
N26	IO95NDB2V1
N27	IO99NDB2V2
N28	IO99PDB2V2
N29	IO107PDB2V3
N30	IO107NDB2V3
P1	IO276NDB7V0
P2	IO278NDB7V0
P3	IO280NDB7V0
P4	IO284NDB7V1
P5	IO279NDB7V0
P6	GFC1/IO275PDB7V0
P7	GFC0/IO275NDB7V0
P8	IO277PDB7V0
P9	IO277NDB7V0
P10	VCCIB7
P11	VCC
P12	GND
P13	GND
P14	GND
P15	GND
P16	GND
P17	GND
P18	GND
P19	GND
P20	VCC
P21	VCCIB2
P22	GCC1/IO112PDB2V3
P23	IO110PDB2V3
P24	IO110NDB2V3
P25	IO109PPB2V3
P26	IO111NPB2V3
P27	IO105PDB2V2
P28	IO105NDB2V2
P29	GCC2/IO117PDB3V0
P30	IO117NDB3V0
R1	GFC2/IO270PDB6V4
R2	GFB1/IO274PPB7V0
R3	VCOMPLF
R4	GFA0/IO273NDB6V4
R5	GFB0/IO274NPB7V0
R6	IO271NDB6V4
R7	GFB2/IO271PDB6V4
R8	IO269PDB6V4
R9	IO269NDB6V4
R10	VCCIB7
R11	VCC
R12	GND
R13	GND
R14	GND
R15	GND
R16	GND
R17	GND
R18	GND
R19	GND
R20	VCC
R21	VCCIB2
R22	GCC0/IO112NDB2V3
R23	GCB2/IO116PDB3V0
R24	IO118PDB3V0
R25	IO111PPB2V3
R26	IO122PPB3V1
R27	GCA0/IO114NPB3V0
R28	VCOMPLC
R29	GCB1/IO113PPB2V3
R30	IO115NPB3V0
T1	IO270NDB6V4
T2	VCCPLF
T3	GFA2/IO272PPB6V4
T4	GFA1/IO273PDB6V4
T5	IO272NPB6V4
T6	IO267NDB6V4
T7	IO267PDB6V4
T8	IO265PDB6V3
T9	IO263PDB6V3
T10	VCCIB6

Revision	Changes	Page
v2.0 (continued)	Table 3-6 • Temperature and Voltage Derating Factors for Timing Delays was updated.	3-5
	Table 3-5 • Package Thermal Resistivities was updated.	3-5
	Table 3-10 • Different Components Contributing to the Dynamic Power Consumption in ProASIC3E Devices was updated.	3-8
	t_{WRO} and t_{CCKH} were added to Table 3-94 • RAM4K9 and Table 3-95 • RAM512X18.	3-74 to 3-74
	The note in Table 3-24 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was updated.	3-23
	Figure 3-43 • Write Access After Write onto Same Address, Figure 3-44 • Read Access After Write onto Same Address, and Figure 3-45 • Write Access After Read onto Same Address are new.	3-71 to 3-73
	Figure 3-53 • Timing Diagram was updated.	3-80
	Notes were added to the package diagrams identifying if they were top or bottom view.	N/A
	The A3PE1500 "208-Pin PQFP" table is new.	4-4
	The A3PE1500 "484-Pin FBGA" table is new.	4-18
	The A3PE1500 "A3PE1500 Function" table is new.	4-24
Advance v0.6 (January 2007)	In the "Packaging Tables" table, the number of I/Os for the A3PE1500 was changed for the FG484 and FG676 packages.	ii
Advance v0.5 (April 2006)	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	Figure 2-8 • Very-Long-Line Resources was updated.	2-8
	The footnotes in Figure 2-27 • CCC/PLL Macro were updated.	2-28
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options.	2-24
	The "SRAM and FIFO" section was updated.	2-21
	The "RESET" section was updated.	2-25
	The "WCLK and RCLK" section was updated.	2-25
	The "RESET" section was updated.	2-25
	The "RESET" section was updated.	2-27
	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	Figure 2-8 • Very-Long-Line Resources was updated.	2-8
	The footnotes in Figure 2-27 • CCC/PLL Macro were updated.	2-28
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options.	2-24
	The "SRAM and FIFO" section was updated.	2-21
	The "RESET" section was updated.	2-25
	The "WCLK and RCLK" section was updated.	2-25