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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	516096
Number of I/O	221
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	324-BGA
Supplier Device Package	324-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3pe3000-2fgg324

VersaTiles

The ProASIC3E core consists of VersaTiles, which have been enhanced beyond the ProASIC^PLUS® core tiles. The ProASIC3E VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-2 for VersaTile configurations.

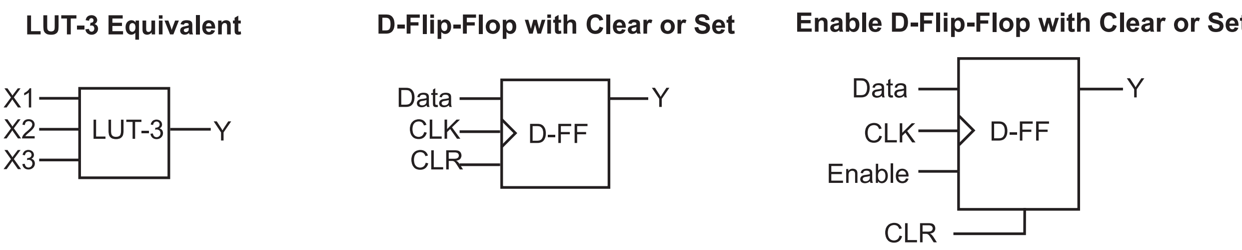


Figure 1-2 • **VersaTile Configurations**

User Nonvolatile FlashROM

ProASIC3E devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3E IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC3E development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-11 on page 2-11.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-12 on page 2-11.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-12 on page 2-11. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

$P_{STAT} = PDC1 + N_{INPUTS} * PDC2 + N_{OUTPUTS} * PDC3$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

Global Clock Contribution—P_{CLOCK}

$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S\text{-}CELL} * PAC4) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3E FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3E FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-11 on page 2-11.

F_{CLK} is the global clock signal frequency.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

***Table 2-33* • Minimum and Maximum DC Input and Output Levels**

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max., V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	μA[4]	μA[4]
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

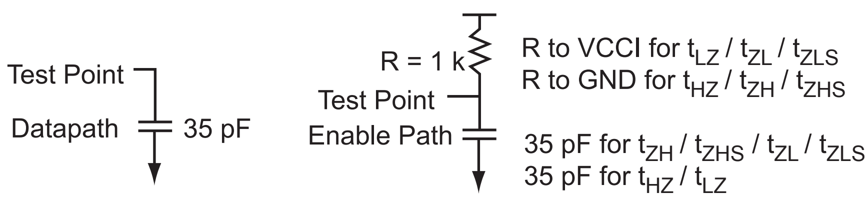


***Figure 2-8* • AC Loading**

***Table 2-34* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

***Table 2-41* • Minimum and Maximum DC Input and Output Levels**

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[3]**	**Max. mA[3]**	**μA[4]**	**μA[4]**
2 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10
6 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	6	6	39	32	10	10
8 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	8	8	55	66	10	10
12 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12	55	66	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V< VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

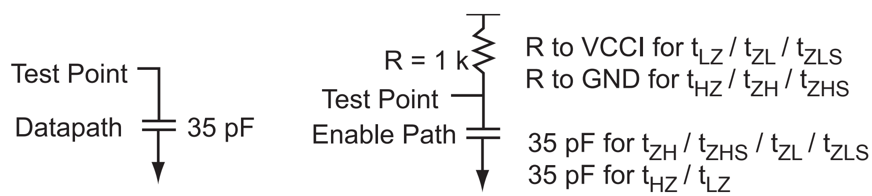


***Figure 2-10* • AC Loading**

***Table 2-42* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	1.5	0.75	–	35

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Voltage-Referenced I/O Characteristics

3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-48 **• Minimum and Maximum DC Input and Output Levels**

3.3 V GTL	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
20 mA[3]	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20	181	268	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

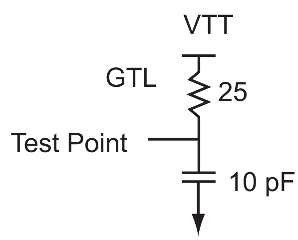


Figure 2-12 **• AC Loading**

Table 2-49 **• AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.05	VREF + 0.05	0.8	0.8	1.2	10

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-50 **• 3.3 V GTL**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V VREF = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.60	2.08	0.04	2.93	0.43	2.04	2.08			4.27	4.31	ns
–1	0.51	1.77	0.04	2.50	0.36	1.73	1.77			3.63	3.67	ns
–2	0.45	1.55	0.03	2.19	0.32	1.52	1.55			3.19	3.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

***Table 2-54* • Minimum and Maximum DC Input and Output Levels**

3.3 V GTL+	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	μA[2]	μA[2]
35 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35	181	268	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

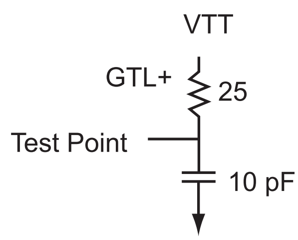


***Figure 2-14* • AC Loading**

***Table 2-55* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

***Table 2-56* • 3.3 V GTL+**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.60	2.06	0.04	1.59	0.43	2.09	2.06			4.33	4.29	ns
–1	0.51	1.75	0.04	1.35	0.36	1.78	1.75			3.68	3.65	ns
–2	0.45	1.53	0.03	1.19	0.32	1.56	1.53			3.23	3.20	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-60 **• Minimum and Maximum DC Input and Output Levels**

HSTL Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	μA[2]	μA[2]
8 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8	39	32	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

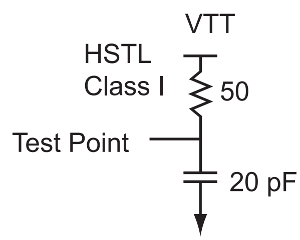


Figure 2-16 **• AC Loading**

Table 2-61 **• AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: **Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-62 **• HSTL Class I**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = .4 V, VREF = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	3.18	0.04	2.12	0.43	3.24	3.14			5.47	5.38	ns
–1	0.56	2.70	0.04	1.81	0.36	2.75	2.67			4.66	4.58	ns
–2	0.49	2.37	0.03	1.59	0.32	2.42	2.35			4.09	4.02	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

***Table 2-63* • Minimum and Maximum DC Input and Output Levels**

HSTL Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max., V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
15 mA[3]	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15	55	66	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

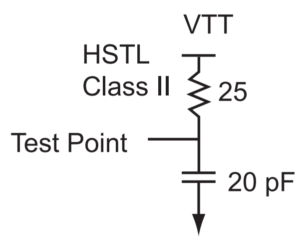


***Figure 2-17* • AC Loading**

***Table 2-64* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: **Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

***Table 2-65* • HSTL Class II**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V, VREF = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	3.02	0.04	2.12	0.43	3.08	2.71			5.32	4.95	ns
–1	0.56	2.57	0.04	1.81	0.36	2.62	2.31			4.52	4.21	ns
–2	0.49	2.26	0.03	1.59	0.32	2.30	2.03			3.97	3.70	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-66 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	μA[2]	μA[2]
15 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15	87	83	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

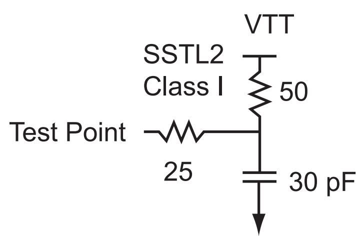


Figure 2-18 • AC Loading

Table 2-67 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-68 • SSTL 2 Class I
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.13	0.04	1.33	0.43	2.17	1.85			4.40	4.08	ns
–1	0.56	1.81	0.04	1.14	0.36	1.84	1.57			3.74	3.47	ns
–2	0.49	1.59	0.03	1.00	0.32	1.62	1.38			3.29	3.05	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

DDR Module Specifications

Input DDR Module

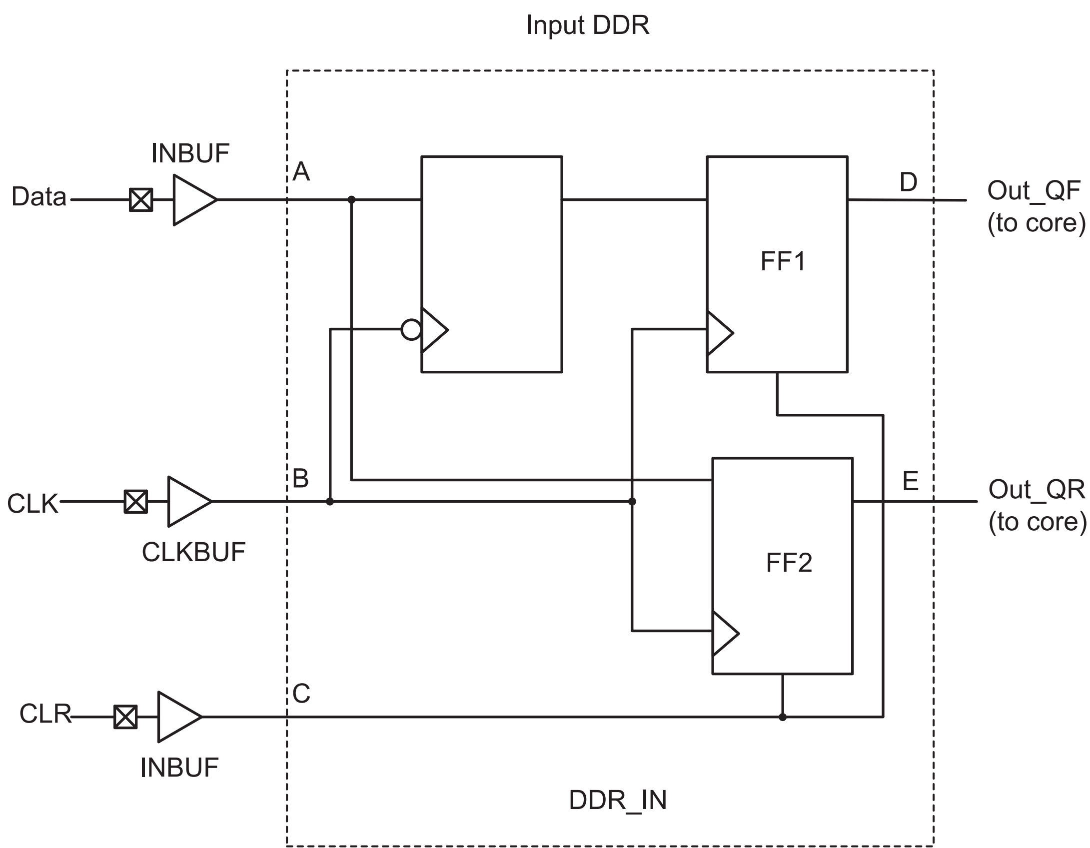


***Figure 2-30* • Input DDR Timing Model**

***Table 2-89* • Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-98 • ProASIC3E CCC/PLL Specification

Parameter		Minimum	Typical	Maximum	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}		1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}		0.75		350	MHz
Delay Increments in Programmable Delay Blocks [1, 2]			160[3]		ps
Serial Clock (SCLK) for Dynamic PLL[4]				125	MHz
Number of Programmable Values in Each Programmable Delay Block				32	
Input Period Jitter				1.5	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}		Max Peak-to-Peak Period Jitter			
		1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz		0.50%		0.70%	
24 MHz to 100 MHz		1.00%		1.20%	
100 MHz to 250 MHz		1.75%		2.00%	
250 MHz to 350 MHz		2.50%		5.60%	
Acquisition Time	LockControl = 0			300	µs
	LockControl = 1			6.0	ms
Tracking Jitter [5]	LockControl = 0			1.6	ns
	LockControl = 1			0.8	ns
Output Duty Cycle		48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]		0.6		5.56	ns
Delay Range in Block: Programmable Delay 2 [1,2]		0.025		5.56	ns
Delay Range in Block: Fixed Delay[1,4]			2.2		ns

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-5 for deratings*
2. *T_J = 25°C, VCC = 1.5 V.*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help for more information.*
4. *Maximum value obtained for a –2 speed-grade device in worst-case commercial conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*
5. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*

Timing Characteristics

Table 2-101 • FIFO
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.38	1.57	1.84	ns
t_{ENH}	REN, WEN Hold Time	0.02	0.02	0.02	ns
t_{BKS}	BLK Setup Time	0.19	0.22	0.26	ns
t_{BKH}	BLK Hold Time	0.00	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (pass-through)	2.36	2.68	3.15	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.89	1.02	1.20	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (pass-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on RD (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET Recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency	310	272	231	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

FG256	
Pin Number	A3PE600 Function
G13	GCC1/IO50PPB2V1
G14	IO44NDB2V1
G15	IO44PDB2V1
G16	IO49NSB2V1
H1	GFB0/IO119NPB7V0
H2	GFA0/IO118NDB6V1
H3	GFB1/IO119PPB7V0
H4	VCOMPLF
H5	GFC0/IO120NPB7V0
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO50NPB2V1
H13	GCB1/IO51PPB2V1
H14	GCA0/IO52NPB3V0
H15	VCOMPLC
H16	GCB0/IO51NPB2V1
J1	GFA2/IO117PSB6V1
J2	GFA1/IO118PDB6V1
J3	VCCPLF
J4	IO116NDB6V1
J5	GFB2/IO116PDB6V1
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO54PPB3V0
J13	GCA1/IO52PPB3V0
J14	GCC2/IO55PPB3V0
J15	VCCPLC
J16	GCA2/IO53PSB3V0

FG256	
Pin Number	A3PE600 Function
K1	GFC2/IO115PSB6V1
K2	IO113PPB6V1
K3	IO112PDB6V1
K4	IO112NDB6V1
K5	VCCIB6
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB3
K13	IO54NPB3V0
K14	IO57NPB3V0
K15	IO55NPB3V0
K16	IO57PPB3V0
L1	IO113NPB6V1
L2	IO109PPB6V0
L3	IO108PDB6V0
L4	IO108NDB6V0
L5	VCCIB6
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB3
L13	GDB0/IO66NPB3V1
L14	IO60NDB3V1
L15	IO60PDB3V1
L16	IO61PDB3V1
M1	IO109NPB6V0
M2	IO106NDB6V0
M3	IO106PDB6V0
M4	GEC0/IO104NPB6V0

FG256	
Pin Number	A3PE600 Function
M5	VMV5
M6	VCCIB5
M7	VCCIB5
M8	IO84NDB5V0
M9	IO84PDB5V0
M10	VCCIB4
M11	VCCIB4
M12	VMV3
M13	VCCPLD
M14	GDB1/IO66PPB3V1
M15	GDC1/IO65PDB3V1
M16	IO61NDB3V1
N1	IO105PDB6V0
N2	IO105NDB6V0
N3	GEC1/IO104PPB6V0
N4	VCOMPLE
N5	GNDQ
N6	GEA2/IO101PPB5V2
N7	IO92NDB5V1
N8	IO90NDB5V1
N9	IO82NDB5V0
N10	IO74NDB4V1
N11	IO74PDB4V1
N12	GNDQ
N13	VCOMPLD
N14	VJTAG
N15	GDC0/IO65NDB3V1
N16	GDA1/IO67PDB3V1
P1	GEB1/IO103PDB6V0
P2	GEB0/IO103NDB6V0
P3	VMV6
P4	VCCPLE
P5	IO101NPB5V2
P6	IO95PPB5V1
P7	IO92PDB5V1
P8	IO90PDB5V1

FG484	
Pin Number	A3PE600 Function
N17	IO57NPB3V0
N18	IO55NPB3V0
N19	IO57PPB3V0
N20	NC
N21	IO56NDB3V0
N22	IO58PDB3V0
P1	NC
P2	IO111PDB6V1
P3	IO115NPB6V1
P4	IO113NPB6V1
P5	IO109PPB6V0
P6	IO108PDB6V0
P7	IO108NDB6V0
P8	VCCIB6
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB3
P16	GDB0/IO66NPB3V1
P17	IO60NDB3V1
P18	IO60PDB3V1
P19	IO61PDB3V1
P20	NC
P21	IO59PDB3V0
P22	IO58NDB3V0
R1	NC
R2	IO110PDB6V0
R3	VCC
R4	IO109NPB6V0
R5	IO106NDB6V0
R6	IO106PDB6V0
R7	GEC0/IO104NPB6V0
R8	VMV5

FG484	
Pin Number	A3PE600 Function
R9	VCCIB5
R10	VCCIB5
R11	IO84NDB5V0
R12	IO84PDB5V0
R13	VCCIB4
R14	VCCIB4
R15	VMV3
R16	VCCPLD
R17	GDB1/IO66PPB3V1
R18	GDC1/IO65PDB3V1
R19	IO61NDB3V1
R20	VCC
R21	IO59NDB3V0
R22	IO62PDB3V1
T1	NC
T2	IO110NDB6V0
T3	NC
T4	IO105PDB6V0
T5	IO105NDB6V0
T6	GEC1/IO104PPB6V0
T7	VCOMPLE
T8	GNDQ
T9	GEA2/IO101PPB5V2
T10	IO92NDB5V1
T11	IO90NDB5V1
T12	IO82NDB5V0
T13	IO74NDB4V1
T14	IO74PDB4V1
T15	GNDQ
T16	VCOMPLD
T17	VJTAG
T18	GDC0/IO65NDB3V1
T19	GDA1/IO67PDB3V1
T20	NC
T21	IO64PDB3V1
T22	IO62NDB3V1

FG484	
Pin Number	A3PE600 Function
U1	NC
U2	IO107PDB6V0
U3	IO107NDB6V0
U4	GEB1/IO103PDB6V0
U5	GEB0/IO103NDB6V0
U6	VMV6
U7	VCCPLE
U8	IO101NPB5V2
U9	IO95PPB5V1
U10	IO92PDB5V1
U11	IO90PDB5V1
U12	IO82PDB5V0
U13	IO76NDB4V1
U14	IO76PDB4V1
U15	VMV4
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO67NDB3V1
U20	NC
U21	IO64NDB3V1
U22	IO63PDB3V1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO102PDB6V0
V5	GEA0/IO102NDB6V0
V6	GNDQ
V7	GEC2/IO99PDB5V2
V8	IO95NPB5V1
V9	IO91NDB5V1
V10	IO91PDB5V1
V11	IO83NDB5V0
V12	IO83PDB5V0
V13	IO77NDB4V1
V14	IO77PDB4V1

FG484	
Pin Number	**A3PE600 Function**
V15	IO69NDB4V0
V16	GDB2/IO69PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO63NDB3V1
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO100NDB5V2
W6	GEB2/IO100PDB5V2
W7	IO99NDB5V2
W8	IO88NDB5V0
W9	IO88PDB5V0
W10	IO89NDB5V0
W11	IO80NDB4V1
W12	IO81NDB4V1
W13	IO81PDB4V1
W14	IO70NDB4V0
W15	GDC2/IO70PDB4V0
W16	IO68NDB4V0
W17	GDA2/IO68PDB4V0
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB6
Y2	NC
Y3	NC
Y4	IO98NDB5V2
Y5	GND
Y6	IO94NDB5V1

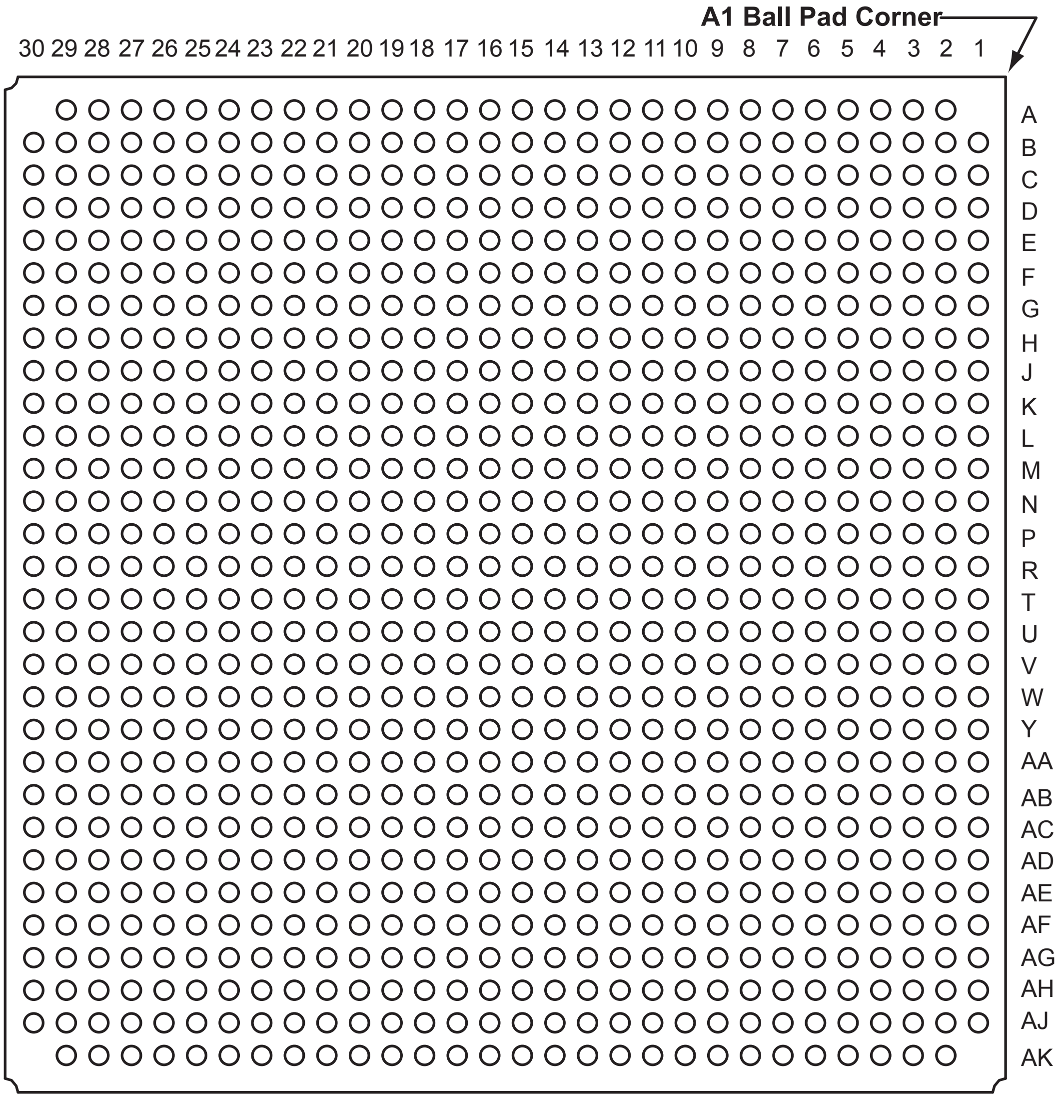
FG484	
Pin Number	**A3PE600 Function**
Y7	IO94PDB5V1
Y8	VCC
Y9	VCC
Y10	IO89PDB5V0
Y11	IO80PDB4V1
Y12	IO78NPB4V1
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB3

FG676	
Pin Number	A3PE1500 Function
R21	IO89NDB3V0
R22	GCB2/IO89PDB3V0
R23	IO90NDB3V0
R24	GCC2/IO90PDB3V0
R25	IO91PDB3V0
R26	IO91NDB3V0
T1	IO186PDB6V2
T2	IO185NDB6V2
T3	GNDQ
T4	IO180PDB6V1
T5	IO180NDB6V1
T6	IO188NDB6V2
T7	GFB2/IO188PDB6V2
T8	VCCIB6
T9	VCC
T10	GND
T11	GND
T12	GND
T13	GND
T14	GND
T15	GND
T16	GND
T17	GND
T18	VCC
T19	VCCIB3
T20	IO99PDB3V1
T21	IO99NDB3V1
T22	IO97PDB3V1
T23	IO97NDB3V1
T24	GNDQ
T25	IO93PPB3V0
T26	NC
U1	IO186NDB6V2
U2	IO184NDB6V2
U3	IO184PDB6V2
U4	IO182NDB6V1

FG676	
Pin Number	A3PE1500 Function
U5	IO182PDB6V1
U6	IO178PDB6V1
U7	IO178NDB6V1
U8	VCCIB6
U9	VCC
U10	GND
U11	GND
U12	GND
U13	GND
U14	GND
U15	GND
U16	GND
U17	GND
U18	VCC
U19	VCCIB3
U20	NC
U21	IO101NDB3V1
U22	IO101PDB3V1
U23	IO92NDB3V0
U24	IO92PDB3V0
U25	IO95PDB3V1
U26	IO93NPB3V0
V1	IO183PDB6V2
V2	IO183NDB6V2
V3	VMV6
V4	IO181PDB6V1
V5	IO181NDB6V1
V6	IO176PDB6V1
V7	IO176NDB6V1
V8	VCCIB6
V9	VCC
V10	VCC
V11	VCC
V12	VCC
V13	VCC
V14	VCC

FG676	
Pin Number	A3PE1500 Function
V15	VCC
V16	VCC
V17	VCC
V18	VCC
V19	VCCIB3
V20	IO107PDB3V2
V21	IO107NDB3V2
V22	IO103NDB3V2
V23	IO103PDB3V2
V24	VMV3
V25	IO95NDB3V1
V26	IO94PDB3V0
W1	IO179NDB6V1
W2	IO179PDB6V1
W3	IO177NDB6V1
W4	IO177PDB6V1
W5	IO172PDB6V0
W6	IO172NDB6V0
W7	VCC
W8	VCC
W9	VCCIB5
W10	VCCIB5
W11	VCCIB5
W12	VCCIB5
W13	VCCIB5
W14	VCCIB4
W15	VCCIB4
W16	VCCIB4
W17	VCCIB4
W18	VCCIB4
W19	VCC
W20	VCCIB3
W21	GDB0/IO109NDB3V2
W22	GDB1/IO109PDB3V2
W23	IO105NDB3V2
W24	IO105PDB3V2

FG896



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/products/fpga-soc/solutions*.

Revision	Changes	Page
Revision 10 (March 2012)	The "In-System Programming (ISP) and Security" section and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34669).	I, 1-1
	The Y security option and Licensed DPA Logo were added to the "ProASIC3E Ordering Information" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 34727).	III
	The following sentence was removed from the "Advanced Architecture" section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOOe devices via an IEEE 1532 JTAG interface" (SAR 34689).	1-3
	The "Specifying I/O States During Programming" section is new (SAR 34699).	1-6
	VCCPLL in Table 2-2 • Recommended Operating Conditions [1] was corrected from "1.4 to 1.6 V" to "1.425 to 1.575 V" (SAR 33851). The T_J symbol was added to the table and notes regarding T_A and T_J were removed. The second of two parameters in the VCCI and VMV row, called "3.3 V DC supply voltage," was corrected to "3.0 V DC supply voltage" (SAR 37227).	2-2
	The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Contribution—P_{CLOCK}" section, was corrected to the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3E FPGA Fabric User's Guide* (SAR 34735).	2-9
	t_{DOUT} was corrected to t_{DIN} in Figure 2-3 • Input Buffer Timing Model and Delays (example) (SAR 37109).	2-13
	The typo related to the values for 3.3 V LVCMOS Wide Range in Table 2-17 • Summary of I/O Timing Characteristics—Software Default Settings was corrected (SAR 37227).	2-19
	The notes regarding drive strength in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section and "3.3 V LVCMOS Wide Range" section and tables were revised for clarification. They now state that the minimum drive strength for the default software configuration when run in wide range is ±100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 34763).	2-18, 2-27

Revision	Changes	Page
v2.0 (continued)	Table 3-6 • Temperature and Voltage Derating Factors for Timing Delays was updated.	3-5
	Table 3-5 • Package Thermal Resistivities was updated.	3-5
	Table 3-10 • Different Components Contributing to the Dynamic Power Consumption in ProASIC3E Devices was updated.	3-8
	t_{WRO} and t_{CCKH} were added to Table 3-94 • RAM4K9 and Table 3-95 • RAM512X18.	3-74 to 3-74
	The note in Table 3-24 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was updated.	3-23
	Figure 3-43 • Write Access After Write onto Same Address, Figure 3-44 • Read Access After Write onto Same Address, and Figure 3-45 • Write Access After Read onto Same Address are new.	3-71 to 3-73
	Figure 3-53 • Timing Diagram was updated.	3-80
	Notes were added to the package diagrams identifying if they were top or bottom view.	N/A
	The A3PE1500 "208-Pin PQFP" table is new.	4-4
	The A3PE1500 "484-Pin FBGA" table is new.	4-18
	The A3PE1500 "A3PE1500 Function" table is new.	4-24
Advance v0.6 (January 2007)	In the "Packaging Tables" table, the number of I/Os for the A3PE1500 was changed for the FG484 and FG676 packages.	ii
Advance v0.5 (April 2006)	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	Figure 2-8 • Very-Long-Line Resources was updated.	2-8
	The footnotes in Figure 2-27 • CCC/PLL Macro were updated.	2-28
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options.	2-24
	The "SRAM and FIFO" section was updated.	2-21
	The "RESET" section was updated.	2-25
	The "WCLK and RCLK" section was updated.	2-25
	The "RESET" section was updated.	2-25
	The "RESET" section was updated.	2-27
	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	Figure 2-8 • Very-Long-Line Resources was updated.	2-8
	The footnotes in Figure 2-27 • CCC/PLL Macro were updated.	2-28
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options.	2-24
	The "SRAM and FIFO" section was updated.	2-21
	The "RESET" section was updated.	2-25
	The "WCLK and RCLK" section was updated.	2-25

Revision	Changes	Page
Advance v0.3 (continued)	The "Methodology" section was updated.	3-9
	The A3PE3000 "208-Pin PQFP" pin table was updated.	4-6