E·XFL



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	516096
Number of I/O	147
Number of Gates	300000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3pe3000-2pqg208i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



1 – ProASIC3E Device Family Overview

General Description

ProASIC3E, the third-generation family of Microsemi flash FPGAs, offers performance, density, and features beyond those of the ProASIC^{PLUS®} family. Nonvolatile flash technology gives ProASIC3E devices the advantage of being a secure, low power, single-chip solution that is Instant On. ProASIC3E is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

ProASIC3E devices offer 1 kbit of on-chip, programmable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on six integrated phase-locked loops (PLLs). ProASIC3E devices have up to three million system gates, supported with up to 504 kbits of true dual-port SRAM and up to 620 user I/Os.

Several ProASIC3E devices support the Cortex-M1 soft IP cores, and the ARM-Enabled devices have Microsemi ordering numbers that begin with M1A3PE.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAMbased FPGAs, flash-based ProASIC3E devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property (IP) cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The ProASIC3E family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the ProASIC3E family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/ communications, computing, and avionics markets.

Security

The nonvolatile, flash-based ProASIC3E devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. ProASIC3E devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

ProASIC3E devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of protection in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in ProASIC3E devices can be encrypted prior to loading, using the industryleading AES-128 (FIPS192) bit block cipher encryption standard. The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. ProASIC3E devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. ProASIC3E devices with AES-based security provide a high level of protection for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of the ProASIC3E family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The ProASIC3E family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. A ProASIC3E device provides the best available security for programmable logic designs.



ProASIC3E Device Family Overview

VersaTiles

The ProASIC3E core consists of VersaTiles, which have been enhanced beyond the ProASIC^{PLUS®} core tiles. The ProASIC3E VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-2 for VersaTile configurations.



User Nonvolatile FlashROM

ProASIC3E devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- · Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- · Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3E IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC3E development software solutions, Libero[®] System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

ProASIC3E DC and Switching Characteristics

Table 2-9 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings (continued) (continued)¹

	C _{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW) ²	Dynamic Power PAC10 (µW/MHz) ³
SSTL3 (I)	30	3.3	26.02	114.87
SSTL3 (II)	30	3.3	42.21	131.76
Differential				
LVDS/B-LVDS/M-LVDS	-	2.5	7.70	89.62
LVPECL	-	3.3	19.42	168.02
Notes:	· · ·		•	

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.

2. PDC3 is the static power (where applicable) measured on VCCI.

3. PAC10 is the total dynamic power measured on VCC and VCCI.

4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

Power Consumption of Various Internal Resources

Table 2-10 • Different Components Contributing to the Dynamic Power Consumption in ProASIC3E Devices

		Device-Specific Dynamic Contributions (μW/MHz)								
Parameter	Definition	A3PE600	A3PE1500	A3PE3000						
PAC1	Clock contribution of a Global Rib	12.77	16.21	19.7						
PAC2	Clock contribution of a Global Spine	1.85	3.06	4.16						
PAC3	Clock contribution of a VersaTile row	0.88								
PAC4	Clock contribution of a VersaTile used as a sequential module		0.12							
PAC5	First contribution of a VersaTile used as a sequential module		0.07							
PAC6	Second contribution of a VersaTile used as a sequential module	0.29								
PAC7	Contribution of a VersaTile used as a combinatorial module		0.29							
PAC8	Average contribution of a routing net		0.70							
PAC9	Contribution of an I/O input pin (standard-dependent)	See T	able 2-8 on pag	je 2-6.						
PAC10	Contribution of an I/O output pin (standard-dependent)	See	Table 2-9 on pag	ge 2-7						
PAC11	Average contribution of a RAM block during a read operation		25.00							
PAC12	Average contribution of a RAM block during a write operation		30.00							
PAC13	Static PLL contribution		2.55 mW							
PAC14	Dynamic contribution for PLL	2.60								

Note: For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power calculator or SmartPower in Libero SoC.

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

		Equivalent			VIL	VIH		VOL	VOH	IOL ³	IOH ³
I/O Standard	Drive Strength	Software Default Drive Strength Option ¹	Slew Rate	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	-0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range	100 µA	12 mA	High	-0.3	0.8	2	3.6	0.2	VCCI – 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	-0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	12 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	12 mA	High	-0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI					Per PC	CI Specificatio	n				
3.3 V PCI-X					Per PCI	-X Specificati	on				
3.3 V GTL	20 mA ²	20 mA ²	High	-0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	-	20	20
2.5 V GTL	20 mA ²	20 mA ²	High	-0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	-	20	20
3.3 V GTL+	35 mA	35 mA	High	-0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	-	35	35
2.5 V GTL+	33 mA	33 mA	High	-0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	-	33	33
HSTL (I)	8 mA	8 mA	High	-0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI - 0.4	8	8
HSTL (II)	15 mA ²	15 mA ²	High	-0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI - 0.4	15	15
SSTL2 (I)	15 mA	15 mA	High	-0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15
SSTL2 (II)	18 mA	18 mA	High	-0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18
SSTL3 (I)	14 mA	14 mA	High	-0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14
SSTL3 (II)	21 mA	21 mA	High	-0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI - 0.9	21	21

 Table 2-13 • Summary of Maximum and Minimum DC Input and Output Levels

 Applicable to Commercial and Industrial Conditions

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2. Output drive strength is below JEDEC specification.

3. Currents are measured at 85°C junction temperature.

4. Output Slew Rates can be extracted from IBIS Models, located at http://www.microsemi.com/index.php?option=com_content&id=1671&lang=en&view=article.

Timing Characteristics

Drivo	Speed				Ū									
Strength	Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
2 mA	Std.	0.66	7.88	0.04	1.20	1.57	0.43	8.03	6.70	2.69	2.59	10.26	8.94	ns
	-1	0.56	6.71	0.04	1.02	1.33	0.36	6.83	5.70	2.29	2.20	8.73	7.60	ns
	-2	0.49.	5.89	0.03	0.90	1.17	0.32	6.00	5.01	2.01	1.93	7.67	6.67	ns
4 mA	Std.	0.66	7.88	0.04	1.20	1.57	0.43	8.03	6.70	2.69	2.59	10.26	8.94	ns
	-1	0.56	6.71	0.04	1.02	1.33	0.36	6.83	5.70	2.29	2.20	8.73	7.60	ns
	-2	0.49	5.89	0.03	0.90	1.17	0.32	6.00	5.01	2.01	1.93	7.67	6.67	ns
6 mA	Std.	0.66	5.08	0.04	1.20	1.57	0.43	5.17	4.14	3.05	3.21	7.41	6.38	ns
	-1	0.56	4.32	0.04	1.02	1.33	0.36	4.40	3.52	2.59	2.73	6.30	5.43	ns
	-2	0.49	3.79	0.03	0.90	1.17	0.32	3.86	3.09	2.28	2.40	5.53	4.76	ns
8 mA	Std.	0.66	5.08	0.04	1.20	1.57	0.43	5.17	4.14	3.05	3.21	7.41	6.38	ns
	-1	0.56	4.32	0.04	1.02	1.33	0.36	4.40	3.52	2.59	2.73	6.30	5.43	ns
	-2	0.49	3.79	0.03	0.90	1.17	0.32	3.86	3.09	2.28	2.40	5.53	4.76	ns
12 mA	Std.	0.66	3.67	0.04	1.20	1.57	0.43	3.74	2.87	3.28	3.61	5.97	5.11	ns
	-1	0.56	3.12	0.04	1.02	1.33	0.36	3.18	2.44	2.79	3.07	5.08	4.34	ns
	-2	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81	ns
16 mA	Std.	0.66	3.46	0.04	1.20	1.57	0.43	3.53	2.61	3.33	3.72	5.76	4.84	ns
	-1	0.56	2.95	0.04	1.02	1.33	0.36	3.00	2.22	2.83	3.17	4.90	4.12	ns
	-2	0.49	2.59	0.03	0.90	1.17	0.32	2.63	1.95	2.49	2.78	4.30	3.62	ns
24 mA	Std.	0.66	3.21	0.04	1.20	1.57	0.43	3.27	2.16	3.39	4.13	5.50	4.39	ns
	-1	0.56	2.73	0.04	1.02	1.33	0.36	2.78	1.83	2.88	3.51	4.68	3.74	ns
	-2	0.49	2.39	0.03	0.90	1.17	0.32	2.44	1.61	2.53	3.08	4.11	3.28	ns

Table 2-27 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew

Commercial-Case Conditions: T_{.1} = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Notes:

1. Software default selection highlighted in gray.

Table 2-28 • 3.3 V LVTTL / 3.3 V LVCMOS Low SlewCommercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Drive	Speed													
Strength	Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
2 mA	Std.	0.66	11.01	0.04	1.20	1.57	0.43	11.21	9.05	2.69	2.44	13.45	11.29	ns
	-1	0.56	9.36	0.04	1.02	1.33	0.36	9.54	7.70	2.29	2.08	11.44	9.60	ns
	-2	0.49	8.22	0.03	0.90	1.17	0.32	8.37	6.76	2.01	1.82	10.04	8.43	ns
4 mA	Std.	0.66	11.01	0.04	1.20	1.57	0.43	11.21	9.05	2.69	2.44	13.45	11.29	ns
	-1	0.56	9.36	0.04	1.02	1.33	0.36	9.54	7.70	2.29	2.08	11.44	9.60	ns
	-2	0.49	8.22	0.03	0.90	1.17	0.32	8.37	6.76	2.01	1.82	10.04	8.43	ns
6 mA	Std.	0.66	7.86	0.04	1.20	1.57	0.43	8.01	6.44	3.04	3.06	10.24	8.68	ns
	-1	0.56	6.69	0.04	1.02	1.33	0.36	6.81	5.48	2.58	2.61	8.71	7.38	ns
	-2	0.49	5.87	0.03	0.90	1.17	0.32	5.98	4.81	2.27	2.29	7.65	6.48	ns
8 mA	Std.	0.66	7.86	0.04	1.20	1.57	0.43	8.01	6.44	3.04	3.06	10.24	8.68	ns
	-1	0.56	6.69	0.04	1.02	1.33	0.36	6.81	5.48	2.58	2.61	8.71	7.38	ns
	-2	0.49	5.87	0.03	0.90	1.17	0.32	5.98	4.81	2.27	2.29	7.65	6.48	ns

ProASIC3E DC and Switching Characteristics

Timing Characteristics

Table 2-39 • 1.8 V LVCMOS High Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive	Speed													
Strength	Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
2 mA	Std.	0.66	12.10	0.04	1.45	1.91	0.43	9.59	12.10	2.78	1.64	11.83	14.34	ns
	-1	0.56	10.30	0.04	1.23	1.62	0.36	8.16	10.30	2.37	1.39	10.06	12.20	ns
	-2	0.49	9.04	0.03	1.08	1.42	0.32	7.16	9.04	2.08	1.22	8.83	10.71	ns
4 mA	Std.	0.66	7.05	0.04	1.45	1.91	0.43	6.20	7.05	3.25	2.86	8.44	9.29	ns
	-1	0.56	6.00	0.04	1.23	1.62	0.36	5.28	6.00	2.76	2.44	7.18	7.90	ns
	-2	0.49	5.27	0.03	1.08	1.42	0.32	4.63	5.27	2.43	2.14	6.30	6.94	ns
6 mA	Std.	0.66	4.52	0.04	1.45	1.91	0.43	4.47	4.52	3.57	3.47	6.70	6.76	ns
	-1	0.56	3.85	0.04	1.23	1.62	0.36	3.80	3.85	3.04	2.95	5.70	5.75	ns
	-2	0.49	3.38	0.03	1.08	1.42	0.32	3.33	3.38	2.66	2.59	5.00	5.05	ns
8 mA	Std.	0.66	4.12	0.04	1.45	1.91	0.43	4.20	3.99	3.63	3.62	6.43	6.23	ns
	-1	0.56	3.51	0.04	1.23	1.62	0.36	3.57	3.40	3.09	3.08	5.47	5.30	ns
	-2	0.49	3.08	0.03	1.08	1.42	0.32	3.14	2.98	2.71	2.71	4.81	4.65	ns
12 mA	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	-1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	-2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns
16 mA	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	-1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	-2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns

Notes:

1. Software default selection highlighted in gray.

Drive	Speed													
Strength	Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{zLS}	t _{zHS}	Units
2 mA	Std.	0.66	15.84	0.04	1.45	1.91	0.43	15.65	15.84	2.78	1.58	17.89	18.07	ns
	-1	0.56	13.47	0.04	1.23	1.62	0.36	13.31	13.47	2.37	1.35	15.22	15.37	ns
	-2	0.49	11.83	0.03	1.08	1.42	0.32	11.69	11.83	2.08	1.18	13.36	13.50	ns
4 mA	Std.	0.66	11.39	0.04	1.45	1.91	0.43	11.60	10.76	3.26	2.77	13.84	12.99	ns
	-1	0.56	9.69	0.04	1.23	1.62	0.36	9.87	9.15	2.77	2.36	11.77	11.05	ns
	-2	0.49	8.51	0.03	1.08	1.42	0.32	8.66	8.03	2.43	2.07	10.33	9.70	ns
6 mA	Std.	0.66	8.97	0.04	1.45	1.91	0.43	9.14	8.10	3.57	3.36	11.37	10.33	ns
	-1	0.56	7.63	0.04	1.23	1.62	0.36	7.77	6.89	3.04	2.86	9.67	8.79	ns
	-2	0.49	6.70	0.03	1.08	1.42	0.32	6.82	6.05	2.66	2.51	8.49	7.72	ns
8 mA	Std.	0.66	8.35	0.04	1.45	1.91	0.43	8.50	7.59	3.64	3.52	10.74	9.82	ns
	-1	0.56	7.10	0.04	1.23	1.62	0.36	7.23	6.45	3.10	3.00	9.14	8.35	ns
	-2	0.49	6.24	0.03	1.08	1.42	0.32	6.35	5.66	2.72	2.63	8.02	7.33	ns
12 mA	Std.	0.66	7.94	0.04	1.45	1.91	0.43	8.09	7.56	3.74	4.11	10.32	9.80	ns
	-1	0.56	6.75	0.04	1.23	1.62	0.36	6.88	6.43	3.18	3.49	8.78	8.33	ns
	-2	0.49	5.93	0.03	1.08	1.42	0.32	6.04	5.65	2.79	3.07	7.71	7.32	ns
16 mA	Std.	0.66	7.94	0.04	1.45	1.91	0.43	8.09	7.56	3.74	4.11	10.32	9.80	ns
	-1	0.56	6.75	0.04	1.23	1.62	0.36	6.88	6.43	3.18	3.49	8.78	8.33	ns
	-2	0.49	5.93	0.03	1.08	1.42	0.32	6.04	5.65	2.79	3.07	7.71	7.32	ns

Table 2-40 • 1.8 V LVCMOS Low SlewCommercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

|--|

HSTL Class I		VIL	VIH		VOL	VOH	IOL	ЮН	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA²	μA²
8 mA	-0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI - 0.4	8	8	39	32	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

2. Currents are measured at 85°C junction temperature.



Figure 2-16 • AC Loading

Table 2-61 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: **Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-62 • HSTL Class I

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = .4 V, VREF = 0.75 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.66	3.18	0.04	2.12	0.43	3.24	3.14			5.47	5.38	ns
-1	0.56	2.70	0.04	1.81	0.36	2.75	2.67			4.66	4.58	ns
-2	0.49	2.37	0.03	1.59	0.32	2.42	2.35			4.09	4.02	ns

ProASIC3E DC and Switching Characteristics

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-75 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class II		VIL	VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA²	μA²
21 mA	-0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21	109	103	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

2. Currents are measured at 85°C junction temperature.



Figure 2-21 • AC Loading

Table 2-76 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-77 • SSTL3 Class II

```
Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 1.5 V
```

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.66	2.07	0.04	1.25	0.43	2.10	1.67			4.34	3.91	ns
-1	0.56	1.76	0.04	1.06	0.36	1.79	1.42			3.69	3.32	ns
-2	0.49	1.54	0.03	0.93	0.32	1.57	1.25			3.24	2.92	ns

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ProASIC3E DC and Switching Characteristics

DC Parameter	Description	Min.	Тур.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL ¹	Output Lower Current	0.65	0.91	1.16	mA
IOH ¹	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
IIH ²	Input High Leakage Current			10	μA
IIL ²	Input Low Leakage Current			10	μΑ
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage ²	100	350		mV

Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels

Notes:

1. IOL/IOH defined by VODIFF/(Resistor Network).

2. Currents are measured at 85°C junction temperature.

Table 2-79 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)
1.075	1.325	Cross point	-

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

ProASIC3E DC and Switching Characteristics

Output Register





Timing Characteristics

Table 2-87 • Output Data Register Propagation DelaysCommercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{OCLKQ}	Clock-to-Q of the Output Data Register	0.59	0.67	0.79	ns
t _{OSUD}	Data Setup Time for the Output Data Register	0.31	0.36	0.42	ns
t _{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t _{OSUE}	Enable Setup Time for the Output Data Register	0.44	0.50	0.59	ns
t _{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t _{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.80	0.91	1.07	ns
t _{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.80	0.91	1.07	ns
t _{OREMCLR}	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	0.00	ns
t _{ORECCLR}	Asynchronous Clear Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
t _{OREMPRE}	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	0.00	ns
t _{ORECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
t _{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
t _{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
t _{OCKMPWH}	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.41	0.48	ns
t _{OCKMPWL}	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.37	0.43	ns





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Iguie	2-33 -	Output	אטט	rinning	Diagram

Timing Characteristics

Table 2-92 • Output DDR Propagation DelaysCommercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{DDROCLKQ}	Clock-to-Out of DDR for Output DDR	0.70	0.80	0.94	ns
t _{DDROSUD1}	Data_F Data Setup for Output DDR	0.38	0.43	0.51	ns
t _{DDROSUD2}	Data_R Data Setup for Output DDR	0.38	0.43	0.51	ns
t _{DDROHD1}	Data_F Data Hold for Output DDR	0.00	0.00	0.00	ns
t _{DDROHD2}	Data_R Data Hold for Output DDR	0.00	0.00	0.00	ns
t _{DDROCLR2Q}	Asynchronous Clear-to-Out for Output DDR	0.80	0.91	1.07	ns
t _{DDROREMCLR}	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	0.00	ns
t _{DDRORECCLR}	Asynchronous Clear Recovery Time for Output DDR	0.22	0.25	0.30	ns
t _{DDROWCLR1}	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	0.25	0.30	ns
t _{DDROCKMPWH}	Clock Minimum Pulse Width High for the Output DDR	0.36	0.41	0.48	ns
t _{DDROCKMPWL}	Clock Minimum Pulse Width Low for the Output DDR	0.32	0.37	0.43	ns
F _{DDOMAX}	Maximum Frequency for the Output DDR	1404	1232	1048	MHz



4 – Package Pin Assignments

PQ208



Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/products/fpga-soc/solutions*.



Package Pin Assignments

PQ208			PQ208	PQ208			
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function		
1	GND	40	VCCIB6	79	IO194NDB5V0		
2	GNDQ	41	GND	80	IO194PDB5V0		
3	VMV7	42	IO244PDB6V1	81	GND		
4	GAB2/IO308PSB7V4	43	IO244NDB6V1	82	IO184NDB4V3		
5	GAA2/IO309PDB7V4	44	GEC1/IO236PDB6V0	83	IO184PDB4V3		
6	IO309NDB7V4	45	GEC0/IO236NDB6V0	84	IO180NDB4V3		
7	GAC2/IO307PDB7V4	46	GEB1/IO235PPB6V0	85	IO180PDB4V3		
8	IO307NDB7V4	47	GEA1/IO234PPB6V0	86	IO176NDB4V2		
9	IO303PDB7V3	48	GEB0/IO235NPB6V0	87	IO176PDB4V2		
10	IO303NDB7V3	49	GEA0/IO234NPB6V0	88	VCC		
11	IO299PDB7V3	50	VMV6	89	VCCIB4		
12	IO299NDB7V3	51	GNDQ	90	IO170NDB4V2		
13	IO295PDB7V2	52	GND	91	IO170PDB4V2		
14	IO295NDB7V2	53	VMV5	92	IO166NDB4V1		
15	IO291PSB7V2	54	GNDQ	93	IO166PDB4V1		
16	VCC	55	IO233NDB5V4	94	IO156NDB4V0		
17	GND	56	GEA2/IO233PDB5V4	95	GDC2/IO156PDB4V0		
18	VCCIB7	57	IO232NDB5V4	96	IO154NPB4V0		
19	IO285PDB7V1	58	GEB2/IO232PDB5V4	97	GND		
20	IO285NDB7V1	59	IO231NDB5V4	98	GDB2/IO155PSB4V0		
21	IO279PSB7V0	60	GEC2/IO231PDB5V4	99	GDA2/IO154PPB4V0		
22	GFC1/IO275PSB7V0	61	IO230PSB5V4	100	GNDQ		
23	GFB1/IO274PDB7V0	62	VCCIB5	101	TCK		
24	GFB0/IO274NDB7V0	63	IO218NDB5V3	102	TDI		
25	VCOMPLF	64	IO218PDB5V3	103	TMS		
26	GFA0/IO273NPB6V4	65	GND	104	VMV4		
27	VCCPLF	66	IO214PSB5V2	105	GND		
28	GFA1/IO273PPB6V4	67	IO212NDB5V2	106	VPUMP		
29	GND	68	IO212PDB5V2	107	GNDQ		
30	GFA2/IO272PDB6V4	69	IO208NDB5V1	108	TDO		
31	IO272NDB6V4	70	IO208PDB5V1	109	TRST		
32	GFB2/IO271PPB6V4	71	VCC	110	VJTAG		
33	GFC2/IO270PPB6V4	72	VCCIB5	111	VMV3		
34	IO271NPB6V4	73	IO202NDB5V1	112	GDA0/IO153NPB3V4		
35	IO270NPB6V4	74	IO202PDB5V1	113	GDB0/IO152NPB3V4		
36	VCC	75	IO198NDB5V0	114	GDA1/IO153PPB3V4		
37	IO252PDB6V2	76	IO198PDB5V0	115	GDB1/IO152PPB3V4		
38	IO252NDB6V2	77	IO197NDB5V0	116	GDC0/IO151NDB3V4		
39	IO248PSB6V1	78	IO197PDB5V0	117	GDC1/IO151PDB3V4		

Package Pin Assignments

	FG324	FG324			FG324
Pin Number	A3PE3000 FBGA	Pin Number	A3PE3000 FBGA	Pin Number	A3PE3000 FBGA
G1	GND	J1	IO267NDB6V4	L1	IO263NDB6V3
G2	IO287PDB7V1	J2	GFA0/IO273NDB6V4	L2	VCCIB6
G3	IO287NDB7V1	J3	VCOMPLF	L3	IO259PDB6V3
G4	IO283PPB7V1	J4	GFA2/IO272PDB6V4	L4	IO259NDB6V3
G5	VCCIB7	J5	GFB0/IO274NPB7V0	L5	GND
G6	IO279PDB7V0	J6	GFC0/IO275NDB7V0	L6	IO270NPB6V4
G7	IO291NPB7V2	J7	GFC1/IO275PDB7V0	L7	VCC
G8	VCC	J8	GND	L8	VCC
G9	IO26NDB0V3	J9	GND	L9	GND
G10	IO34NDB0V4	J10	GND	L10	GND
G11	VCC	J11	GND	L11	VCC
G12	IO94NPB2V1	J12	GCA2/IO115PDB3V0	L12	VCC
G13	IO98PDB2V2	J13	GCA1/IO114PDB3V0	L13	IO132PDB3V2
G14	VCCIB2	J14	GCA0/IO114NDB3V0	L14	GND
G15	GCC0/IO112NPB2V3	J15	GCB0/IO113NDB2V3	L15	IO117NDB3V0
G16	IO104PDB2V2	J16	VCOMPLC	L16	IO128NPB3V1
G17	IO104NDB2V2	J17	IO120NPB3V0	L17	VCCIB3
G18	GND	J18	IO108NDB2V3	L18	IO124PPB3V1
H1	IO267PDB6V4	K1	IO263PDB6V3	M1	GND
H2	VCCIB7	K2	GFA1/IO273PDB6V4	M2	IO255PDB6V2
H3	IO283NPB7V1	K3	VCCPLF	M3	IO255NDB6V2
H4	GFB1/IO274PPB7V0	K4	IO272NDB6V4	M4	IO251PPB6V2
H5	GND	K5	GFC2/IO270PPB6V4	M5	VCCIB6
H6	IO279NDB7V0	K6	GFB2/IO271PDB6V4	M6	GEB0/IO235NDB6V0
H7	VCC	K7	IO271NDB6V4	M7	GEB1/IO235PDB6V0
H8	VCC	K8	GND	M8	VCC
H9	GND	K9	GND	M9	IO192PPB4V4
H10	GND	K10	GND	M10	IO154NPB4V0
H11	VCC	K11	GND	M11	VCC
H12	VCC	K12	IO115NDB3V0	M12	GDA0/IO153NPB3V4
H13	IO98NDB2V2	K13	GCB2/IO116PDB3V0	M13	IO132NDB3V2
H14	GND	K14	IO116NDB3V0	M14	VCCIB3
H15	GCB1/IO113PDB2V3	K15	GCC2/IO117PDB3V0	M15	IO134NDB3V2
H16	GCC1/IO112PPB2V3	K16	VCCPLC	M16	IO134PDB3V2
H17	VCCIB2	K17	IO124NPB3V1	M17	IO128PPB3V1
H18	IO108PDB2V3	K18	IO120PPB3V0	M18	GND



FG484						
Pin Number	A3PE600 Function					
V15	IO69NDB4V0					
V16	GDB2/IO69PDB4V0					
V17	TDI					
V18	GNDQ					
V19	TDO					
V20	GND					
V21	NC					
V22	IO63NDB3V1					
W1	NC					
W2	NC					
W3	NC					
W4	GND					
W5	IO100NDB5V2					
W6	GEB2/IO100PDB5V2					
W7	IO99NDB5V2					
W8	IO88NDB5V0					
W9	IO88PDB5V0					
W10	IO89NDB5V0					
W11	IO80NDB4V1					
W12	IO81NDB4V1					
W13	IO81PDB4V1					
W14	IO70NDB4V0					
W15	GDC2/IO70PDB4V0					
W16	IO68NDB4V0					
W17	GDA2/IO68PDB4V0					
W18	TMS					
W19	GND					
W20	NC					
W21	NC					
W22	NC					
Y1	VCCIB6					
Y2	NC					
Y3	NC					
Y4	IO98NDB5V2					
Y5	GND					
Y6	IO94NDB5V1					

FG484						
A3PE600 Function						
IO94PDB5V1						
VCC						
VCC						
IO89PDB5V0						
IO80PDB4V1						
IO78NPB4V1						
NC						
VCC						
VCC						
NC						
NC						
GND						
NC						
NC						
NC						
VCCIB3						



FG676



Note

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5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the ProASIC3E datasheet.

Revision	Changes	Page
Revision 15 (June 2015)	Updated "ProASIC3E Ordering Information". Interchanged the positions of Y-Security Feature and I- Application (Temperature Range) (SAR 67296).	1-111
	Added Note "Only devices with package size greater than or equal to 5x5 are supported".	
	Updated Commercial and Industrial Junction Temperatures (SAR 67588).	
	Added the A3PE3000 package to Table 2-5 (SARs 52320 and 58737).	2-5
	Updated "VCCIBx I/O Supply Voltage" (SAR 43323).	3-1
Revision 14 (May 2014)	Added 2 mA and 6 mA I/O short currents values in"I/O Short Currents IOSH/IOSL" (SAR 56295).	2-22 2-24
	Added 2 mA and 6 mA minimum and maximum DC input and output levels in "Minimum and Maximum DC Input and Output Levels" (SAR 56295).	2-25 2-25
	Added 3.3 V LVTTL / 3.3 V LVCMOS High Slew Commercial-Case Conditions for 2 mA and 6 mA in "3.3 V LVTTL / 3.3 V LVCMOS High Slew" (SAR 56295).	
	Added 3.3 V LVTTL / 3.3 V LVCMOS Low Slew Commercial-Case Conditions for 2 mA and 6 mA in "3.3 V LVTTL / 3.3 V LVCMOS Low Slew" (SAR 56295).	
Revision 13 (January 2013)	In the "Features and Benefits" section, updated the Clock Conditioning Circuit (CCC) and PLL Wide Input Frequency Range from '1.5 MHz to 200 MHz' to '1.5MHz to 350 MHz' based on Table 2-98 (SAR 22196).	1-1
	The "ProASIC3E Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43220).	1-111
	Added a note to "Recommended Operating Conditions ¹ " table (SAR 42716): The programming temperature range supported is $T_{ambient} = 0^{\circ}C$ to 85°C.	2-2
	The note in "ProASIC3E CCC/PLL Specification" table referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42571).	2-70
	Libero Integrated Design Environment (IDE) was changed to Libero System-on- Chip (SoC) throughout the document (SAR 40285).	NA
	Live at Power-Up (LAPU) has been replaced with 'Instant On'.	
Revision 12 (September 2012)	The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data.	1-1



Revision		Changes	Page	
Revision 9 (Aug 2009)	All references to speed grade	-F have been removed from this document.	N/A	
Product Brief v1.2				
	The "Pro I/Os with Advance definitions of hot-swap and co	ed I/O Standards" section was revised to add Id-sparing.	1-6	
DC and Switching Characteristics v1.3	3.3 V LVCMOS and 1.2 V L datasheet. This affects all ta LVCMOS data.	VCMOS Wide Range support was added to the ables that contained 3.3 V LVCMOS and 1.2 V	N/A	
	IIL and IIH input leakage cur Maximum DC Input and Outpu	rrent information was added to all "Minimum and it Levels" tables.	N/A	
	–F was removed from the data	asheet. The speed grade is no longer supported.	N/A	
	In the Table 2-2 • Recomme voltage" and note 4 are new.	ended Operating Conditions ¹ "3.0 V DC supply	2-2	
	The Table 2-4 • Overshoot and	d Undershoot Limits ¹ table was updated.	2-3	
	The Table 2-6 • Temperature table was updated.	and Voltage Derating Factors for Timing Delays	2-5	
	There are new parameters an table.	nd data was updated in the Table 2-99 • RAM4K9	2-76	
	There are new parameters • RAM512X18 table.	s and data was updated in the Table 2-100	2-77	
Revision 8 (Feb 2008)	Table 1-2 • ProASIC3E FPGAs Package Sizes Dimensions is new.			
Product Brief v1.1				
Revision 7 (Jun 2008) DC and Switching	The title of Table 2-4 • Overshoot and Undershoot Limits ¹ was modified to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted.			
	Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels was updated.			
Revision 6 (Jun 2008)	The A3PE600 "FG484" table was missing G22. The pin and its function were added to the table.		4-27	
Revision 5 (Jun 2008) Packaging v1.4	The naming conventions changed for the following pins in the "FG484" for the A3PE600:		4-22	
	Pin Number	New Function Name		
	J19	IO45PPB2V1		
	K20	IO45NPB2V1		
	M2	IO114NPB6V1		
	N1	IO114PPB6V1		
	N4	GFC2/IO115PPB6V1		
	P3	IO115NPB6V1		
Revision 4 (Apr 2008) Product Brief v1.0	The product brief portion of the datasheet was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.			
Packaging v1.3	The "FG324" package diagram was replaced.			



Datasheet Information

Revision	Changes	Page
Advance v0.5 (continued)	The "I/O User Input/Output" pin description was updated to include information on what happens when the pin is unused.	2-50
	The "JTAG Pins" section was updated to include information on what happens when the pin is unused.	2-51
	The "Programming" section was updated to include information concerning serialization.	2-53
	The "JTAG 1532" section was updated to include SAMPLE/PRELOAD information.	2-54
	The "DC and Switching Characteristics" chapter was updated with new information.	Starting on page 3-1
	Table 3-6 was updated.	3-5
	In Table 3-10, PAC4 was updated.	3-8
	Table 3-19 was updated.	3-20
	The note in Table 3-24 was updated.	3-23
	All Timing Characteristics tables were updated from LVTTL to Register Delays	3-26 to 3-64
	The Timing Characteristics for RAM4K9, RAM512X18, and FIFO were updated.	3-74 to 3-79
	F _{TCKMAX} was updated in Table 3-98.	3-80
Advance v0.4 (October 2005)	The "Packaging Tables" table was updated.	ii
Advance v0.3	Figure 2-11 was updated.	2-9
	The "Clock Resources (VersaNets)" section was updated.	2-9
	The "VersaNet Global Networks and Spine Access" section was updated.	2-9
	The "PLL Macro" section was updated.	2-15
	Figure 2-27 was updated.	2-28
	Figure 2-20 was updated.	2-19
	Table 2-5 was updated.	2-25
	Table 2-6 was updated.	2-25
	The "FIFO Flag Usage Considerations" section was updated.	2-27
	Table 2-33 was updated.	2-51
	Figure 2-24 was updated.	2-31
	The "Cold-Sparing Support" section is new.	2-34
	Table 2-45 was updated.	2-64
	Table 2-48 was updated.	2-81
	Pin descriptions in the "JTAG Pins" section were updated.	2-51
	The "Pin Descriptions" section was updated.	2-50
	Table 3-7 was updated.	3-6