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### Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

#### Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	270
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/a3pe600-2fg484">https://www.e-xfl.com/product-detail/microchip-technology/a3pe600-2fg484</a>

## Temperature Grade Offerings

Package	A3PE600	A3PE1500	A3PE3000
<b>Cortex-M1 Devices</b>		<b>M1A3PE1500</b>	<b>M1A3PE3000</b>
PQ208	C, I	C, I	C, I
FG256	C, I	–	–
FG324	–	–	C, I
FG484	C, I	C, I	C, I
FG676	–	C, I	–
FG896	–	–	C, I

*Note:* C = Commercial temperature range: 0°C to 70°C ambient temperature  
 I = Industrial temperature range: –40°C to 85°C ambient temperature

## Speed Grade and Temperature Grade Matrix

Temperature Grade	Std.	–1	–2
C <sup>1</sup>	✓	✓	✓
I <sup>2</sup>	✓	✓	✓

*Notes:*

1. C = Commercial temperature range: 0°C to 70°C ambient temperature
2. I = Industrial temperature range: –40°C to 85°C ambient temperature

References made to ProASIC3E devices also apply to ARM-enabled ProASIC3E devices. The ARM-enabled part numbers start with M1 (Cortex-M1).

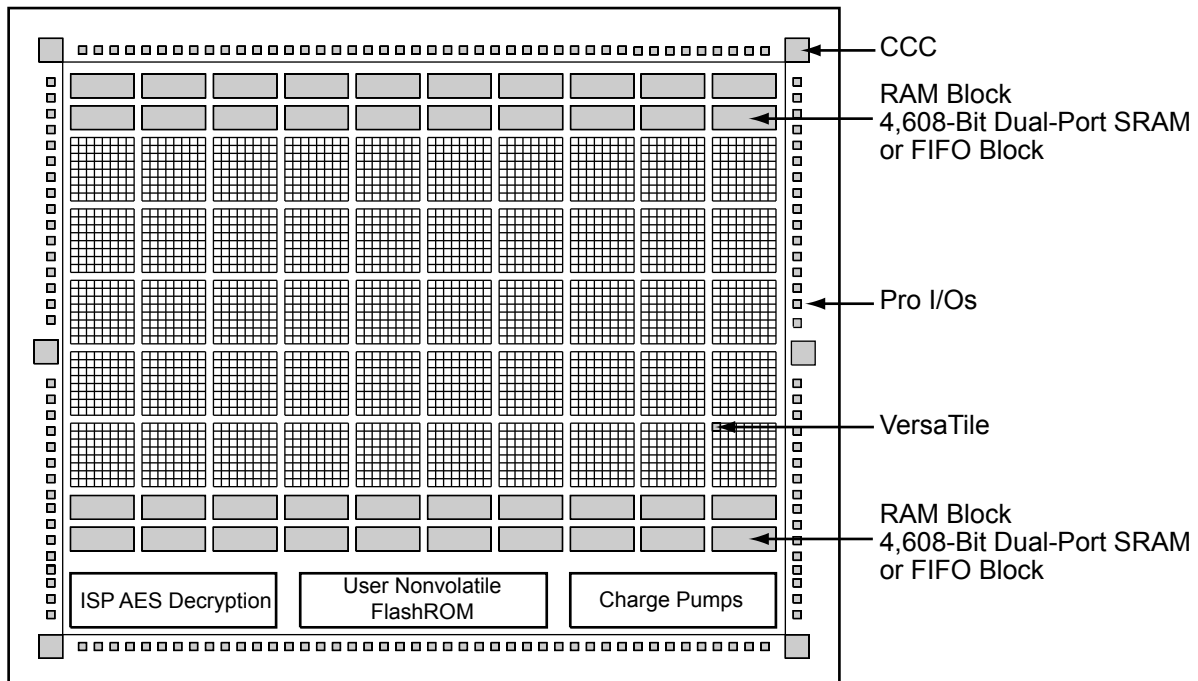
Contact your local Microsemi SoC Products Group representative for device availability:  
[www.microsemi.com/index.php?option=com\\_content&id=135&lang=en&view=article](http://www.microsemi.com/index.php?option=com_content&id=135&lang=en&view=article).

## Advanced Architecture

The proprietary ProASIC3E architecture provides granularity comparable to standard-cell ASICs. The ProASIC3E device consists of five distinct and programmable architectural features (Figure 1-1 on page 3):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- Pro I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the ProASIC3E core tile as either a three-input lookup table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC family of third-generation architecture Flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.



**Figure 1-1 • ProASIC3E Device Architecture Overview**

**Table 2-9 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings (continued)  
(continued)<sup>1</sup>**

	C <sub>LOAD</sub> (pF)	VCCI (V)	Static Power PDC3 (mW) <sup>2</sup>	Dynamic Power PAC10 (μW/MHz) <sup>3</sup>
SSTL3 (I)	30	3.3	26.02	114.87
SSTL3 (II)	30	3.3	42.21	131.76
<b>Differential</b>				
LVDS/B-LVDS/M-LVDS	–	2.5	7.70	89.62
LVPECL	–	3.3	19.42	168.02
<i>Notes:</i>				
1. Dynamic power consumption is given for standard load and software default drive strength and output slew.				
2. PDC3 is the static power (where applicable) measured on VCCI.				
3. PAC10 is the total dynamic power measured on VCC and VCCI.				
4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.				

## Power Consumption of Various Internal Resources

**Table 2-10 • Different Components Contributing to the Dynamic Power Consumption in ProASIC3E Devices**

Parameter	Definition	Device-Specific Dynamic Contributions (μW/MHz)		
		A3PE600	A3PE1500	A3PE3000
PAC1	Clock contribution of a Global Rib	12.77	16.21	19.7
PAC2	Clock contribution of a Global Spine	1.85	3.06	4.16
PAC3	Clock contribution of a VersaTile row	0.88		
PAC4	Clock contribution of a VersaTile used as a sequential module	0.12		
PAC5	First contribution of a VersaTile used as a sequential module	0.07		
PAC6	Second contribution of a VersaTile used as a sequential module	0.29		
PAC7	Contribution of a VersaTile used as a combinatorial module	0.29		
PAC8	Average contribution of a routing net	0.70		
PAC9	Contribution of an I/O input pin (standard-dependent)	See <a href="#">Table 2-8 on page 2-6</a> .		
PAC10	Contribution of an I/O output pin (standard-dependent)	See <a href="#">Table 2-9 on page 2-7</a>		
PAC11	Average contribution of a RAM block during a read operation	25.00		
PAC12	Average contribution of a RAM block during a write operation	30.00		
PAC13	Static PLL contribution	2.55 mW		
PAC14	Dynamic contribution for PLL	2.60		

*Note:* For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power calculator or SmartPower in Libero SoC.



**Table 2-14 • Summary of Maximum and Minimum DC Input Levels  
Applicable to Commercial and Industrial Conditions**

DC I/O Standards	Commercial <sup>1</sup>		Industrial <sup>2</sup>	
	IIL <sup>3</sup>	IIH <sup>4</sup>	IIL <sup>3</sup>	IIH <sup>4</sup>
	μA	μA	μA	μA
3.3 V LVTTTL / 3.3 V LVCMOS	10	10	15	15
3.3 V LVCMOS Wide Range	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15
3.3 V GTL	10	10	15	15
2.5 V GTL	10	10	15	15
3.3 V GTL+	10	10	15	15
2.5 V GTL+	10	10	15	15
HSTL (I)	10	10	15	15
HSTL (II)	10	10	15	15
SSTL2 (I)	10	10	15	15
SSTL2 (II)	10	10	15	15
SSTL3 (I)	10	10	15	15
SSTL3 (II)	10	10	15	15

**Notes:**

1. Commercial range ( $0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$ )
2. Industrial range ( $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ )
3. IIL is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
4. IIH is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges.

### Timing Characteristics

**Table 2-43 • 1.5 V LVCMOS High Slew**  
Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$ , Worst-Case  $V_{CCI} = 1.4\text{ V}$

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.66	8.53	0.04	1.70	2.14	0.43	7.26	8.53	3.39	2.79	9.50	10.77	ns
	-1	0.56	7.26	0.04	1.44	1.82	0.36	6.18	7.26	2.89	2.37	8.08	9.16	ns
	-2	0.49	6.37	0.03	1.27	1.60	0.32	5.42	6.37	2.53	2.08	7.09	8.04	ns
4 mA	Std.	0.66	5.41	0.04	1.70	2.14	0.43	5.22	5.41	3.75	3.48	7.45	7.65	ns
	-1	0.56	4.60	0.04	1.44	1.82	0.36	4.44	4.60	3.19	2.96	6.34	6.50	ns
	-2	0.49	4.04	0.03	1.27	1.60	0.32	3.89	4.04	2.80	2.60	5.56	5.71	ns
6 mA	Std.	0.66	4.80	0.04	1.70	2.14	0.43	4.89	4.75	3.83	3.67	7.13	6.98	ns
	-1	0.56	4.09	0.04	1.44	1.82	0.36	4.16	4.04	3.26	3.12	6.06	5.94	ns
	-2	0.49	3.59	0.03	1.27	1.60	0.32	3.65	3.54	2.86	2.74	5.32	5.21	ns
8 mA	Std.	0.66	4.42	0.04	1.70	2.14	0.43	4.50	3.62	3.96	4.37	6.74	5.86	ns
	-1	0.56	3.76	0.04	1.44	1.82	0.36	3.83	3.08	3.37	3.72	5.73	4.98	ns
	-2	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns
12 mA	Std.	0.66	4.42	0.04	1.70	2.14	0.43	4.50	3.62	3.96	4.37	6.74	5.86	ns
	-1	0.56	3.76	0.04	1.44	1.82	0.36	3.83	3.08	3.37	3.72	5.73	4.98	ns
	-2	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns

**Notes:**

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

**Table 2-44 • 1.5 V LVCMOS Low Slew**  
Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$ , Worst-Case  $V_{CCI} = 1.4\text{ V}$

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.66	14.11	0.04	1.70	2.14	0.43	14.37	13.14	3.40	2.68	16.61	15.37	ns
	-1	0.56	12.00	0.04	1.44	1.82	0.36	12.22	11.17	2.90	2.28	14.13	13.08	ns
	-2	0.49	10.54	0.03	1.27	1.60	0.32	10.73	9.81	2.54	2.00	12.40	11.48	ns
4 mA	Std.	0.66	11.23	0.04	1.70	2.14	0.43	11.44	9.87	3.77	3.36	13.68	12.10	ns
	-1	0.56	9.55	0.04	1.44	1.82	0.36	9.73	8.39	3.21	2.86	11.63	10.29	ns
	-2	0.49	8.39	0.03	1.27	1.60	0.32	8.54	7.37	2.81	2.51	10.21	9.04	ns
6 mA	Std.	0.66	10.45	0.04	1.70	2.14	0.43	10.65	9.24	3.84	3.55	12.88	11.48	ns
	-1	0.56	8.89	0.04	1.44	1.82	0.36	9.06	7.86	3.27	3.02	10.96	9.76	ns
	-2	0.49	7.81	0.03	1.27	1.60	0.32	7.95	6.90	2.87	2.65	9.62	8.57	ns
8 mA	Std.	0.66	10.02	0.04	1.70	2.14	0.43	10.20	9.23	3.97	4.22	12.44	11.47	ns
	-1	0.56	8.52	0.04	1.44	1.82	0.36	8.68	7.85	3.38	3.59	10.58	9.75	ns
	-2	0.49	7.48	0.03	1.27	1.60	0.32	7.62	6.89	2.97	3.15	9.29	8.56	ns
12 mA	Std.	0.66	10.02	0.04	1.70	2.14	0.43	10.20	9.23	3.97	4.22	12.44	11.47	ns
	-1	0.56	8.52	0.04	1.44	1.82	0.36	8.68	7.85	3.38	3.59	10.58	9.75	ns
	-2	0.49	7.48	0.03	1.27	1.60	0.32	7.62	6.89	2.97	3.15	9.29	8.56	ns

**Note:** For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

### HSTL Class I

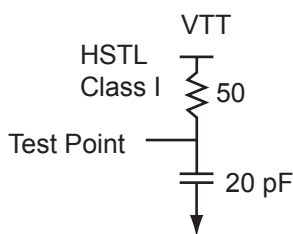
High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-60 • Minimum and Maximum DC Input and Output Levels**

HSTL Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
8 mA	-0.3	VREF - 0.1	VREF + 0.1	3.6	0.4	VCCI - 0.4	8	8	39	32	10	10

**Notes:**

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.



**Figure 2-16 • AC Loading**

**Table 2-61 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C <sub>LOAD</sub> (pF)
VREF - 0.1	VREF + 0.1	0.75	0.75	0.75	20

*Note:* \*Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

### Timing Characteristics

**Table 2-62 • HSTL Class I**

Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = .4 V, VREF = 0.75 V

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.66	3.18	0.04	2.12	0.43	3.24	3.14			5.47	5.38	ns
-1	0.56	2.70	0.04	1.81	0.36	2.75	2.67			4.66	4.58	ns
-2	0.49	2.37	0.03	1.59	0.32	2.42	2.35			4.09	4.02	ns

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

### SSTL2 Class I

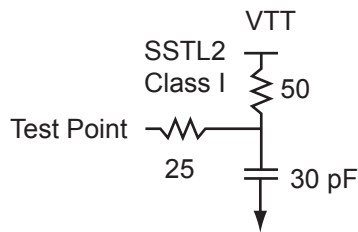
Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-66 • Minimum and Maximum DC Input and Output Levels**

SSTL2 Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	mA <sup>1</sup>	mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
15 mA	-0.3	VREF - 0.2	VREF + 0.2	3.6	0.54	VCCI - 0.62	15	15	87	83	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.



**Figure 2-18 • AC Loading**

**Table 2-67 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C <sub>LOAD</sub> (pF)
VREF - 0.2	VREF + 0.2	1.25	1.25	1.25	30

Note: \*Measuring point = V<sub>trip</sub>. See Table 2-15 on page 2-18 for a complete table of trip points.

### Timing Characteristics

**Table 2-68 • SSTL 2 Class I**

Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V,  
Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.66	2.13	0.04	1.33	0.43	2.17	1.85			4.40	4.08	ns
-1	0.56	1.81	0.04	1.14	0.36	1.84	1.57			3.74	3.47	ns
-2	0.49	1.59	0.03	1.00	0.32	1.62	1.38			3.29	3.05	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

### Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

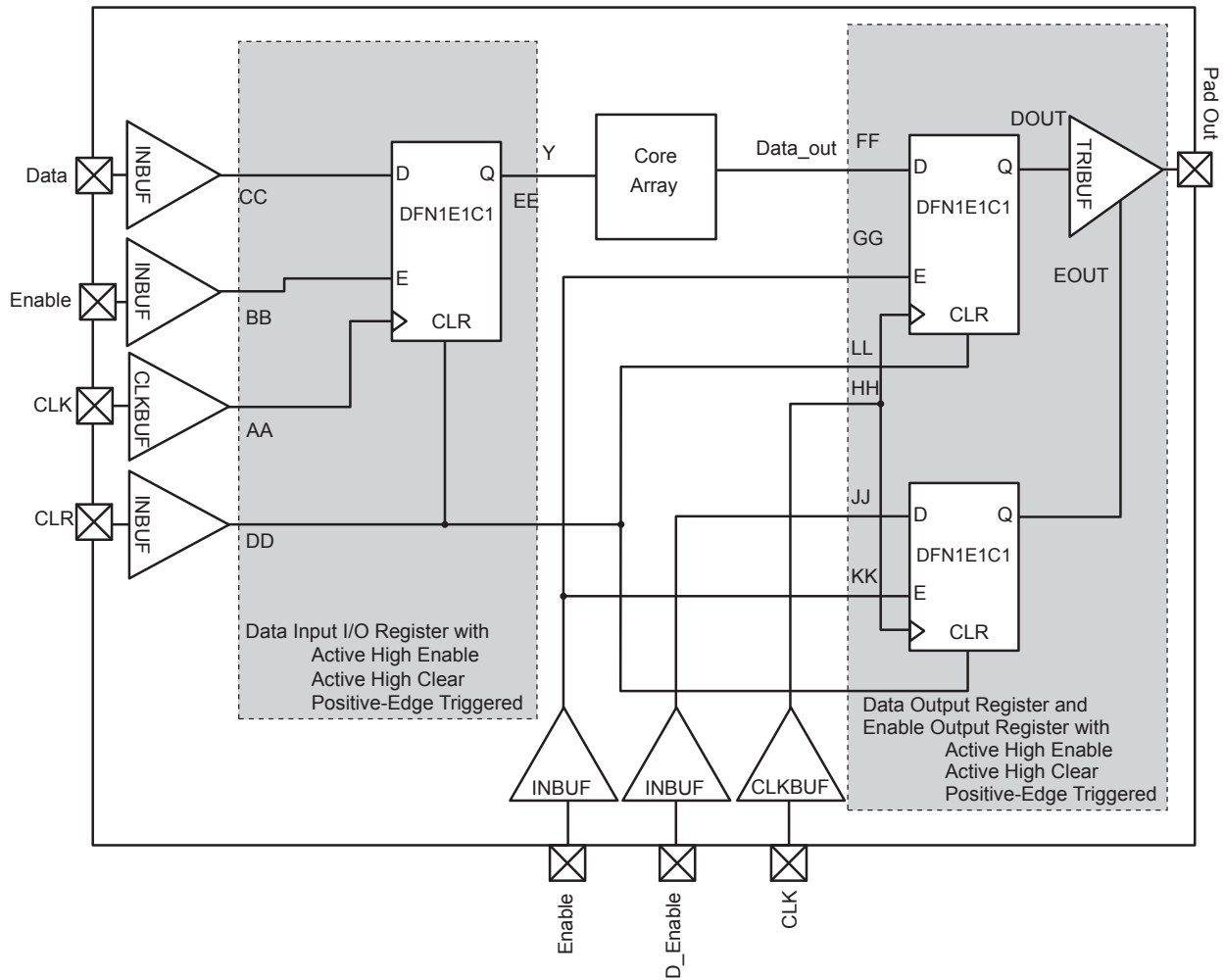


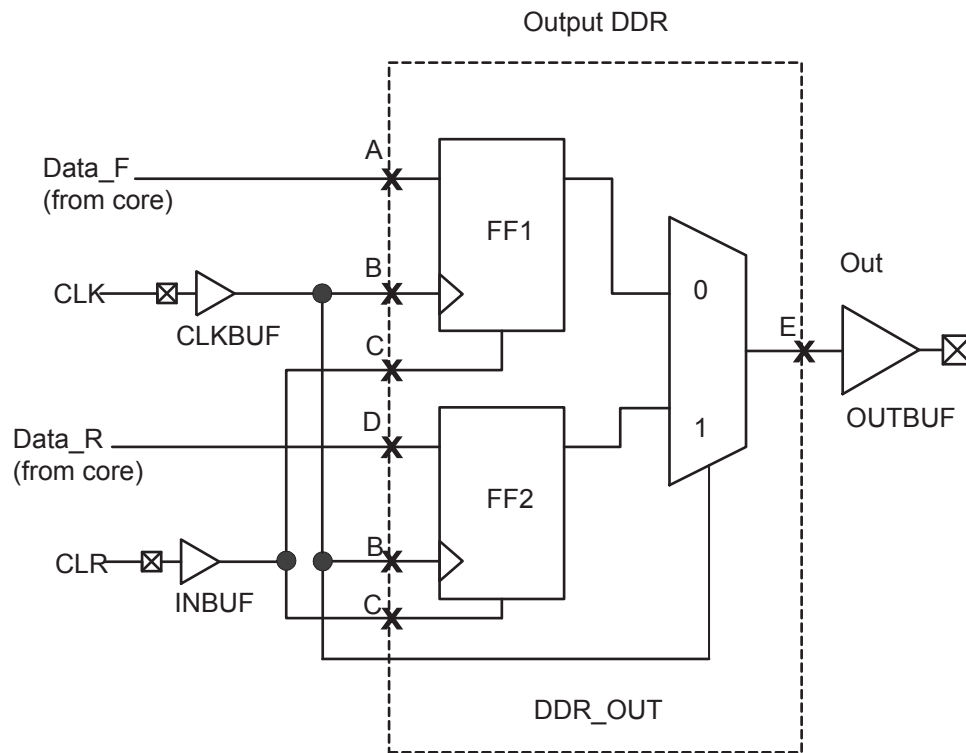
Figure 2-26 • Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

**Table 2-85 • Parameter Definition and Measuring Nodes**

<b>Parameter Name</b>	<b>Parameter Definition</b>	<b>Measuring Nodes (from, to)*</b>
$t_{OCLKQ}$	Clock-to-Q of the Output Data Register	HH, DOUT
$t_{OSUD}$	Data Setup Time for the Output Data Register	FF, HH
$t_{OHD}$	Data Hold Time for the Output Data Register	FF, HH
$t_{OSUE}$	Enable Setup Time for the Output Data Register	GG, HH
$t_{OHE}$	Enable Hold Time for the Output Data Register	GG, HH
$t_{OCLR2Q}$	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
$t_{OECLKQ}$	Clock-to-Q of the Output Enable Register	HH, EOUT
$t_{OESUD}$	Data Setup Time for the Output Enable Register	JJ, HH
$t_{OEHD}$	Data Hold Time for the Output Enable Register	JJ, HH
$t_{OESUE}$	Enable Setup Time for the Output Enable Register	KK, HH
$t_{OEHE}$	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
$t_{iCLKQ}$	Clock-to-Q of the Input Data Register	AA, EE
$t_{iSUD}$	Data Setup Time for the Input Data Register	CC, AA
$t_{iHD}$	Data Hold Time for the Input Data Register	CC, AA
$t_{iSUE}$	Enable Setup Time for the Input Data Register	BB, AA
$t_{iHE}$	Enable Hold Time for the Input Data Register	BB, AA
$t_{iCLR2Q}$	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{iREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{iRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

*Note:* \*See Figure 2-26 on page 2-55 for more information.

## Output DDR Module



**Figure 2-32 • Output DDR Timing Model**

**Table 2-91 • Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

### Timing Characteristics

**Table 2-95 • A3PE600 Global Resource**  
Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2		-1		Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	0.83	1.04	0.94	1.18	1.11	1.39	ns
$t_{RCKH}$	Input High Delay for Global Clock	0.81	1.06	0.93	1.21	1.09	1.42	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.25		0.28		0.33	ns

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

**Table 2-96 • A3PE1500 Global Resource**  
Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2		-1		Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	1.07	1.29	1.22	1.47	1.43	1.72	ns
$t_{RCKH}$	Input High Delay for Global Clock	1.06	1.32	1.21	1.50	1.42	1.76	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

**Table 2-97 • A3PE3000 Global Resource**  
Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2		-1		Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	1.41	1.62	1.60	1.85	1.88	2.17	ns
$t_{RCKH}$	Input High Delay for Global Clock	1.40	1.66	1.59	1.89	1.87	2.22	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.26		0.29		0.35	ns

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.



## Timing Characteristics

**Table 2-99 • RAM4K9**

 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$ 

Parameter	Description	-2	-1	Std.	Units
$t_{AS}$	Address setup time	0.25	0.28	0.33	ns
$t_{AH}$	Address hold time	0.00	0.00	0.00	ns
$t_{ENS}$	REN, WEN setup time	0.14	0.16	0.19	ns
$t_{ENH}$	REN, WEN hold time	0.10	0.11	0.13	ns
$t_{BKS}$	BLK setup time	0.23	0.27	0.31	ns
$t_{BKH}$	BLK hold time	0.02	0.02	0.02	ns
$t_{DS}$	Input data (DIN) setup time	0.18	0.21	0.25	ns
$t_{DH}$	Input data (DIN) hold time	0.00	0.00	0.00	ns
$t_{CKQ1}$	Clock High to new data valid on DOUT (output retained, WMODE = 0)	1.79	2.03	2.39	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.36	2.68	3.15	ns
$t_{CKQ2}$	Clock High to new data valid on DOUT (pipelined)	0.89	1.02	1.20	ns
$t_{C2CWWL}^1$	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Closing Edge	0.33	0.28	0.25	ns
$t_{C2CWWH}^1$	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge	0.30	0.26	0.23	ns
$t_{C2CRWH}^1$	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.45	0.38	0.34	ns
$t_{C2CWRH}^1$	Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge	0.49	0.42	0.37	ns
$t_{RSTBQ}$	RESET Low to data out Low on DO (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on DO (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.21	0.24	0.29	ns
$t_{CYC}$	Clock cycle time	3.23	3.68	4.32	ns
$F_{MAX}$	Maximum frequency	310	272	231	MHz

**Notes:**

1. For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

FG484	
Pin Number	A3PE1500 Function
C21	NC
C22	VCCIB2
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0
D7	GAB0/IO01NDB0V0
D8	IO09PDB0V1
D9	IO13PDB0V1
D10	IO21PDB0V2
D11	IO31NDB0V3
D12	IO37NDB1V0
D13	IO37PDB1V0
D14	IO49NDB1V2
D15	IO49PDB1V2
D16	GBB1/IO56PDB1V3
D17	GBA0/IO57NDB1V3
D18	GBA1/IO57PDB1V3
D19	GND
D20	NC
D21	IO69PDB2V1
D22	NC
E1	NC
E2	IO218PPB7V3
E3	GND
E4	GAB2/IO220PDB7V3
E5	GAA2/IO221PDB7V3
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO09NDB0V1
E9	IO13NDB0V1
E10	IO21NDB0V2
E11	IO31PDB0V3
E12	IO35NDB1V0

FG484	
Pin Number	A3PE1500 Function
E13	IO41NDB1V1
E14	IO41PDB1V1
E15	GBC1/IO55PDB1V3
E16	GBB0/IO56NDB1V3
E17	GNDQ
E18	GBA2/IO58PDB2V0
E19	IO63NDB2V0
E20	GND
E21	IO69NDB2V1
E22	NC
F1	IO218NPB7V3
F2	IO216NDB7V3
F3	IO216PDB7V3
F4	IO220NDB7V3
F5	IO221NDB7V3
F6	VMV7
F7	VCCPLA
F8	GAC0/IO02NDB0V0
F9	GAC1/IO02PDB0V0
F10	IO23NDB0V2
F11	IO23PDB0V2
F12	IO35PDB1V0
F13	IO39NDB1V0
F14	IO45PDB1V1
F15	GBC0/IO55NDB1V3
F16	VCCPLB
F17	VMV2
F18	IO58NDB2V0
F19	IO63PDB2V0
F20	NC
F21	NC
F22	NC
G1	IO211NDB7V2
G2	IO211PDB7V2
G3	NC
G4	IO214PDB7V3

FG484	
Pin Number	A3PE1500 Function
G5	IO217PDB7V3
G6	GAC2/IO219PDB7V3
G7	VCOMPLA
G8	GNDQ
G9	IO19NDB0V2
G10	IO19PDB0V2
G11	IO25PDB0V3
G12	IO33PDB1V0
G13	IO39PDB1V0
G14	IO45NDB1V1
G15	GNDQ
G16	VCOMPLB
G17	GBB2/IO59PDB2V0
G18	IO62PDB2V0
G19	IO62NDB2V0
G20	IO71PDB2V2
G21	IO71NDB2V2
G22	NC
H1	IO209PSB7V2
H2	NC
H3	VCC
H4	IO214NDB7V3
H5	IO217NDB7V3
H6	IO219NDB7V3
H7	IO215PDB7V3
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO25NDB0V3
H12	IO33NDB1V0
H13	VCCIB1
H14	VCCIB1
H15	VMV1
H16	GBC2/IO60PDB2V0
H17	IO59NDB2V0
H18	IO67NDB2V1

FG484		FG484		FG484	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
N17	IO132NPB3V2	R9	VCCIB5	U1	IO240PPB6V0
N18	IO117NPB3V0	R10	VCCIB5	U2	IO238PDB6V0
N19	IO132PPB3V2	R11	IO196NDB5V0	U3	IO238NDB6V0
N20	GNDQ	R12	IO196PDB5V0	U4	GEB1/IO235PDB6V0
N21	IO126NDB3V1	R13	VCCIB4	U5	GEB0/IO235NDB6V0
N22	IO128PDB3V1	R14	VCCIB4	U6	VMV6
P1	IO247PDB6V1	R15	VMV3	U7	VCCPLE
P2	IO253PDB6V2	R16	VCCPLD	U8	IO233NPB5V4
P3	IO270NPB6V4	R17	GDB1/IO152PPB3V4	U9	IO222PPB5V3
P4	IO261NPB6V3	R18	GDC1/IO151PDB3V4	U10	IO206PDB5V1
P5	IO249PPB6V1	R19	IO138NDB3V3	U11	IO202PDB5V1
P6	IO259PDB6V3	R20	VCC	U12	IO194PDB5V0
P7	IO259NDB6V3	R21	IO130NDB3V2	U13	IO176NDB4V2
P8	VCCIB6	R22	IO134PDB3V2	U14	IO176PDB4V2
P9	GND	T1	IO243PPB6V1	U15	VMV4
P10	VCC	T2	IO245NDB6V1	U16	TCK
P11	VCC	T3	IO243NPB6V1	U17	VPUMP
P12	VCC	T4	IO241PDB6V0	U18	TRST
P13	VCC	T5	IO241NDB6V0	U19	GDA0/IO153NDB3V4
P14	GND	T6	GEC1/IO236PPB6V0	U20	IO144NDB3V3
P15	VCCIB3	T7	VCOMPLE	U21	IO140NDB3V3
P16	GDB0/IO152NPB3V4	T8	GNDQ	U22	IO142PDB3V3
P17	IO136NDB3V2	T9	GEA2/IO233PPB5V4	V1	IO239PDB6V0
P18	IO136PDB3V2	T10	IO206NDB5V1	V2	IO240NPB6V0
P19	IO138PDB3V3	T11	IO202NDB5V1	V3	GND
P20	VMV3	T12	IO194NDB5V0	V4	GEA1/IO234PDB6V0
P21	IO130PDB3V2	T13	IO186NDB4V4	V5	GEA0/IO234NDB6V0
P22	IO128NDB3V1	T14	IO186PDB4V4	V6	GNDQ
R1	IO247NDB6V1	T15	GNDQ	V7	GEC2/IO231PDB5V4
R2	IO245PDB6V1	T16	VCOMPLD	V8	IO222NPB5V3
R3	VCC	T17	VJTAG	V9	IO204NDB5V1
R4	IO249NPB6V1	T18	GDC0/IO151NDB3V4	V10	IO204PDB5V1
R5	IO251NDB6V2	T19	GDA1/IO153PDB3V4	V11	IO195NDB5V0
R6	IO251PDB6V2	T20	IO144PDB3V3	V12	IO195PDB5V0
R7	GEC0/IO236NPB6V0	T21	IO140PDB3V3	V13	IO178NDB4V3
R8	VMV5	T22	IO134NDB3V2	V14	IO178PDB4V3

FG484	
Pin Number	A3PE3000 Function
V15	IO155NDB4V0
V16	GDB2/IO155PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	IO146PDB3V4
V22	IO142NDB3V3
W1	IO239NDB6V0
W2	IO237PDB6V0
W3	IO230PSB5V4
W4	GND
W5	IO232NDB5V4
W6	GEB2/IO232PDB5V4
W7	IO231NDB5V4
W8	IO214NDB5V2
W9	IO214PDB5V2
W10	IO200NDB5V0
W11	IO192NDB4V4
W12	IO184NDB4V3
W13	IO184PDB4V3
W14	IO156NDB4V0
W15	GDC2/IO156PDB4V0
W16	IO154NDB4V0
W17	GDA2/IO154PDB4V0
W18	TMS
W19	GND
W20	IO150NDB3V4
W21	IO146NDB3V4
W22	IO148PPB3V4
Y1	VCCIB6
Y2	IO237NDB6V0
Y3	IO228NDB5V4
Y4	IO224NDB5V3
Y5	GND
Y6	IO220NDB5V3

FG484	
Pin Number	A3PE3000 Function
Y7	IO220PDB5V3
Y8	VCC
Y9	VCC
Y10	IO200PDB5V0
Y11	IO192PDB4V4
Y12	IO188NPB4V4
Y13	IO187PSB4V4
Y14	VCC
Y15	VCC
Y16	IO164NDB4V1
Y17	IO164PDB4V1
Y18	GND
Y19	IO158PPB4V0
Y20	IO150PDB3V4
Y21	IO148NPB3V4
Y22	VCCIB3

FG676	
Pin Number	A3PE1500 Function
R21	IO89NDB3V0
R22	GCB2/IO89PDB3V0
R23	IO90NDB3V0
R24	GCC2/IO90PDB3V0
R25	IO91PDB3V0
R26	IO91NDB3V0
T1	IO186PDB6V2
T2	IO185NDB6V2
T3	GNDQ
T4	IO180PDB6V1
T5	IO180NDB6V1
T6	IO188NDB6V2
T7	GFB2/IO188PDB6V2
T8	VCCIB6
T9	VCC
T10	GND
T11	GND
T12	GND
T13	GND
T14	GND
T15	GND
T16	GND
T17	GND
T18	VCC
T19	VCCIB3
T20	IO99PDB3V1
T21	IO99NDB3V1
T22	IO97PDB3V1
T23	IO97NDB3V1
T24	GNDQ
T25	IO93PPB3V0
T26	NC
U1	IO186NDB6V2
U2	IO184NDB6V2
U3	IO184PDB6V2
U4	IO182NDB6V1

FG676	
Pin Number	A3PE1500 Function
U5	IO182PDB6V1
U6	IO178PDB6V1
U7	IO178NDB6V1
U8	VCCIB6
U9	VCC
U10	GND
U11	GND
U12	GND
U13	GND
U14	GND
U15	GND
U16	GND
U17	GND
U18	VCC
U19	VCCIB3
U20	NC
U21	IO101NDB3V1
U22	IO101PDB3V1
U23	IO92NDB3V0
U24	IO92PDB3V0
U25	IO95PDB3V1
U26	IO93NPB3V0
V1	IO183PDB6V2
V2	IO183NDB6V2
V3	VMV6
V4	IO181PDB6V1
V5	IO181NDB6V1
V6	IO176PDB6V1
V7	IO176NDB6V1
V8	VCCIB6
V9	VCC
V10	VCC
V11	VCC
V12	VCC
V13	VCC
V14	VCC

FG676	
Pin Number	A3PE1500 Function
V15	VCC
V16	VCC
V17	VCC
V18	VCC
V19	VCCIB3
V20	IO107PDB3V2
V21	IO107NDB3V2
V22	IO103NDB3V2
V23	IO103PDB3V2
V24	VMV3
V25	IO95NDB3V1
V26	IO94PDB3V0
W1	IO179NDB6V1
W2	IO179PDB6V1
W3	IO177NDB6V1
W4	IO177PDB6V1
W5	IO172PDB6V0
W6	IO172NDB6V0
W7	VCC
W8	VCC
W9	VCCIB5
W10	VCCIB5
W11	VCCIB5
W12	VCCIB5
W13	VCCIB5
W14	VCCIB4
W15	VCCIB4
W16	VCCIB4
W17	VCCIB4
W18	VCCIB4
W19	VCC
W20	VCCIB3
W21	GDB0/IO109NDB3V2
W22	GDB1/IO109PDB3V2
W23	IO105NDB3V2
W24	IO105PDB3V2

FG896	
Pin Number	A3PE3000 Function
AG9	IO225NPB5V3
AG10	IO223NPB5V3
AG11	IO221PDB5V3
AG12	IO221NDB5V3
AG13	IO205NPB5V1
AG14	IO199NDB5V0
AG15	IO199PDB5V0
AG16	IO187NDB4V4
AG17	IO187PDB4V4
AG18	IO181NDB4V3
AG19	IO171PPB4V2
AG20	IO165NPB4V1
AG21	IO161NPB4V0
AG22	IO159NDB4V0
AG23	IO159PDB4V0
AG24	IO158PPB4V0
AG25	GDB2/IO155PDB4V0
AG26	GDA2/IO154PPB4V0
AG27	GND
AG28	VJTAG
AG29	VCC
AG30	IO149NDB3V4
AH1	GND
AH2	IO233NPB5V4
AH3	VCC
AH4	GEB2/IO232PPB5V4
AH5	VCCIB5
AH6	IO219NDB5V3
AH7	IO219PDB5V3
AH8	IO227NDB5V4
AH9	IO227PDB5V4
AH10	IO225PPB5V3
AH11	IO223PPB5V3
AH12	IO211NDB5V2
AH13	IO211PDB5V2
AH14	IO205PPB5V1

FG896	
Pin Number	A3PE3000 Function
AH15	IO195NDB5V0
AH16	IO185NDB4V3
AH17	IO185PDB4V3
AH18	IO181PDB4V3
AH19	IO177NDB4V2
AH20	IO171NPB4V2
AH21	IO165PPB4V1
AH22	IO161PPB4V0
AH23	IO157NDB4V0
AH24	IO157PDB4V0
AH25	IO155NDB4V0
AH26	VCCIB4
AH27	TDI
AH28	VCC
AH29	VPUMP
AH30	GND
AJ1	GND
AJ2	GND
AJ3	GEA2/IO233PPB5V4
AJ4	VCC
AJ5	IO217NPB5V2
AJ6	VCC
AJ7	IO215NPB5V2
AJ8	IO213NDB5V2
AJ9	IO213PDB5V2
AJ10	IO209NDB5V1
AJ11	IO209PDB5V1
AJ12	IO203NDB5V1
AJ13	IO203PDB5V1
AJ14	IO197NDB5V0
AJ15	IO195PDB5V0
AJ16	IO183NDB4V3
AJ17	IO183PDB4V3
AJ18	IO179NPB4V3
AJ19	IO177PDB4V2
AJ20	IO173NDB4V2

FG896	
Pin Number	A3PE3000 Function
AJ21	IO173PDB4V2
AJ22	IO163NDB4V1
AJ23	IO163PDB4V1
AJ24	IO167NPB4V1
AJ25	VCC
AJ26	IO156NPB4V0
AJ27	VCC
AJ28	TMS
AJ29	GND
AJ30	GND
AK2	GND
AK3	GND
AK4	IO217PPB5V2
AK5	GND
AK6	IO215PPB5V2
AK7	GND
AK8	IO207NDB5V1
AK9	IO207PDB5V1
AK10	IO201NDB5V0
AK11	IO201PDB5V0
AK12	IO193NDB4V4
AK13	IO193PDB4V4
AK14	IO197PDB5V0
AK15	IO191NDB4V4
AK16	IO191PDB4V4
AK17	IO189NDB4V4
AK18	IO189PDB4V4
AK19	IO179PPB4V3
AK20	IO175NDB4V2
AK21	IO175PDB4V2
AK22	IO169NDB4V1
AK23	IO169PDB4V1
AK24	GND
AK25	IO167PPB4V1
AK26	GND
AK27	GDC2/IO156PPB4V0

FG896	
Pin Number	A3PE3000 Function
AK28	GND
AK29	GND
B1	GND
B2	GND
B3	GAA2/IO309PPB7V4
B4	VCC
B5	IO14PPB0V1
B6	VCC
B7	IO07PPB0V0
B8	IO09PDB0V1
B9	IO15PPB0V1
B10	IO19NDB0V2
B11	IO19PDB0V2
B12	IO29NDB0V3
B13	IO29PDB0V3
B14	IO31PPB0V3
B15	IO37NDB0V4
B16	IO37PDB0V4
B17	IO41PDB1V0
B18	IO51NDB1V1
B19	IO59PDB1V2
B20	IO53PDB1V1
B21	IO53NDB1V1
B22	IO61NDB1V2
B23	IO61PDB1V2
B24	IO69NPB1V3
B25	VCC
B26	GBC0/IO79NPB1V4
B27	VCC
B28	IO64NPB1V2
B29	GND
B30	GND
C1	GND
C2	IO309NPB7V4
C3	VCC
C4	GAA0/IO00NPB0V0

FG896	
Pin Number	A3PE3000 Function
C5	VCCIB0
C6	IO03PDB0V0
C7	IO03NDB0V0
C8	GAB1/IO01PDB0V0
C9	IO05PDB0V0
C10	IO15NPB0V1
C11	IO25NDB0V3
C12	IO25PDB0V3
C13	IO31NPB0V3
C14	IO27NDB0V3
C15	IO39NDB0V4
C16	IO39PDB0V4
C17	IO55PPB1V1
C18	IO51PDB1V1
C19	IO59NDB1V2
C20	IO63NDB1V2
C21	IO63PDB1V2
C22	IO67NDB1V3
C23	IO67PDB1V3
C24	IO75NDB1V4
C25	IO75PDB1V4
C26	VCCIB1
C27	IO64PPB1V2
C28	VCC
C29	GBA1/IO81PPB1V4
C30	GND
D1	IO303PPB7V3
D2	VCC
D3	IO305NPB7V3
D4	GND
D5	GAA1/IO00PPB0V0
D6	GAC1/IO02PDB0V0
D7	IO06NPB0V0
D8	GAB0/IO01NDB0V0
D9	IO05NDB0V0
D10	IO11NDB0V1

FG896	
Pin Number	A3PE3000 Function
D11	IO11PDB0V1
D12	IO23NDB0V2
D13	IO23PDB0V2
D14	IO27PDB0V3
D15	IO40PDB0V4
D16	IO47NDB1V0
D17	IO47PDB1V0
D18	IO55NPB1V1
D19	IO65NDB1V3
D20	IO65PDB1V3
D21	IO71NDB1V3
D22	IO71PDB1V3
D23	IO73NDB1V4
D24	IO73PDB1V4
D25	IO74NDB1V4
D26	GBB0/IO80NPB1V4
D27	GND
D28	GBA0/IO81NPB1V4
D29	VCC
D30	GBA2/IO82PPB2V0
E1	GND
E2	IO303NPB7V3
E3	VCCIB7
E4	IO305PPB7V3
E5	VCC
E6	GAC0/IO02NDB0V0
E7	VCCIB0
E8	IO06PPB0V0
E9	IO24NDB0V2
E10	IO24PDB0V2
E11	IO13NDB0V1
E12	IO13PDB0V1
E13	IO34NDB0V4
E14	IO34PDB0V4
E15	IO40NDB0V4
E16	IO49NDB1V1

FG896		FG896		FG896	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
T11	VCC	U17	GND	V23	IO128NDB3V1
T12	GND	U18	GND	V24	IO132PDB3V2
T13	GND	U19	GND	V25	IO130PPB3V2
T14	GND	U20	VCC	V26	IO126NDB3V1
T15	GND	U21	VCCIB3	V27	IO129NDB3V1
T16	GND	U22	IO120PDB3V0	V28	IO127NDB3V1
T17	GND	U23	IO128PDB3V1	V29	IO125NDB3V1
T18	GND	U24	IO124PDB3V1	V30	IO123PDB3V1
T19	GND	U25	IO124NDB3V1	W1	IO266NDB6V4
T20	VCC	U26	IO126PDB3V1	W2	IO262NDB6V3
T21	VCCIB3	U27	IO129PDB3V1	W3	IO260NDB6V3
T22	IO109NPB2V3	U28	IO127PDB3V1	W4	IO252NDB6V2
T23	IO116NDB3V0	U29	IO125PDB3V1	W5	IO251NDB6V2
T24	IO118NDB3V0	U30	IO121NDB3V0	W6	IO251PDB6V2
T25	IO122NPB3V1	V1	IO268NDB6V4	W7	IO255NDB6V2
T26	GCA1/IO114PPB3V0	V2	IO262PDB6V3	W8	IO249PPB6V1
T27	GCB0/IO113NPB2V3	V3	IO260PDB6V3	W9	IO253PDB6V2
T28	GCA2/IO115PPB3V0	V4	IO252PDB6V2	W10	VCCIB6
T29	VCCPLC	V5	IO257NPB6V2	W11	VCC
T30	IO121PDB3V0	V6	IO261NPB6V3	W12	GND
U1	IO268PDB6V4	V7	IO255PDB6V2	W13	GND
U2	IO264NDB6V3	V8	IO259PDB6V3	W14	GND
U3	IO264PDB6V3	V9	IO259NDB6V3	W15	GND
U4	IO258PDB6V3	V10	VCCIB6	W16	GND
U5	IO258NDB6V3	V11	VCC	W17	GND
U6	IO257PPB6V2	V12	GND	W18	GND
U7	IO261PPB6V3	V13	GND	W19	GND
U8	IO265NDB6V3	V14	GND	W20	VCC
U9	IO263NDB6V3	V15	GND	W21	VCCIB3
U10	VCCIB6	V16	GND	W22	IO134PDB3V2
U11	VCC	V17	GND	W23	IO138PDB3V3
U12	GND	V18	GND	W24	IO132NDB3V2
U13	GND	V19	GND	W25	IO136NPB3V2
U14	GND	V20	VCC	W26	IO130NPB3V2
U15	GND	V21	VCCIB3	W27	IO141PDB3V3
U16	GND	V22	IO120NDB3V0	W28	IO135PDB3V2



Revision	Changes	Page
Revision 11 (August 2012)	Added a Note stating "VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information." to Table 2-1 • Absolute Maximum Ratings and Table 2-2 • Recommended Operating Conditions <sup>1</sup> (SAR 38322).	2-1 3-1 2-1
	The drive strength, IOL, and IOH value for 3.3 V GTL and 2.5 V GTL was changed from 25 mA to 20 mA in the following tables (SAR 31924): "Summary of Maximum and Minimum DC Input and Output Levels" table "Summary of I/O Timing Characteristics—Software Default Settings" table "I/O Output Buffer Maximum Resistances <sup>1</sup> " table "Minimum and Maximum DC Input and Output Levels" table "Minimum and Maximum DC Input and Output Levels" table Also added note stating "Output drive strength is below JEDEC specification" for Tables 2-17 and 2-19. Additionally, the IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected from 51 to 35 (for 3.3 V GTL+) and from 40 to 33 (for 2.5 V GTL+) in table Table 2-13 (SAR 39714).	2-16 2-19 2-20 2-39 2-40
	"Duration of Short Circuit Event Before Failure" table was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 37934).	2-22
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34796): "It uses a 5 V–tolerant input buffer and push-pull output buffer." This change was made in revision 10 and omitted from the change table in error.	2-30
	Revision 11 (continued)	Figure 2-11 was updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34889).
In Table 2-81 VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 37222).		2-52
Figure 2-47 and Figure 2-48 are new (SAR 34848).		2-79
The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions and Packaging" chapter: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38322). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.		3-1