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Understanding Embedded - FPGAs (Field Programmable Gate Array)

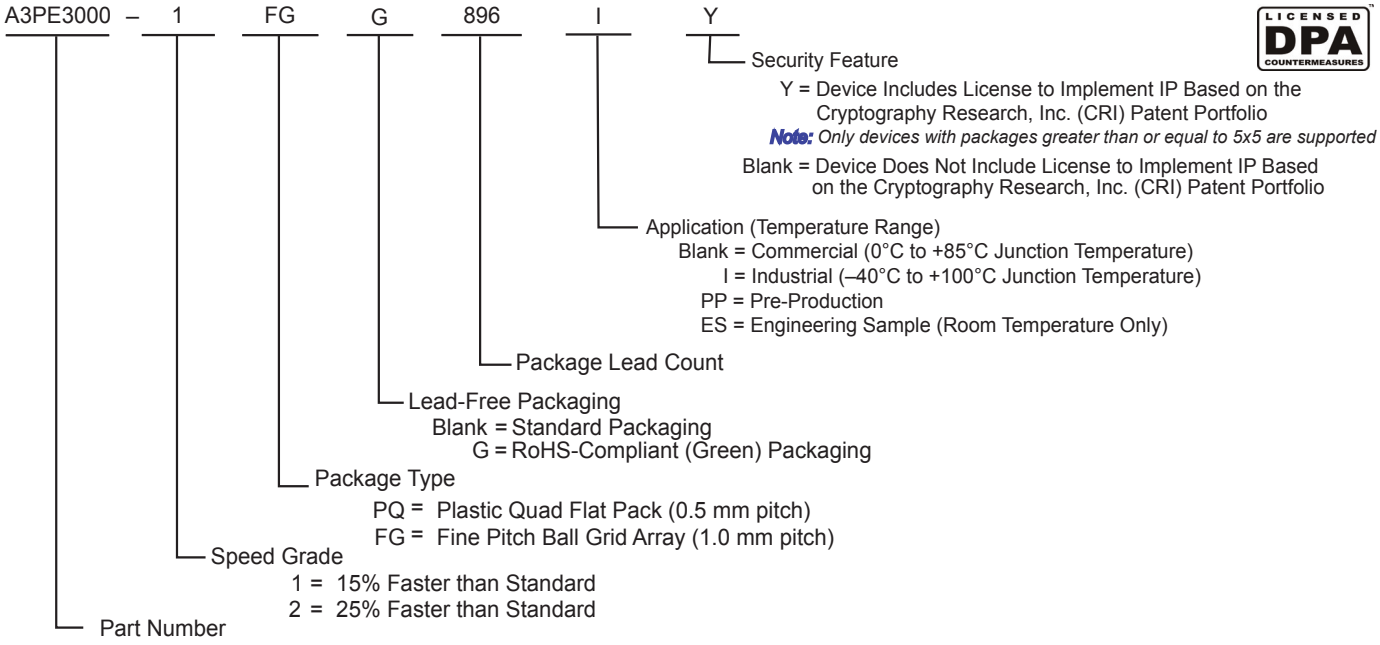
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	165
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3pe600-2fgg256i

ProASIC3E Ordering Information



ProASIC3E Devices

A3PE600 = 600,000 System Gates
A3PE1500 = 1,500,000 System Gates
A3PE3000 = 3,000,000 System Gates

ProASIC3E Devices with Cortex-M1

M1A3PE1500 = 1,500,000 System Gates
M1A3PE3000 = 3,000,000 System Gates

Temperature Grade Offerings

Package	A3PE600	A3PE1500	A3PE3000
Cortex-M1 Devices		**M1A3PE1500**	**M1A3PE3000**
PQ208	C, I	C, I	C, I
FG256	C, I	–	–
FG324	–	–	C, I
FG484	C, I	C, I	C, I
FG676	–	C, I	–
FG896	–	–	C, I

Note: C = Commercial temperature range: 0°C to 70°C ambient temperature
I = Industrial temperature range: –40°C to 85°C ambient temperature

Speed Grade and Temperature Grade Matrix

Temperature Grade	Std.	–1	–2
C [1]	✓	✓	✓
I [2]	✓	✓	✓

Notes:
1. *C = Commercial temperature range: 0°C to 70°C ambient temperature*
2. *I = Industrial temperature range: –40°C to 85°C ambient temperature*

References made to ProASIC3E devices also apply to ARM-enabled ProASIC3E devices. The ARM-enabled part numbers start with M1 (Cortex-M1).

Contact your local Microsemi SoC Products Group representative for device availability: *www.microsemi.com/index.php?option=com_content&id=135&lang=en&view=article*.

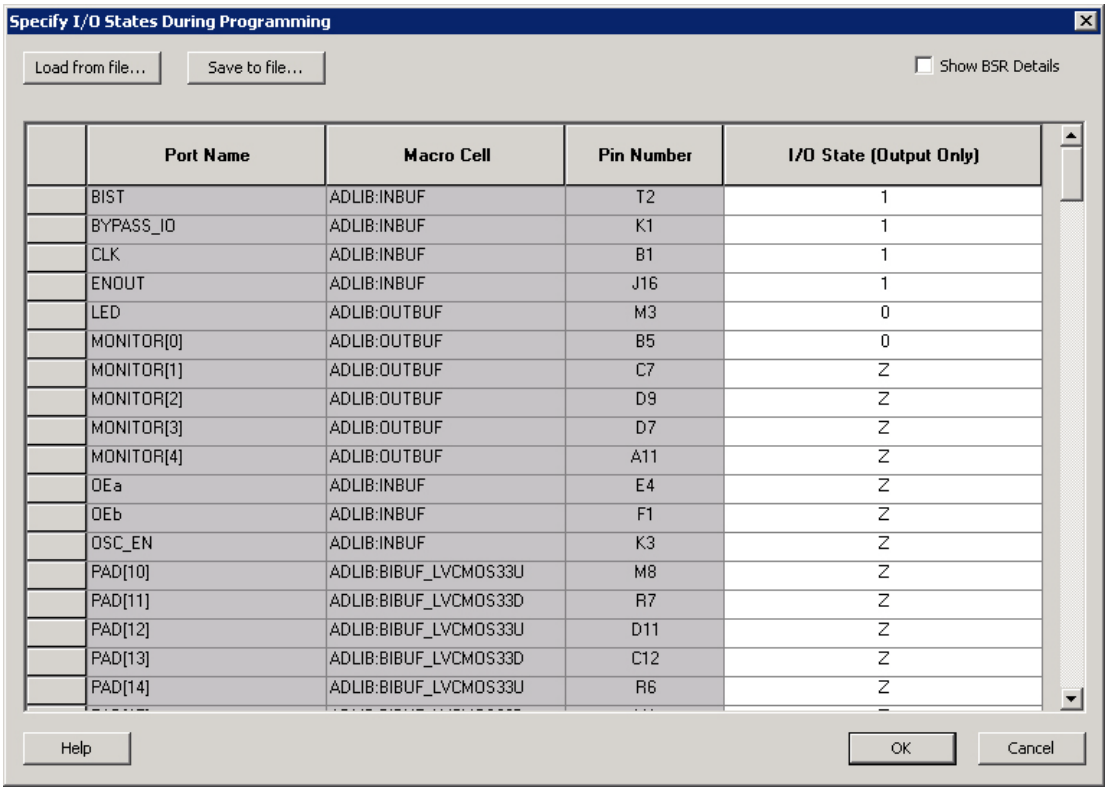


Figure 1-3 • **I/O States During Programming Window**

6. Click OK to return to the FlashPoint – Programming File Generator window.

   I/O States during programming are saved to the ADB and resulting programming files after completing programming file generation.

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-15 • Summary of AC Measuring Points

Standard	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_REF)	Measuring Trip Point (Vtrip)
3.3 V LVTTL / 3.3 V LVCMOS	–	–	1.4 V
3.3 V LVCMOS Wide Range	–	–	1.4 V
2.5 V LVCMOS	–	–	1.2 V
1.8 V LVCMOS	–	–	0.90 V
1.5 V LVCMOS	–	–	0.75 V
3.3 V PCI	–	–	0.285 * VCCI (RR) 0.615 * VCCI (FF))
3.3 V PCI-X	–	–	0.285 * VCCI (RR) 0.615 * VCCI (FF)
3.3 V GTL	0.8 V	1.2 V	VREF
2.5 V GTL	0.8 V	1.2 V	VREF
3.3 V GTL+	1.0 V	1.5 V	VREF
2.5 V GTL+	1.0 V	1.5 V	VREF
HSTL (I)	0.75 V	0.75 V	VREF
HSTL (II)	0.75 V	0.75 V	VREF
SSTL2 (I)	1.25 V	1.25 V	VREF
SSTL2 (II)	1.25 V	1.25 V	VREF
SSTL3 (I)	1.5 V	1.485 V	VREF
SSTL3 (II)	1.5 V	1.485 V	VREF
LVDS	–	–	Cross point
LVPECL	–	–	Cross point

Table 2-16 • I/O AC Parameter Definitions

Parameter	Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer with Schmitt trigger disabled
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{PYS}	Pad to Data delay through the Input Buffer with Schmitt trigger enabled
t_{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t_{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

Timing Characteristics

Table 2-35 • 2.5 V LVCMOS High Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	8.82	0.04	1.51	1.66	0.43	8.13	8.82	2.72	2.29	10.37	11.05	ns
	–1	0.56	7.50	0.04	1.29	1.41	0.36	6.92	7.50	2.31	1.95	8.82	9.40	ns
	–2	0.49	6.58	0.03	1.13	1.24	0.32	6.07	6.58	2.03	1.71	7.74	8.25	ns
8 mA	Std.	0.66	5.27	0.04	1.51	1.66	0.43	5.27	5.27	3.10	3.03	7.50	7.51	ns
	–1	0.56	4.48	0.04	1.29	1.41	0.36	4.48	4.48	2.64	2.58	6.38	6.38	ns
	–2	0.49	3.94	0.03	1.13	1.24	0.32	3.93	3.94	2.32	2.26	5.60	5.61	ns
12 mA	Std.	0.66	3.74	0.04	1.51	1.66	0.43	3.81	3.49	3.37	3.49	6.05	5.73	ns
	–1	0.56	3.18	0.04	1.29	1.41	0.36	3.24	2.97	2.86	2.97	5.15	4.87	ns
	–2	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28	ns
16 mA	Std.	0.66	3.53	0.04	1.51	1.66	0.43	3.59	3.12	3.42	3.62	5.83	5.35	ns
	–1	0.56	3.00	0.04	1.29	1.41	0.36	3.06	2.65	2.91	3.08	4.96	4.55	ns
	–2	0.49	2.63	0.03	1.13	1.24	0.32	2.68	2.33	2.56	2.71	4.35	4.00	ns
24 mA	Std.	0.66	3.26	0.04	1.51	1.66	0.43	3.32	2.48	3.49	4.11	5.56	4.72	ns
	–1	0.56	2.77	0.04	1.29	1.41	0.36	2.83	2.11	2.97	3.49	4.73	4.01	ns
	–2	0.49	2.44	0.03	1.13	1.24	0.32	2.48	1.85	2.61	3.07	4.15	3.52	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

Table 2-40 • 1.8 V LVCMOS Low Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	15.84	0.04	1.45	1.91	0.43	15.65	15.84	2.78	1.58	17.89	18.07	ns
	–1	0.56	13.47	0.04	1.23	1.62	0.36	13.31	13.47	2.37	1.35	15.22	15.37	ns
	–2	0.49	11.83	0.03	1.08	1.42	0.32	11.69	11.83	2.08	1.18	13.36	13.50	ns
4 mA	Std.	0.66	11.39	0.04	1.45	1.91	0.43	11.60	10.76	3.26	2.77	13.84	12.99	ns
	–1	0.56	9.69	0.04	1.23	1.62	0.36	9.87	9.15	2.77	2.36	11.77	11.05	ns
	–2	0.49	8.51	0.03	1.08	1.42	0.32	8.66	8.03	2.43	2.07	10.33	9.70	ns
6 mA	Std.	0.66	8.97	0.04	1.45	1.91	0.43	9.14	8.10	3.57	3.36	11.37	10.33	ns
	–1	0.56	7.63	0.04	1.23	1.62	0.36	7.77	6.89	3.04	2.86	9.67	8.79	ns
	–2	0.49	6.70	0.03	1.08	1.42	0.32	6.82	6.05	2.66	2.51	8.49	7.72	ns
8 mA	Std.	0.66	8.35	0.04	1.45	1.91	0.43	8.50	7.59	3.64	3.52	10.74	9.82	ns
	–1	0.56	7.10	0.04	1.23	1.62	0.36	7.23	6.45	3.10	3.00	9.14	8.35	ns
	–2	0.49	6.24	0.03	1.08	1.42	0.32	6.35	5.66	2.72	2.63	8.02	7.33	ns
12 mA	Std.	0.66	7.94	0.04	1.45	1.91	0.43	8.09	7.56	3.74	4.11	10.32	9.80	ns
	–1	0.56	6.75	0.04	1.23	1.62	0.36	6.88	6.43	3.18	3.49	8.78	8.33	ns
	–2	0.49	5.93	0.03	1.08	1.42	0.32	6.04	5.65	2.79	3.07	7.71	7.32	ns
16 mA	Std.	0.66	7.94	0.04	1.45	1.91	0.43	8.09	7.56	3.74	4.11	10.32	9.80	ns
	–1	0.56	6.75	0.04	1.23	1.62	0.36	6.88	6.43	3.18	3.49	8.78	8.33	ns
	–2	0.49	5.93	0.03	1.08	1.42	0.32	6.04	5.65	2.79	3.07	7.71	7.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-24. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

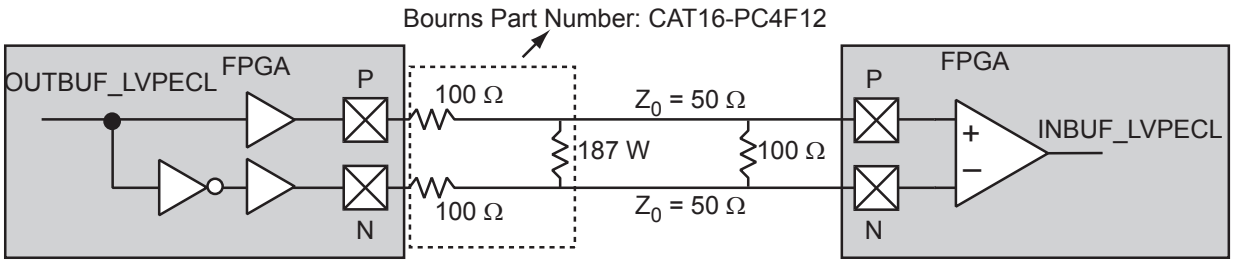


Figure 2-24 • **LVPECL Circuit Diagram and Board-Level Implementation**

Table 2-81 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

Table 2-82 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)
1.64	1.94	Cross point	–

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-83 • **LVPECL**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.66	1.83	0.04	1.63	ns
–1	0.56	1.55	0.04	1.39	ns
–2	0.49	1.36	0.03	1.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

***Table 2-84* • Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

*Note: *See Figure 2-25 on page 2-53 for more information.*

Output Register

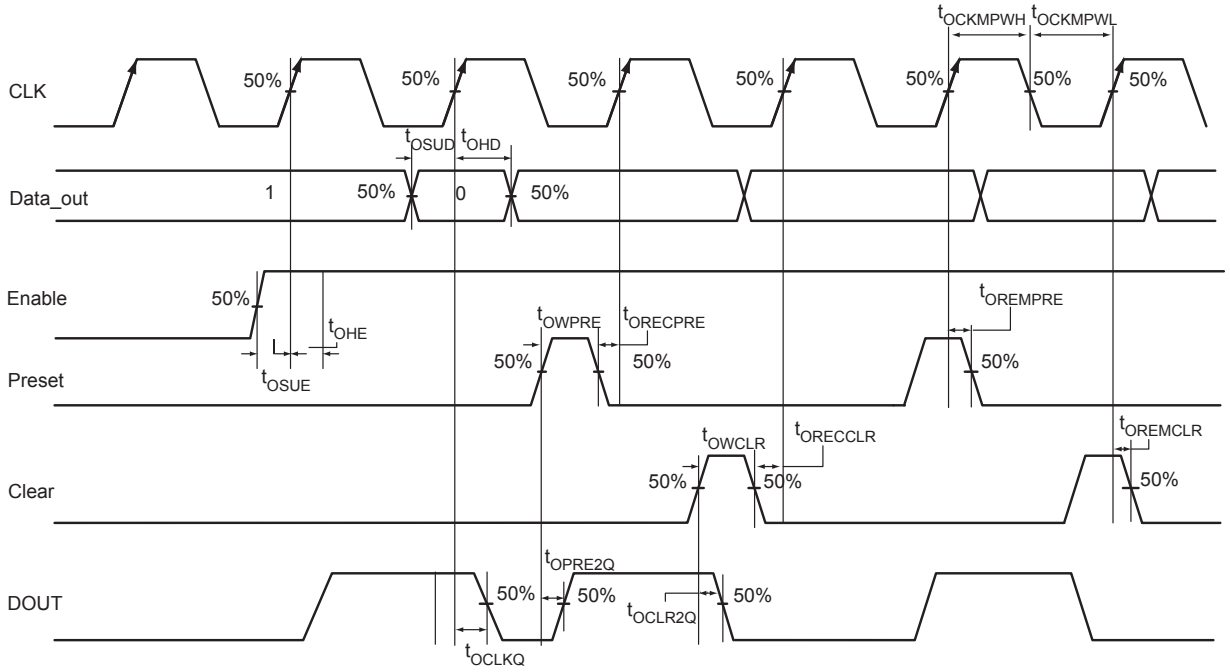


Figure 2-28 • **Output Register Timing Diagram**

Timing Characteristics

Table 2-87 • **Output Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.59	0.67	0.79	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.31	0.36	0.42	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.44	0.50	0.59	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.80	0.91	1.07	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.80	0.91	1.07	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.41	0.48	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Timing Characteristics

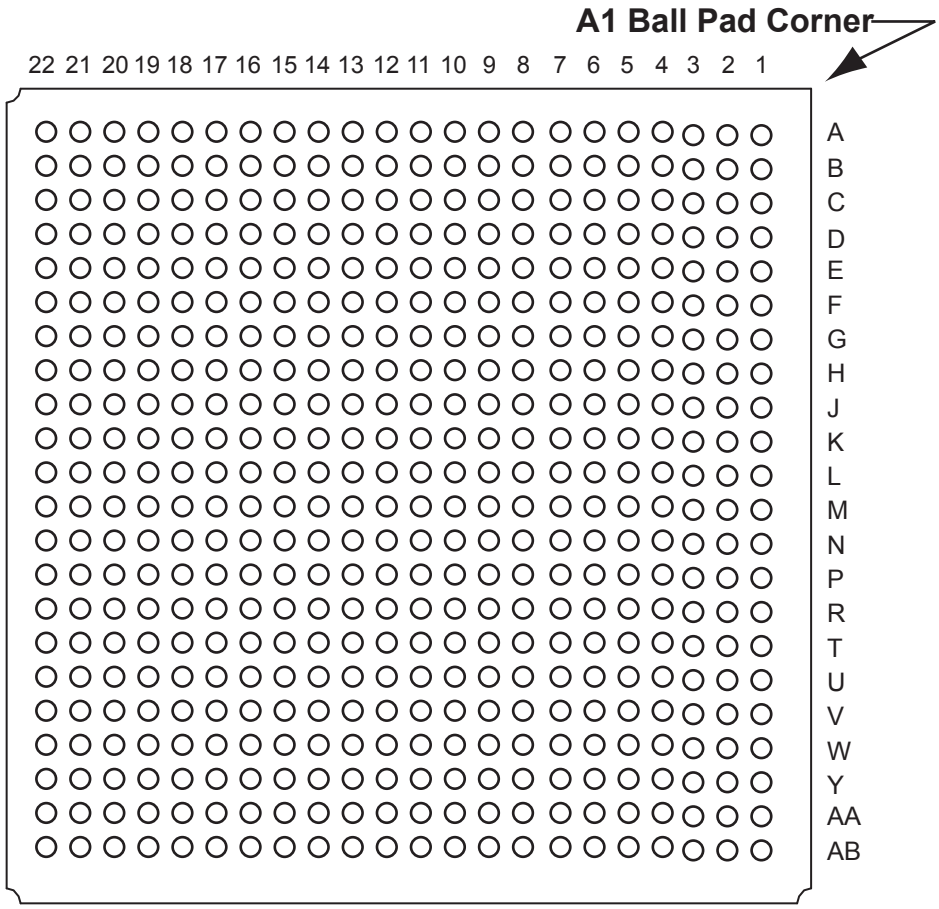
Table 2-99 • RAM4K9
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.28	0.33	ns
t_{AH}	Address hold time	0.00	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.14	0.16	0.19	ns
t_{ENH}	REN, WEN hold time	0.10	0.11	0.13	ns
t_{BKS}	BLK setup time	0.23	0.27	0.31	ns
t_{BKH}	BLK hold time	0.02	0.02	0.02	ns
t_{DS}	Input data (DIN) setup time	0.18	0.21	0.25	ns
t_{DH}	Input data (DIN) hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	1.79	2.03	2.39	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.36	2.68	3.15	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	0.89	1.02	1.20	ns
t_{C2CWWL} [1]	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Closing Edge	0.33	0.28	0.25	ns
t_{C2CWWH} [1]	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge	0.30	0.26	0.23	ns
t_{C2CRWH} [1]	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.45	0.38	0.34	ns
t_{C2CWRH} [1]	Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge	0.49	0.42	0.37	ns
t_{RSTBQ}	RESET Low to data out Low on DO (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on DO (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.21	0.24	0.29	ns
t_{CYC}	Clock cycle time	3.23	3.68	4.32	ns
F_{MAX}	Maximum frequency	310	272	231	MHz

Notes:

1. *For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

FG484



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/products/fpga-soc/solutions*.

FG484	
Pin Number	A3PE600 Function
A1	GND
A2	GND
A3	VCCIB0
A4	IO06NDB0V1
A5	IO06PDB0V1
A6	IO08NDB0V1
A7	IO08PDB0V1
A8	IO11PDB0V1
A9	IO17PDB0V2
A10	IO18NDB0V2
A11	IO18PDB0V2
A12	IO22PDB1V0
A13	IO26PDB1V0
A14	IO29NDB1V1
A15	IO29PDB1V1
A16	IO31NDB1V1
A17	IO31PDB1V1
A18	IO32NDB1V1
A19	NC
A20	VCCIB1
A21	GND
A22	GND
AA1	GND
AA2	VCCIB6
AA3	NC
AA4	IO98PDB5V2
AA5	IO96NDB5V2
AA6	IO96PDB5V2
AA7	IO86NDB5V0
AA8	IO86PDB5V0
AA9	IO85PDB5V0
AA10	IO85NDB5V0
AA11	IO78PPB4V1
AA12	IO79NDB4V1
AA13	IO79PDB4V1
AA14	NC

FG484	
Pin Number	A3PE600 Function
AA15	NC
AA16	IO71NDB4V0
AA17	IO71PDB4V0
AA18	NC
AA19	NC
AA20	NC
AA21	VCCIB3
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB5
AB4	IO97NDB5V2
AB5	IO97PDB5V2
AB6	IO93NDB5V1
AB7	IO93PDB5V1
AB8	IO87NDB5V0
AB9	IO87PDB5V0
AB10	NC
AB11	NC
AB12	IO75NDB4V1
AB13	IO75PDB4V1
AB14	IO72NDB4V0
AB15	IO72PDB4V0
AB16	IO73NDB4V0
AB17	IO73PDB4V0
AB18	NC
AB19	NC
AB20	VCCIB4
AB21	GND
AB22	GND
B1	GND
B2	VCCIB7
B3	NC
B4	IO03NDB0V0
B5	IO03PDB0V0
B6	IO07NDB0V1

FG484	
Pin Number	A3PE600 Function
B7	IO07PDB0V1
B8	IO11NDB0V1
B9	IO17NDB0V2
B10	IO14PDB0V2
B11	IO19PDB0V2
B12	IO22NDB1V0
B13	IO26NDB1V0
B14	NC
B15	NC
B16	IO30NDB1V1
B17	IO30PDB1V1
B18	IO32PDB1V1
B19	NC
B20	NC
B21	VCCIB2
B22	GND
C1	VCCIB7
C2	NC
C3	NC
C4	NC
C5	GND
C6	IO04NDB0V0
C7	IO04PDB0V0
C8	VCC
C9	VCC
C10	IO14NDB0V2
C11	IO19NDB0V2
C12	NC
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC

FG484	
Pin Number	**A3PE1500 Function**
H19	IO67PDB2V1
H20	VCC
H21	VMV2
H22	IO74PSB2V2
J1	IO212NDB7V2
J2	IO212PDB7V2
J3	VMV7
J4	IO206PDB7V1
J5	IO204PDB7V1
J6	IO210PDB7V2
J7	IO215NDB7V3
J8	VCCIB7
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB2
J16	IO60NDB2V0
J17	IO65NDB2V1
J18	IO65PDB2V1
J19	IO75PPB2V2
J20	GNDQ
J21	IO77PDB2V2
J22	IO79PDB2V3
K1	IO200NDB7V1
K2	IO200PDB7V1
K3	GNDQ
K4	IO206NDB7V1
K5	IO204NDB7V1
K6	IO210NDB7V2
K7	GFC1/IO192PPB7V0
K8	VCCIB7
K9	VCC
K10	GND

FG484	
Pin Number	**A3PE1500 Function**
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB2
K16	GCC1/IO85PPB2V3
K17	IO73NDB2V2
K18	IO73PDB2V2
K19	IO81NPB2V3
K20	IO75NPB2V2
K21	IO77NDB2V2
K22	IO79NDB2V3
L1	NC
L2	IO196PDB7V0
L3	IO196NDB7V0
L4	GFB0/IO191NPB7V0
L5	GFA0/IO190NDB6V2
L6	GFB1/IO191PPB7V0
L7	VCOMPLF
L8	GFC0/IO192NPB7V0
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO85NPB2V3
L16	GCB1/IO86PPB2V3
L17	GCA0/IO87NPB3V0
L18	VCOMPLC
L19	GCB0/IO86NPB2V3
L20	IO81PPB2V3
L21	IO83NDB2V3
L22	IO83PDB2V3
M1	GNDQ
M2	IO185NPB6V2

FG484	
Pin Number	**A3PE1500 Function**
M3	IO189NDB6V2
M4	GFA2/IO189PDB6V2
M5	GFA1/IO190PDB6V2
M6	VCCPLF
M7	IO188NDB6V2
M8	GFB2/IO188PDB6V2
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO89PPB3V0
M16	GCA1/IO87PPB3V0
M17	GCC2/IO90PPB3V0
M18	VCCPLC
M19	GCA2/IO88PDB3V0
M20	IO88NDB3V0
M21	IO93PDB3V0
M22	NC
N1	IO185PPB6V2
N2	IO183NDB6V2
N3	VMV6
N4	GFC2/IO187PPB6V2
N5	IO184PPB6V2
N6	IO186PDB6V2
N7	IO186NDB6V2
N8	VCCIB6
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB3
N16	IO89NPB3V0

FG484	
Pin Number	A3PE1500 Function
N17	IO91NPB3V0
N18	IO90NPB3V0
N19	IO91PPB3V0
N20	GNDQ
N21	IO93NDB3V0
N22	IO95PDB3V1
P1	NC
P2	IO183PDB6V2
P3	IO187NPB6V2
P4	IO184NPB6V2
P5	IO176PPB6V1
P6	IO182PDB6V1
P7	IO182NDB6V1
P8	VCCIB6
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB3
P16	GDB0/IO109NPB3V2
P17	IO97NDB3V1
P18	IO97PDB3V1
P19	IO99PDB3V1
P20	VMV3
P21	IO98PDB3V1
P22	IO95NDB3V1
R1	NC
R2	IO177PDB6V1
R3	VCC
R4	IO176NPB6V1
R5	IO174NDB6V0
R6	IO174PDB6V0
R7	GEC0/IO169NPB6V0
R8	VMV5

FG484	
Pin Number	A3PE1500 Function
R9	VCCIB5
R10	VCCIB5
R11	IO135NDB5V0
R12	IO135PDB5V0
R13	VCCIB4
R14	VCCIB4
R15	VMV3
R16	VCCPLD
R17	GDB1/IO109PPB3V2
R18	GDC1/IO108PDB3V2
R19	IO99NDB3V1
R20	VCC
R21	IO98NDB3V1
R22	IO101PDB3V1
T1	NC
T2	IO177NDB6V1
T3	NC
T4	IO171PDB6V0
T5	IO171NDB6V0
T6	GEC1/IO169PPB6V0
T7	VCOMPLE
T8	GNDQ
T9	GEA2/IO166PPB5V3
T10	IO145NDB5V1
T11	IO141NDB5V0
T12	IO139NDB5V0
T13	IO119NDB4V1
T14	IO119PDB4V1
T15	GNDQ
T16	VCOMPLD
T17	VJTAG
T18	GDC0/IO108NDB3V2
T19	GDA1/IO110PDB3V2
T20	NC
T21	IO103PDB3V2
T22	IO101NDB3V1

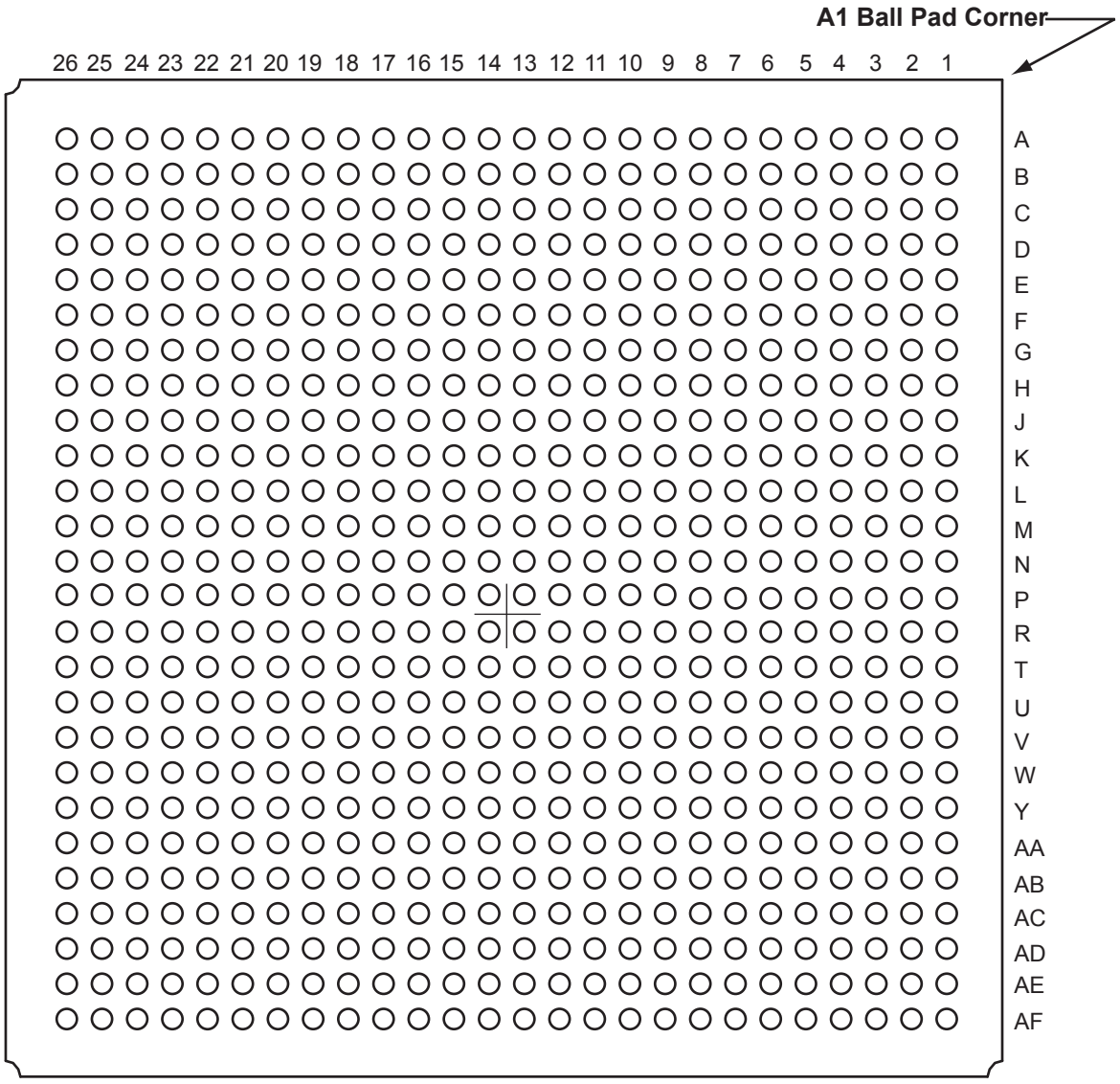
FG484	
Pin Number	A3PE1500 Function
U1	IO175PPB6V1
U2	IO173PDB6V0
U3	IO173NDB6V0
U4	GEB1/IO168PDB6V0
U5	GEB0/IO168NDB6V0
U6	VMV6
U7	VCCPLE
U8	IO166NPB5V3
U9	IO157PPB5V2
U10	IO145PDB5V1
U11	IO141PDB5V0
U12	IO139PDB5V0
U13	IO121NDB4V1
U14	IO121PDB4V1
U15	VMV4
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO110NDB3V2
U20	NC
U21	IO103NDB3V2
U22	IO105PDB3V2
V1	NC
V2	IO175NPB6V1
V3	GND
V4	GEA1/IO167PDB6V0
V5	GEA0/IO167NDB6V0
V6	GNDQ
V7	GEC2/IO164PDB5V3
V8	IO157NPB5V2
V9	IO151NDB5V2
V10	IO151PDB5V2
V11	IO137NDB5V0
V12	IO137PDB5V0
V13	IO123NDB4V1
V14	IO123PDB4V1

FG484	
Pin Number	A3PE3000 Function
A1	GND
A2	GND
A3	VCCIB0
A4	IO10NDB0V1
A5	IO10PDB0V1
A6	IO16NDB0V1
A7	IO16PDB0V1
A8	IO18PDB0V2
A9	IO24PDB0V2
A10	IO28NDB0V3
A11	IO28PDB0V3
A12	IO46PDB1V0
A13	IO54PDB1V1
A14	IO56NDB1V1
A15	IO56PDB1V1
A16	IO64NDB1V2
A17	IO64PDB1V2
A18	IO72NDB1V3
A19	IO74NDB1V4
A20	VCCIB1
A21	GND
A22	GND
AA1	GND
AA2	VCCIB6
AA3	IO228PDB5V4
AA4	IO224PDB5V3
AA5	IO218NDB5V3
AA6	IO218PDB5V3
AA7	IO212NDB5V2
AA8	IO212PDB5V2
AA9	IO198PDB5V0
AA10	IO198NDB5V0
AA11	IO188PPB4V4
AA12	IO180NDB4V3
AA13	IO180PDB4V3
AA14	IO170NDB4V2

FG484	
Pin Number	A3PE3000 Function
AA15	IO170PDB4V2
AA16	IO166NDB4V1
AA17	IO166PDB4V1
AA18	IO160NDB4V0
AA19	IO160PDB4V0
AA20	IO158NPB4V0
AA21	VCCIB3
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB5
AB4	IO216NDB5V2
AB5	IO216PDB5V2
AB6	IO210NDB5V2
AB7	IO210PDB5V2
AB8	IO208NDB5V1
AB9	IO208PDB5V1
AB10	IO197NDB5V0
AB11	IO197PDB5V0
AB12	IO174NDB4V2
AB13	IO174PDB4V2
AB14	IO172NDB4V2
AB15	IO172PDB4V2
AB16	IO168NDB4V1
AB17	IO168PDB4V1
AB18	IO162NDB4V1
AB19	IO162PDB4V1
AB20	VCCIB4
AB21	GND
AB22	GND
B1	GND
B2	VCCIB7
B3	IO06PPB0V0
B4	IO08NDB0V0
B5	IO08PDB0V0
B6	IO14NDB0V1

FG484	
Pin Number	A3PE3000 Function
B7	IO14PDB0V1
B8	IO18NDB0V2
B9	IO24NDB0V2
B10	IO34PDB0V4
B11	IO40PDB0V4
B12	IO46NDB1V0
B13	IO54NDB1V1
B14	IO62NDB1V2
B15	IO62PDB1V2
B16	IO68NDB1V3
B17	IO68PDB1V3
B18	IO72PDB1V3
B19	IO74PDB1V4
B20	IO76NPB1V4
B21	VCCIB2
B22	GND
C1	VCCIB7
C2	IO303PDB7V3
C3	IO305PDB7V3
C4	IO06NPB0V0
C5	GND
C6	IO12NDB0V1
C7	IO12PDB0V1
C8	VCC
C9	VCC
C10	IO34NDB0V4
C11	IO40NDB0V4
C12	IO48NDB1V0
C13	IO48PDB1V0
C14	VCC
C15	VCC
C16	IO70NDB1V3
C17	IO70PDB1V3
C18	GND
C19	IO76PPB1V4
C20	IO88NDB2V0

FG676

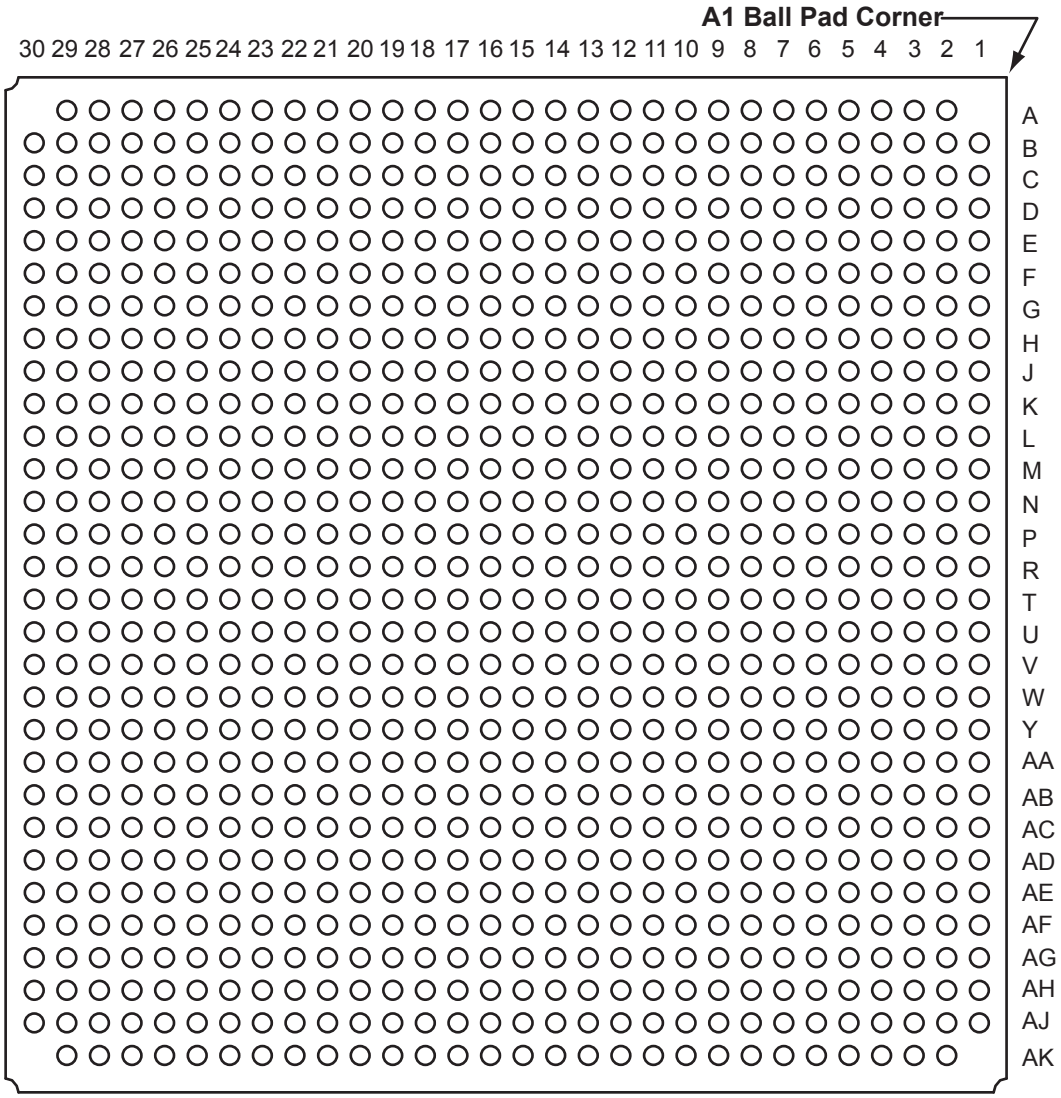


Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/products/fpga-soc/solutions*.

FG896



Note: This is the bottom view of the package.

Note

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5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the ProASIC3E datasheet.

Revision	Changes	Page
Revision 15 (June 2015)	Updated "ProASIC3E Ordering Information". Interchanged the positions of Y- Security Feature and I- Application (Temperature Range) (SAR 67296). Added Note "Only devices with package size greater than or equal to 5x5 are supported". Updated Commercial and Industrial Junction Temperatures (SAR 67588).	*1-III*
	Added the A3PE3000 package to Table 2-5 (SARs 52320 and 58737).	*2-5*
	Updated "VCCIBx I/O Supply Voltage" (SAR 43323).	*3-1*
Revision 14 (May 2014)	Added 2 mA and 6 mA I/O short currents values in *"I/O Short Currents IOSH/IOSL"* (SAR 56295). Added 2 mA and 6 mA minimum and maximum DC input and output levels in "Minimum and Maximum DC Input and Output Levels"(SAR 56295). Added 3.3 V LVTTL / 3.3 V LVCMOS High Slew Commercial-Case Conditions for 2 mA and 6 mA in "3.3 V LVTTL / 3.3 V LVCMOS High Slew" (SAR 56295). Added 3.3 V LVTTL / 3.3 V LVCMOS Low Slew Commercial-Case Conditions for 2 mA and 6 mA in "3.3 V LVTTL / 3.3 V LVCMOS Low Slew" (SAR 56295).	*2-22* *2-24* *2-25* *2-25*
Revision 13 (January 2013)	In the "Features and Benefits" section, updated the Clock Conditioning Circuit (CCC) and PLL Wide Input Frequency Range from '1.5 MHz to 200 MHz' to '1.5MHz to 350 MHz' based on Table 2-98 (SAR 22196).	1-I
	The "ProASIC3E Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43220).	1-III
	Added a note to "Recommended Operating Conditions [1]" table (SAR 42716): The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.	2-2
	The note in "ProASIC3E CCC/PLL Specification" table referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42571).	2-70
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40285). Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 12 (September 2012)	The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data.	1-1

Revision	Changes	Page
v2.0 (continued)	Table 3-6 • Temperature and Voltage Derating Factors for Timing Delays was updated.	3-5
	Table 3-5 • Package Thermal Resistivities was updated.	3-5
	Table 3-10 • Different Components Contributing to the Dynamic Power Consumption in ProASIC3E Devices was updated.	3-8
	t_{WRO} and t_{CCKH} were added to Table 3-94 • RAM4K9 and Table 3-95 • RAM512X18.	3-74 to 3-74
	The note in Table 3-24 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was updated.	3-23
	Figure 3-43 • Write Access After Write onto Same Address, Figure 3-44 • Read Access After Write onto Same Address, and Figure 3-45 • Write Access After Read onto Same Address are new.	3-71 to 3-73
	Figure 3-53 • Timing Diagram was updated.	3-80
	Notes were added to the package diagrams identifying if they were top or bottom view.	N/A
	The A3PE1500 "208-Pin PQFP" table is new.	4-4
	The A3PE1500 "484-Pin FBGA" table is new.	4-18
	The A3PE1500 "A3PE1500 Function" table is new.	4-24
Advance v0.6 (January 2007)	In the "Packaging Tables" table, the number of I/Os for the A3PE1500 was changed for the FG484 and FG676 packages.	ii
Advance v0.5 (April 2006)	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	Figure 2-8 • Very-Long-Line Resources was updated.	2-8
	The footnotes in Figure 2-27 • CCC/PLL Macro were updated.	2-28
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options.	2-24
	The "SRAM and FIFO" section was updated.	2-21
	The "RESET" section was updated.	2-25
	The "WCLK and RCLK" section was updated.	2-25
	The "RESET" section was updated.	2-25
	The "RESET" section was updated.	2-27
	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	Figure 2-8 • Very-Long-Line Resources was updated.	2-8
	The footnotes in Figure 2-27 • CCC/PLL Macro were updated.	2-28
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options.	2-24
	The "SRAM and FIFO" section was updated.	2-21
	The "RESET" section was updated.	2-25
	The "WCLK and RCLK" section was updated.	2-25

Revision	Changes	Page
Advance v0.5 (continued)	The "I/O User Input/Output" pin description was updated to include information on what happens when the pin is unused.	2-50
	The "JTAG Pins" section was updated to include information on what happens when the pin is unused.	2-51
	The "Programming" section was updated to include information concerning serialization.	2-53
	The "JTAG 1532" section was updated to include SAMPLE/PRELOAD information.	2-54
	The "DC and Switching Characteristics" chapter was updated with new information.	Starting on page 3-1
	Table 3-6 was updated.	3-5
	In Table 3-10, PAC4 was updated.	3-8
	Table 3-19 was updated.	3-20
	The note in Table 3-24 was updated.	3-23
	All Timing Characteristics tables were updated from LVTTL to Register Delays	3-26 to 3-64
	The Timing Characteristics for RAM4K9, RAM512X18, and FIFO were updated.	3-74 to 3-79
	F_{TCKMAX} was updated in Table 3-98.	3-80
Advance v0.4 (October 2005)	The "Packaging Tables" table was updated.	ii
Advance v0.3	Figure 2-11 was updated.	2-9
	The "Clock Resources (VersaNets)" section was updated.	2-9
	The "VersaNet Global Networks and Spine Access" section was updated.	2-9
	The "PLL Macro" section was updated.	2-15
	Figure 2-27 was updated.	2-28
	Figure 2-20 was updated.	2-19
	Table 2-5 was updated.	2-25
	Table 2-6 was updated.	2-25
	The "FIFO Flag Usage Considerations" section was updated.	2-27
	Table 2-33 was updated.	2-51
	Figure 2-24 was updated.	2-31
	The "Cold-Sparing Support" section is new.	2-34
	Table 2-45 was updated.	2-64
	Table 2-48 was updated.	2-81
	Pin descriptions in the "JTAG Pins" section were updated.	2-51
	The "Pin Descriptions" section was updated.	2-50
	Table 3-7 was updated.	3-6