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Understanding Embedded - FPGAs (Field Programmable Gate Array)

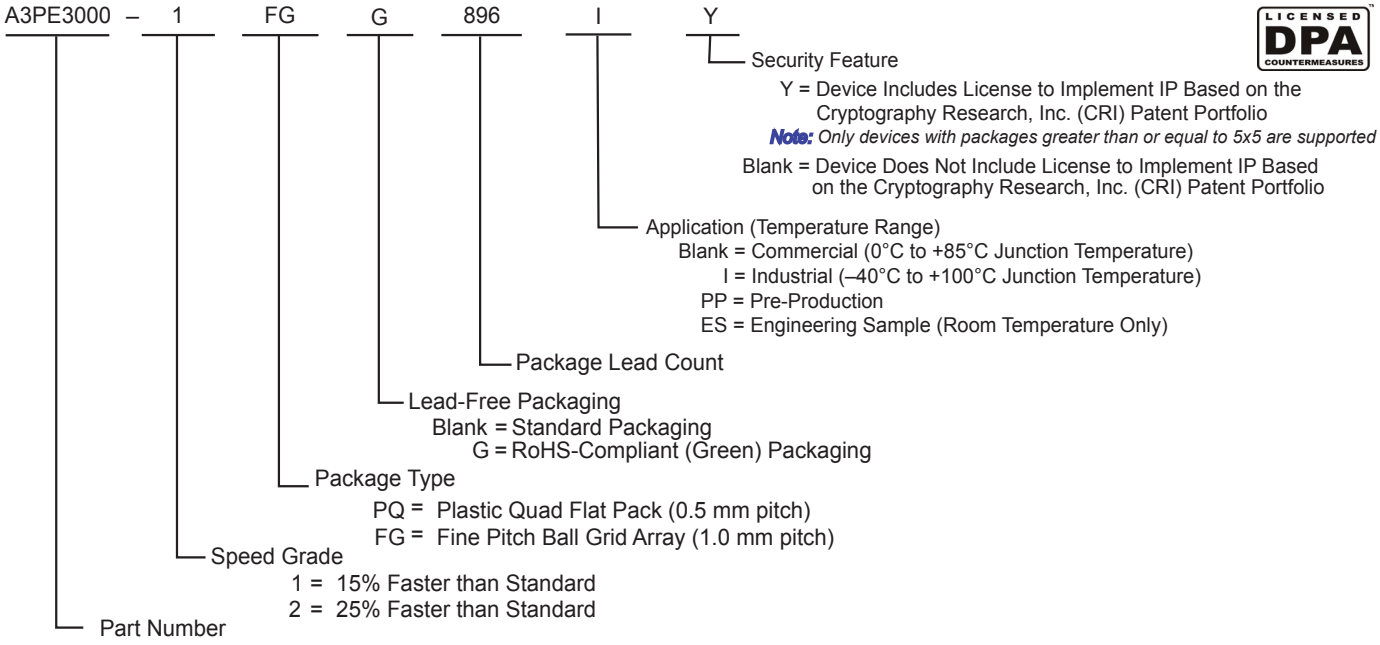
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	270
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3pe600-2fgg484

ProASIC3E Ordering Information



ProASIC3E Devices

A3PE600 = 600,000 System Gates
A3PE1500 = 1,500,000 System Gates
A3PE3000 = 3,000,000 System Gates

ProASIC3E Devices with Cortex-M1

M1A3PE1500 = 1,500,000 System Gates
M1A3PE3000 = 3,000,000 System Gates

Advanced Architecture

The proprietary ProASIC3E architecture provides granularity comparable to standard-cell ASICs. The ProASIC3E device consists of five distinct and programmable architectural features (Figure 1-1 on page 3):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- Pro I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the ProASIC3E core tile as either a three-input lookup table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC family of third-generation architecture Flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

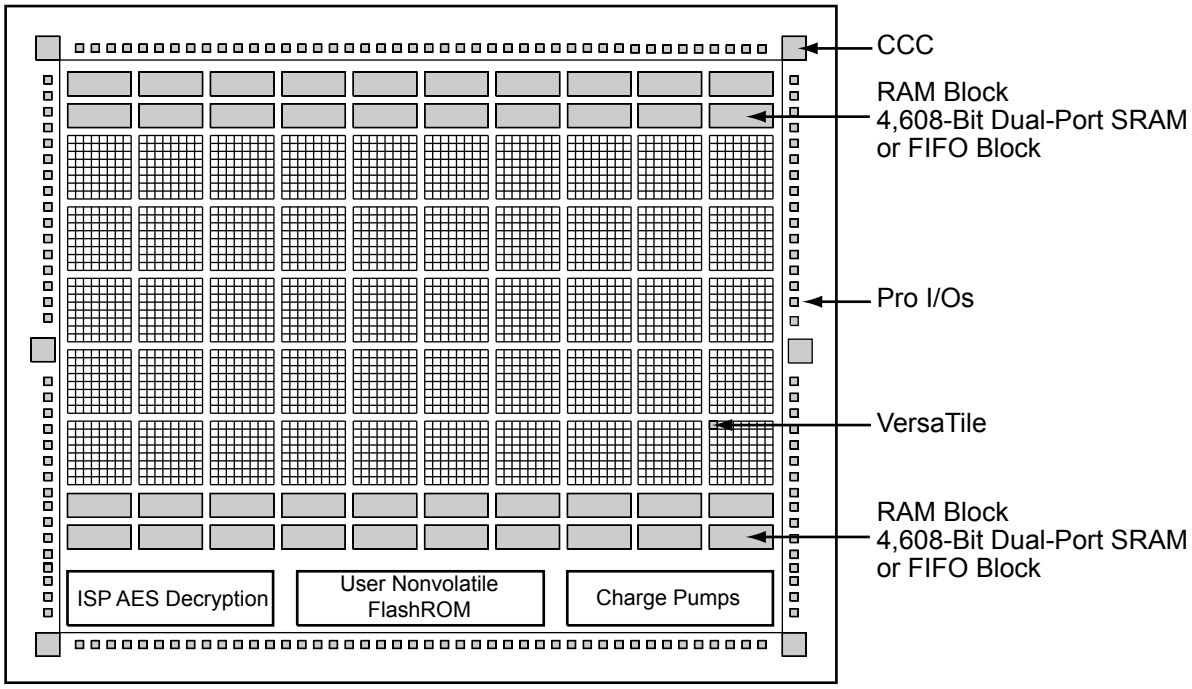


Figure 1-1 • **ProASIC3E Device Architecture Overview**

Table 2-4 • Overshoot and Undershoot Limits [1]

VCCI and VMV	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
3. *This table does not provide PCI overshoot/undershoot limits.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC®3E device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4.

There are five regions to consider during power-up.

ProASIC3E I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 on page 2-4).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

Table 2-8 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings (continued)

	VMV (V)	Static Power PDC2 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
HSTL (I)	1.5	0.17	2.03
HSTL (II)	1.5	0.17	2.03
SSTL2 (I)	2.5	1.38	4.48
SSTL2 (II)	2.5	1.38	4.48
SSTL3 (I)	3.3	3.21	9.26
SSTL3 (II)	3.3	3.21	9.26
Differential			
LVDS/B-LVDS/M-LVDS	2.5	2.26	1.50
LVPECL	3.3	5.71	2.17

Notes:

1. *PDC2 is the static power (where applicable) measured on VMV.*
2. *PAC9 is the total dynamic power measured on VCC and VMV.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.*

Table 2-9 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1]

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL/LVCMOS	35	3.3	–	474.70
3.3 V LVTTL/LVCMOS Wide Range[4]	35	3.3	–	474.70
2.5 V LVCMOS	35	2.5	–	270.73
1.8 V LVCMOS	35	1.8	–	151.78
1.5 V LVCMOS (JESD8-11)	35	1.5	–	104.55
3.3 V PCI	10	3.3	–	204.61
3.3 V PCI-X	10	3.3	–	204.61
Voltage-Referenced				
3.3 V GTL	10	3.3	–	24.08
2.5 V GTL	10	2.5	–	13.52
3.3 V GTL+	10	3.3	–	24.10
2.5 V GTL+	10	2.5	–	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.22
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.60

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PDC3 is the static power (where applicable) measured on VCCI.*
3. *PAC10 is the total dynamic power measured on VCC and VCCI.*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

Detailed I/O DC Characteristics

***Table 2-18* • Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

***Table 2-19* • I/O Output Buffer Maximum Resistances[1]**

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	100	300
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	4 mA	100	200
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75
3.3 V GTL	20 mA[4]	11	–
2.5 V GTL	20 mA[4]	14	–

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website at www.microsemi.com/index.php?option=com_content&id=1671&lang=en&view=article.*
2. *$R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / IOLspec*
3. *$R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / IOHspec*
4. *Output drive strength is below JEDEC specification.*

Table 2-21 • I/O Short Currents IOSH/IOSL

	Drive Strength	IOSH (mA)*	IOSL (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55

Notes:

1. *T_J = 100°C*
2. *Applicable to 3.3 V LVCMOS Wide Range. IOSL/IOSH dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.*

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-22 • Duration of Short Circuit Event Before Failure

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years

Table 2-28 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
12 mA	Std.	0.66	6.03	0.04	1.20	1.57	0.43	6.14	5.02	3.28	3.47	8.37	7.26	ns
	–1	0.56	5.13	0.04	1.02	1.33	0.36	5.22	4.27	2.79	2.95	7.12	6.17	ns
	–2	0.49	4.50	0.03	0.90	1.17	0.32	4.58	3.75	2.45	2.59	6.25	5.42	ns
16 mA	Std.	0.66	5.62	0.04	1.20	1.57	0.43	5.72	4.72	3.32	3.58	7.96	6.96	ns
	–1	0.56	4.78	0.04	1.02	1.33	0.36	4.87	4.02	2.83	3.04	6.77	5.92	ns
	–2	0.49	4.20	0.03	0.90	1.17	0.32	4.27	3.53	2.48	2.67	5.94	5.20	ns
24 mA	Std.	0.66	5.24	0.04	1.20	1.57	0.43	5.34	4.69	3.39	3.96	7.58	6.93	ns
	–1	0.56	4.46	0.04	1.02	1.33	0.36	4.54	3.99	2.88	3.37	6.44	5.89	ns
	–2	0.49	3.92	0.03	0.90	1.17	0.32	3.99	3.50	2.53	2.96	5.66	5.17	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

1.8 V LVCMOS

Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-37 • Minimum and Maximum DC Input and Output Levels

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	11	9	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	22	17	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	6	6	44	35	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8	51	45	10	10
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12	74	91	10	10
16 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	16	16	74	91	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

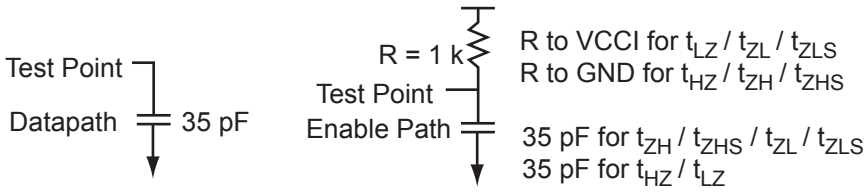


Figure 2-9 • AC Loading

Table 2-38 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	1.8	0.9	–	35

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-99 • RAM4K9
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.28	0.33	ns
t_{AH}	Address hold time	0.00	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.14	0.16	0.19	ns
t_{ENH}	REN, WEN hold time	0.10	0.11	0.13	ns
t_{BKS}	BLK setup time	0.23	0.27	0.31	ns
t_{BKH}	BLK hold time	0.02	0.02	0.02	ns
t_{DS}	Input data (DIN) setup time	0.18	0.21	0.25	ns
t_{DH}	Input data (DIN) hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	1.79	2.03	2.39	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.36	2.68	3.15	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	0.89	1.02	1.20	ns
t_{C2CWWL} [1]	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Closing Edge	0.33	0.28	0.25	ns
t_{C2CWWH} [1]	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge	0.30	0.26	0.23	ns
t_{C2CRWH} [1]	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.45	0.38	0.34	ns
t_{C2CWRH} [1]	Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge	0.49	0.42	0.37	ns
t_{RSTBQ}	RESET Low to data out Low on DO (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on DO (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.21	0.24	0.29	ns
t_{CYC}	Clock cycle time	3.23	3.68	4.32	ns
F_{MAX}	Maximum frequency	310	272	231	MHz

Notes:

1. *For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

FIFO

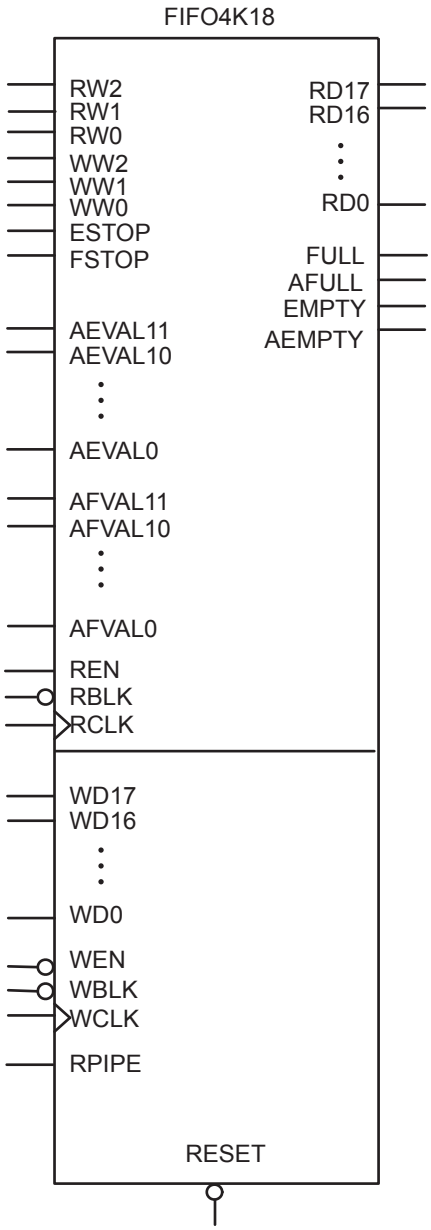


Figure 2-46 • **FIFO Model**

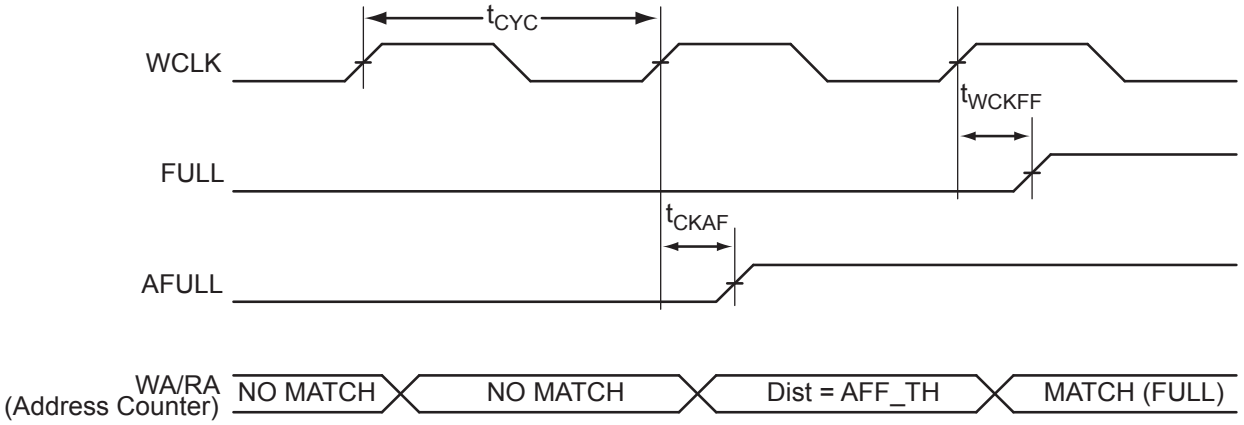


Figure 2-51 • **FIFO FULL Flag and AFULL Flag Assertion**

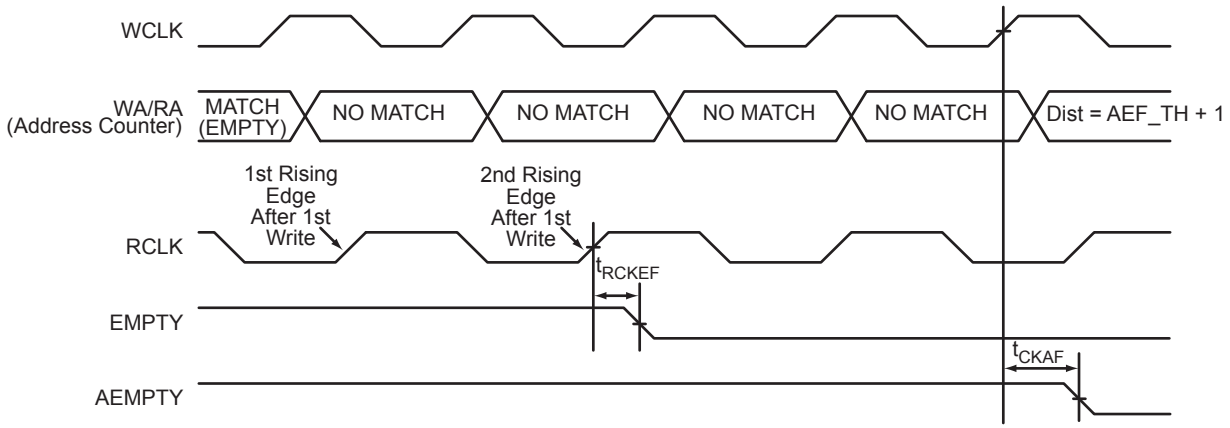


Figure 2-52 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

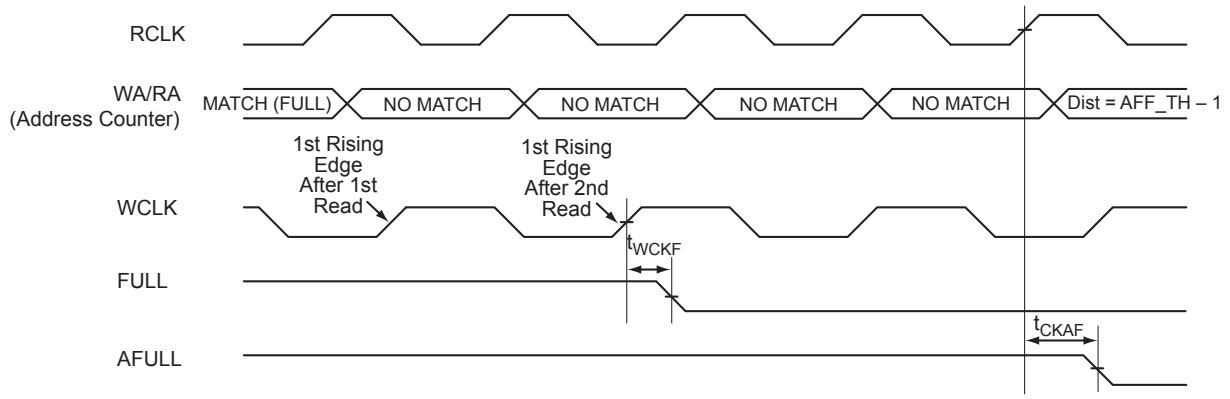


Figure 2-53 • **FIFO FULL Flag and AFULL Flag Deassertion**

Refer to the I/O Structure section of the *ProASIC3E FPGA Fabric User's Guide* for an explanation of the naming of global pins.

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 W to 1 kΩ will satisfy the requirements. Refer to Table 3-1 for more information.

***Table 3-1* • Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on the JTAG chain*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin is pulled down.*

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

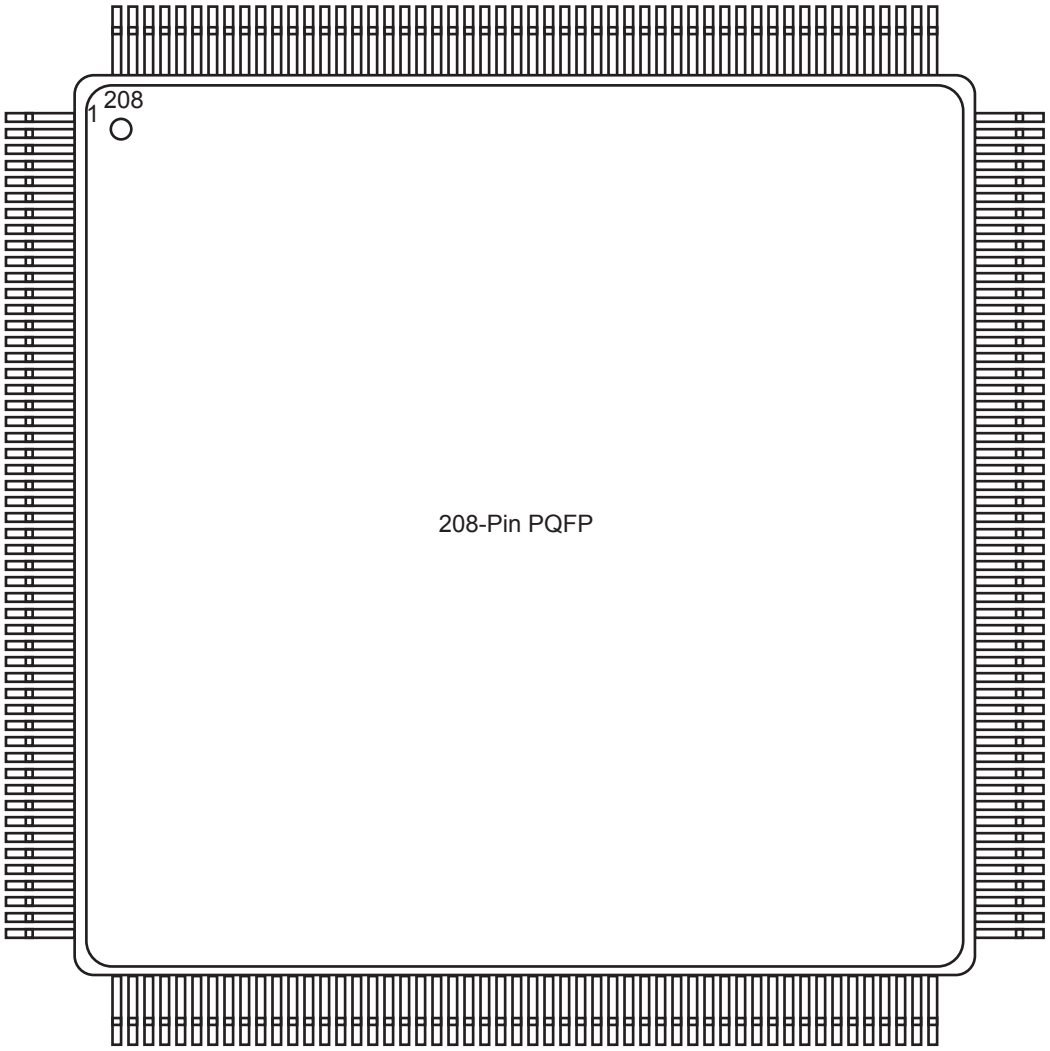
The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-1 and must satisfy the parallel resistance value requirement. The values in Table 3-1 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

4 – Package Pin Assignments

PQ208



Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/products/fpga-soc/solutions*.

PQ208	
Pin Number	A3PE3000 Function
118	IO134NDB3V2
119	IO134PDB3V2
120	IO132NDB3V2
121	IO132PDB3V2
122	GND
123	VCCIB3
124	GCC2/IO117PSB3V0
125	GCB2/IO116PSB3V0
126	NC
127	IO115NDB3V0
128	GCA2/IO115PDB3V0
129	GCA1/IO114PPB3V0
130	GND
131	VCCPLC
132	GCA0/IO114NPB3V0
133	VCOMPLC
134	GCB0/IO113NDB2V3
135	GCB1/IO113PDB2V3
136	GCC1/IO112PSB2V3
137	IO110NDB2V3
138	IO110PDB2V3
139	IO106PSB2V3
140	VCCIB2
141	GND
142	VCC
143	IO99NDB2V2
144	IO99PDB2V2
145	IO96NDB2V1
146	IO96PDB2V1
147	IO91NDB2V1
148	IO91PDB2V1
149	IO88NDB2V0
150	IO88PDB2V0
151	GBC2/IO84PSB2V0
152	GBA2/IO82PSB2V0
153	GBB2/IO83PSB2V0
154	VMV2
155	GNDQ
156	GND

PQ208	
Pin Number	A3PE3000 Function
157	VMV1
158	GNDQ
159	GBA1/IO81PDB1V4
160	GBA0/IO81NDB1V4
161	GBB1/IO80PDB1V4
162	GND
163	GBB0/IO80NDB1V4
164	GBC1/IO79PDB1V4
165	GBC0/IO79NDB1V4
166	IO74PDB1V4
167	IO74NDB1V4
168	IO70PDB1V3
169	IO70NDB1V3
170	VCCIB1
171	VCC
172	IO56PSB1V1
173	IO55PDB1V1
174	IO55NDB1V1
175	IO54PDB1V1
176	IO54NDB1V1
177	IO40PDB0V4
178	GND
179	IO40NDB0V4
180	IO37PDB0V4
181	IO37NDB0V4
182	IO35PDB0V4
183	IO35NDB0V4
184	IO32PDB0V3
185	IO32NDB0V3
186	VCCIB0
187	VCC
188	IO28PDB0V3
189	IO28NDB0V3
190	IO24PDB0V2
191	IO24NDB0V2
192	IO21PSB0V2
193	IO16PDB0V1
194	IO16NDB0V1
195	GND

PQ208	
Pin Number	A3PE3000 Function
196	IO11PDB0V1
197	IO11NDB0V1
198	IO08PDB0V0
199	IO08NDB0V0
200	VCCIB0
201	GAC1/IO02PDB0V0
202	GAC0/IO02NDB0V0
203	GAB1/IO01PDB0V0
204	GAB0/IO01NDB0V0
205	GAA1/IO00PDB0V0
206	GAA0/IO00NDB0V0
207	GNDQ
208	VMV0

FG324	
Pin Number	**A3PE3000 FBGA**
N1	IO247NDB6V1
N2	IO247PDB6V1
N3	IO251NPB6V2
N4	GEC0/IO236NDB6V0
N5	VCOMPLE
N6	IO212NDB5V2
N7	IO212PDB5V2
N8	IO192NPB4V4
N9	IO174PDB4V2
N10	IO170PDB4V2
N11	GDA2/IO154PPB4V0
N12	GDB2/IO155PPB4V0
N13	GDA1/IO153PPB3V4
N14	VCOMPLD
N15	GDB0/IO152NDB3V4
N16	GDB1/IO152PDB3V4
N17	IO138NDB3V3
N18	IO138PDB3V3
P1	IO245PDB6V1
P2	GNDQ
P3	VMV6
P4	GEC1/IO236PDB6V0
P5	VCCPLE
P6	IO214PDB5V2
P7	VCCIB5
P8	GND
P9	IO174NDB4V2
P10	IO170NDB4V2
P11	GND
P12	VCCIB4
P13	IO155NPB4V0
P14	VCCPLD
P15	VJTAG
P16	GDC0/IO151NDB3V4
P17	GDC1/IO151PDB3V4
P18	IO142PDB3V3

FG324	
Pin Number	**A3PE3000 FBGA**
R1	IO245NDB6V1
R2	VCCIB6
R3	GEA1/IO234PPB6V0
R4	IO232NDB5V4
R5	GEB2/IO232PDB5V4
R6	IO214NDB5V2
R7	IO202PDB5V1
R8	IO194PDB5V0
R9	IO186PDB4V4
R10	IO178PDB4V3
R11	IO168NSB4V1
R12	IO164PDB4V1
R13	GDC2/IO156PDB4V0
R14	TCK
R15	VPUMP
R16	TRST
R17	VCCIB3
R18	IO142NDB3V3
T1	IO241PDB6V0
T2	GEA0/IO234NPB6V0
T3	IO233NPB5V4
T4	IO231NPB5V4
T5	VMV5
T6	IO208NDB5V1
T7	IO202NDB5V1
T8	IO194NDB5V0
T9	IO186NDB4V4
T10	IO178NDB4V3
T11	IO166NPB4V1
T12	IO164NDB4V1
T13	IO156NDB4V0
T14	VMV4
T15	TDI
T16	GNDQ
T17	TDO
T18	IO146PDB3V4

FG324	
Pin Number	**A3PE3000 FBGA**
U1	IO241NDB6V0
U2	GEA2/IO233PPB5V4
U3	GEC2/IO231PPB5V4
U4	VCCIB5
U5	GNDQ
U6	IO208PDB5V1
U7	IO198PPB5V0
U8	VCCIB5
U9	IO182NPB4V3
U10	IO180NPB4V3
U11	VCCIB4
U12	IO166PPB4V1
U13	IO162PDB4V1
U14	GNDQ
U15	VCCIB4
U16	TMS
U17	VMV3
U18	IO146NDB3V4
V1	GND
V2	IO218NDB5V3
V3	IO218PDB5V3
V4	IO206NDB5V1
V5	IO206PDB5V1
V6	IO198NPB5V0
V7	GND
V8	IO190NDB4V4
V9	IO190PDB4V4
V10	IO182PPB4V3
V11	IO180PPB4V3
V12	GND
V13	IO162NDB4V1
V14	IO160NDB4V0
V15	IO160PDB4V0
V16	IO158NDB4V0
V17	IO158PDB4V0
V18	GND

FG484	
Pin Number	**A3PE600 Function**
C21	NC
C22	VCCIB2
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0
D7	GAB0/IO01NDB0V0
D8	IO05PDB0V0
D9	IO10PDB0V1
D10	IO12PDB0V2
D11	IO16NDB0V2
D12	IO23NDB1V0
D13	IO23PDB1V0
D14	IO28NDB1V1
D15	IO28PDB1V1
D16	GBB1/IO34PDB1V1
D17	GBA0/IO35NDB1V1
D18	GBA1/IO35PDB1V1
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO133PDB7V1
E5	GAA2/IO134PDB7V1
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO05NDB0V0
E9	IO10NDB0V1
E10	IO12NDB0V2
E11	IO16PDB0V2
E12	IO20NDB1V0

FG484	
Pin Number	**A3PE600 Function**
E13	IO24NDB1V0
E14	IO24PDB1V0
E15	GBC1/IO33PDB1V1
E16	GBB0/IO34NDB1V1
E17	GNDQ
E18	GBA2/IO36PDB2V0
E19	IO42NDB2V0
E20	GND
E21	NC
E22	NC
F1	NC
F2	IO131NDB7V1
F3	IO131PDB7V1
F4	IO133NDB7V1
F5	IO134NDB7V1
F6	VMV7
F7	VCCPLA
F8	GAC0/IO02NDB0V0
F9	GAC1/IO02PDB0V0
F10	IO15NDB0V2
F11	IO15PDB0V2
F12	IO20PDB1V0
F13	IO25NDB1V0
F14	IO27PDB1V0
F15	GBC0/IO33NDB1V1
F16	VCCPLB
F17	VMV2
F18	IO36NDB2V0
F19	IO42PDB2V0
F20	NC
F21	NC
F22	NC
G1	IO127NDB7V1
G2	IO127PDB7V1
G3	NC
G4	IO128PDB7V1

FG484	
Pin Number	**A3PE600 Function**
G5	IO129PDB7V1
G6	GAC2/IO132PDB7V1
G7	VCOMPLA
G8	GNDQ
G9	IO09NDB0V1
G10	IO09PDB0V1
G11	IO13PDB0V2
G12	IO21PDB1V0
G13	IO25PDB1V0
G14	IO27NDB1V0
G15	GNDQ
G16	VCOMPLB
G17	GBB2/IO37PDB2V0
G18	IO39PDB2V0
G19	IO39NDB2V0
G20	IO43PDB2V0
G21	IO43NDB2V0
G22	NC
H1	NC
H2	NC
H3	VCC
H4	IO128NDB7V1
H5	IO129NDB7V1
H6	IO132NDB7V1
H7	IO130PDB7V1
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO13NDB0V2
H12	IO21NDB1V0
H13	VCCIB1
H14	VCCIB1
H15	VMV1
H16	GBC2/IO38PDB2V0
H17	IO37NDB2V0
H18	IO41NDB2V0

FG676	
Pin Number	A3PE1500 Function
G13	IO21NDB0V2
G14	IO27PDB0V3
G15	IO35NDB1V0
G16	IO39PDB1V0
G17	IO51NDB1V2
G18	IO53NDB1V2
G19	VCCIB1
G20	GBA2/IO58PPB2V0
G21	GNDQ
G22	IO64NDB2V1
G23	IO64PDB2V1
G24	IO72PDB2V2
G25	IO72NDB2V2
G26	IO78PDB2V2
H1	IO208NDB7V2
H2	IO208PDB7V2
H3	IO209NDB7V2
H4	IO209PDB7V2
H5	IO219NDB7V3
H6	GAC2/IO219PDB7V3
H7	VCCIB7
H8	VCC
H9	VCCIB0
H10	VCCIB0
H11	VCCIB0
H12	VCCIB0
H13	VCCIB0
H14	VCCIB1
H15	VCCIB1
H16	VCCIB1
H17	VCCIB1
H18	VCCIB1
H19	VCC
H20	VCC
H21	IO58NPB2V0
H22	IO70PDB2V1

FG676	
Pin Number	A3PE1500 Function
H23	IO69PDB2V1
H24	IO76PDB2V2
H25	IO76NDB2V2
H26	IO78NDB2V2
J1	IO197NDB7V0
J2	IO197PDB7V0
J3	VMV7
J4	IO215NDB7V3
J5	IO215PDB7V3
J6	IO214PDB7V3
J7	IO214NDB7V3
J8	VCCIB7
J9	VCC
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	VCC
J15	VCC
J16	VCC
J17	VCC
J18	VCC
J19	VCCIB2
J20	IO62PDB2V0
J21	IO62NDB2V0
J22	IO70NDB2V1
J23	IO69NDB2V1
J24	VMV2
J25	IO80PDB2V3
J26	IO80NDB2V3
K1	IO195PDB7V0
K2	IO199NDB7V1
K3	IO199PDB7V1
K4	IO205NDB7V1
K5	IO205PDB7V1
K6	IO217PDB7V3

FG676	
Pin Number	A3PE1500 Function
K7	IO217NDB7V3
K8	VCCIB7
K9	VCC
K10	GND
K11	GND
K12	GND
K13	GND
K14	GND
K15	GND
K16	GND
K17	GND
K18	VCC
K19	VCCIB2
K20	IO65PDB2V1
K21	IO65NDB2V1
K22	IO74PDB2V2
K23	IO74NDB2V2
K24	IO75PDB2V2
K25	IO75NDB2V2
K26	IO84PDB2V3
L1	IO195NDB7V0
L2	IO198PPB7V0
L3	GNDQ
L4	IO201PDB7V1
L5	IO201NDB7V1
L6	IO210NDB7V2
L7	IO210PDB7V2
L8	VCCIB7
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	GND
L15	GND
L16	GND

FG896	
Pin Number	A3PE3000 Function
A2	GND
A3	GND
A4	IO14NPB0V1
A5	GND
A6	IO07NPB0V0
A7	GND
A8	IO09NDB0V1
A9	IO17NDB0V2
A10	IO17PDB0V2
A11	IO21NDB0V2
A12	IO21PDB0V2
A13	IO33NDB0V4
A14	IO33PDB0V4
A15	IO35NDB0V4
A16	IO35PDB0V4
A17	IO41NDB1V0
A18	IO43NDB1V0
A19	IO43PDB1V0
A20	IO45NDB1V0
A21	IO45PDB1V0
A22	IO57NDB1V2
A23	IO57PDB1V2
A24	GND
A25	IO69PPB1V3
A26	GND
A27	GBC1/IO79PPB1V4
A28	GND
A29	GND
AA1	IO256PDB6V2
AA2	IO248PDB6V1
AA3	IO248NDB6V1
AA4	IO246NDB6V1
AA5	GEA1/IO234PDB6V0
AA6	GEA0/IO234NDB6V0
AA7	IO243PPB6V1
AA8	IO245NDB6V1

FG896	
Pin Number	A3PE3000 Function
AA9	GEB1/IO235PPB6V0
AA10	VCC
AA11	IO226PPB5V4
AA12	VCCIB5
AA13	VCCIB5
AA14	VCCIB5
AA15	VCCIB5
AA16	VCCIB4
AA17	VCCIB4
AA18	VCCIB4
AA19	VCCIB4
AA20	IO174PDB4V2
AA21	VCC
AA22	IO142NPB3V3
AA23	IO144NDB3V3
AA24	IO144PDB3V3
AA25	IO146NDB3V4
AA26	IO146PDB3V4
AA27	IO147PDB3V4
AA28	IO139NDB3V3
AA29	IO139PDB3V3
AA30	IO133NDB3V2
AB1	IO256NDB6V2
AB2	IO244PDB6V1
AB3	IO244NDB6V1
AB4	IO241PDB6V0
AB5	IO241NDB6V0
AB6	IO243NPB6V1
AB7	VCCIB6
AB8	VCCPLE
AB9	VCC
AB10	IO222PDB5V3
AB11	IO218PPB5V3
AB12	IO206NDB5V1
AB13	IO206PDB5V1
AB14	IO198NDB5V0

FG896	
Pin Number	A3PE3000 Function
AB15	IO198PDB5V0
AB16	IO192NDB4V4
AB17	IO192PDB4V4
AB18	IO178NDB4V3
AB19	IO178PDB4V3
AB20	IO174NDB4V2
AB21	IO162NPB4V1
AB22	VCC
AB23	VCCPLD
AB24	VCCIB3
AB25	IO150PDB3V4
AB26	IO148PDB3V4
AB27	IO147NDB3V4
AB28	IO145PDB3V3
AB29	IO143PDB3V3
AB30	IO137PDB3V2
AC1	IO254PDB6V2
AC2	IO254NDB6V2
AC3	IO240PDB6V0
AC4	GEC1/IO236PDB6V0
AC5	IO237PDB6V0
AC6	IO237NDB6V0
AC7	VCOMPLE
AC8	GND
AC9	IO226NPB5V4
AC10	IO222NDB5V3
AC11	IO216NPB5V2
AC12	IO210NPB5V2
AC13	IO204NDB5V1
AC14	IO204PDB5V1
AC15	IO194NDB5V0
AC16	IO188NDB4V4
AC17	IO188PDB4V4
AC18	IO182PPB4V3
AC19	IO170NPB4V2
AC20	IO164NDB4V1

Revision	Changes	Page
Revision 11 (August 2012)	Added a Note stating "VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information." to Table 2-1 • Absolute Maximum Ratings and Table 2-2 • Recommended Operating Conditions [1] (SAR 38322).	2-1 3-1 2-1
	The drive strength, IOL, and IOH value for 3.3 V GTL and 2.5 V GTL was changed from 25 mA to 20 mA in the following tables (SAR 31924): "Summary of Maximum and Minimum DC Input and Output Levels" table "Summary of I/O Timing Characteristics—Software Default Settings" table "I/O Output Buffer Maximum Resistances[1]" table "Minimum and Maximum DC Input and Output Levels" table) "Minimum and Maximum DC Input and Output Levels" table Also added note stating "Output drive strength is below JEDEC specification" for Tables 2-17 and 2-19. Additionally, the IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected from 51 to 35 (for 3.3 V GTL+) and from 40 to 33 (for 2.5 V GTL+) in table Table 2-13 (SAR 39714).	 2-16 2-19 2-20 2-39 2-40
	"Duration of Short Circuit Event Before Failure" table was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 37934).	2-22
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34796): "It uses a 5 V–tolerant input buffer and push-pull output buffer." This change was made in revision 10 and omitted from the change table in error.	2-30
Revision 11 (continued)	Figure 2-11 was updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34889).	2-38
	In Table 2-81 VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 37222).	2-52
	Figure 2-47and Figure 2-48 are new (SAR 34848).	2-79
	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions and Packaging" chapter: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with “Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks” (SAR 38322). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1

Revision	Changes	Page
Revision 3 (Apr 2008) Packaging v1.2	The following pins had duplicates and the extra pins were deleted from the "PQ208" A3PE3000 table: 36, 62, 171 Note: There were no pin function changes in this update.	4-2
	The following pins had duplicates and the extra pins were deleted from the "FG324" table: E2, E3, E16, E17, P2, P3, T16, U17 Note: There were no pin function changes in this update.	4-12
	The "FG256" pin table was updated for the A3PE600 device because the old PAT were based on the IFX die, and this is the final UMC die version.	4-9
	The "FG484" was updated for the A3PE600 device because the old PAT were based on the IFX die, and this is the final UMC die version.	4-22
	The following pins had duplicates and the extra pins were deleted from the "FG896" table: AD6, AE5, AE28, AF29, F5, F26, G6, G25 Note: There were no pin function changes in this update.	4-41
Revision 2 (Mar 2008) Product Brief rev. 1	The FG324 package was added to the "ProASIC3E Product Family" table, the "I/Os Per Package1" table, and the "Temperature Grade Offerings" table for A3PE3000.	I, II, IV
Revision 1 (Feb 2008) DC and Switching Characteristics v1.1	In Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature 1, Maximum Operating Junction Temperature was changed from 110°C to 100°C for both commercial and industrial grades.	2
	The "PLL Behavior at Brownout Condition" section is new.	2-4
	In the "PLL Contribution—PPLL" section, the following was deleted: FCLKIN is the input clock frequency.	2-10
	In Table 2-14 • Summary of Maximum and Minimum DC Input Levels, the note was incorrect. It previously said T_J and it was corrected and changed to T_A.	2-17
	In Table 2-98 • ProASIC3E CCC/PLL Specification, the SCLK parameter and note 1 are new.	2-70
	Table 2-103 • JTAG 1532 was populated with the parameter data, which was not in the previous version of the document.	2-83
Revision 1 (cont'd) Packaging v1.1	The "PQ208" pin table for A3PE3000 was updated.	4-2
	The "FG324" pin table for A3PE3000 is new.	4-13
	The "FG484" pin table for A3PE3000 is new.	4-17
	The "FG896" pin table for A3PE3000 is new.	4-41
Revision 0 (Jan 2008)	This document was previously in datasheet v2.1. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is 51700098-001-0.	N/A
v2.1 (July 2007)	CoreMP7 information was removed from the "Features and Benefits" section.	1-I
	The M1 device part numbers have been updated in ProASIC3E Product Family, "Packaging Tables", "Temperature Grade Offerings", "Speed Grade and Temperature Grade Matrix", and "Speed Grade and Temperature Grade Matrix".	1-I