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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	270
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3pe600-2fgg484i

SRAM and FIFO

ProASIC3E devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

ProASIC3E devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC3E family contains six CCCs, each with an integrated PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

To maximize user I/Os, only the center east and west PLLs are available in devices using the PQ208 package. However, all six CCC blocks are still usable; the four corner CCCs allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from –7.56 ns to +11.12 ns
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration.
- Output duty cycle = 50% ± 1.5% or better
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used
- Maximum acquisition time = 300 µs
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter— allowable input jitter is up to 1.5 ns
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × (350 MHz / f_{OUT_CCC})

Global Clocking

ProASIC3E devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high fanout nets.

2 – ProASIC3E DC and Switching Characteristics

General Specifications

DC and switching characteristics for –F speed grade targets are based only on simulation.

The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI [2]	DC I/O output buffer supply voltage	–0.3 to 3.75	V
VMV [2]	DC I/O input buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG} [3]	Storage temperature	–65 to +150	°C
T_J [3]	Junction temperature	+125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-3 on page 2-2.*
2. *VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information.*
3. *For flash programming and retention maximum limits, refer to Table 2-3 on page 2-2, and for recommended operating limits, refer to Table 2-2 on page 2-2.*

Table 2-2 • Recommended Operating Conditions [1]

Symbol	Parameter		Commercial	Industrial	Units
T_A	Ambient temperature		0 to +70	–40 to +85	°C
T_J	Junction temperature		0 to +85	–40 to +100	°C
VCC	1.5 V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage	Programming Mode[2]	3.15 to 3.45	3.15 to 3.45	V
		Operation[3]	0 to 3.6	0 to 3.6	V
VCCPLL	Analog power supply (PLL)		1.425 to 1.575	1.425 to 1.575	V
VCCI and VMV [4]	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	3.0 V DC supply voltage[5]		2.7 to 3.6	2.7 to 3.6	V
	LVDS/B-LVDS/M-LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.*
3. *VPUMP can be left floating during normal operation (not programming mode).*
4. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-13 on page 2-16. VMV and VCCI should be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information.*
5. *To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microsemi recommends that the user follow best design practices using Microsemi's timing and power simulation tools.*
6. *3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.*

Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature [1]

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

Table 2-4 • Overshoot and Undershoot Limits [1]

VCCI and VMV	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
3. *This table does not provide PCI overshoot/undershoot limits.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC®3E device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4.

There are five regions to consider during power-up.

ProASIC3E I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 on page 2-4).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-13 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[1]	Slew Rate	VIL		VIH		VOL	VOH	IOL[3]	IOH[3]
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range	100 µA	12 mA	High	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI Specification										
3.3 V PCI-X	Per PCI-X Specification										
3.3 V GTL	20 mA[2]	20 mA[2]	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
2.5 V GTL	20 mA[2]	20 mA[2]	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
3.3 V GTL+	35 mA	35 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35
2.5 V GTL+	33 mA	33 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33
HSTL (I)	8 mA	8 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8
HSTL (II)	15 mA[2]	15 mA[2]	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15
SSTL2 (I)	15 mA	15 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15
SSTL2 (II)	18 mA	18 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18
SSTL3 (I)	14 mA	14 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14
SSTL3 (II)	21 mA	21 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *Output drive strength is below JEDEC specification.*
3. *Currents are measured at 85°C junction temperature.*
4. *Output Slew Rates can be extracted from IBIS Models, located at http://www.microsemi.com/index.php?option=com_content&id=1671&lang=en&view=article.*

Table 2-17 • Summary of I/O Timing Characteristics—Software Default Settings –2 Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option)[1]	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)
3.3 V LVTTL / 3.3 V LVCMOS	12	12	High	35	–	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81
3.3 V LVCMOS Wide Range[2]	100 µA	12	High	35	–	0.49	4.24	0.03	1.36	1.78	0.32	4.24	3.25	3.78	4.17	6.77	5.79
2.5 V LVCMOS	12	12	High	35	–	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28
1.8 V LVCMOS	12	12	High	35	–	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98
1.5 V LVCMOS	12	12	High	35	–	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37
3.3 V PCI	Per PCI spec	–	High	10	25 [3]	0.49	2.09	0.03	0.78	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16
3.3 V PCI-X	Per PCI-X spec	–	High	10	25[3]	0.49	2.09	0.03	0.78	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16
3.3 V GTL	20 [4]	–	High	10	25	0.45	1.55	0.03	2.19	–	0.32	1.52	1.55	–	–	3.19	3.22
2.5 V GTL	20 [4]	–	High	10	25	0.45	1.59	0.03	1.83	–	0.32	1.61	1.59	–	–	3.28	3.26
3.3 V GTL+	35	–	High	10	25	0.45	1.53	0.03	1.19	–	0.32	1.56	1.53	–	–	3.23	3.20
2.5 V GTL+	33	–	High	10	25	0.45	1.65	0.03	1.13	–	0.32	1.68	1.57	–	–	3.35	3.24
HSTL (I)	8	–	High	20	50	0.49	2.37	0.03	1.59	–	0.32	2.42	2.35	–	–	4.09	4.02
HSTL (II)	15 [4]	–	High	20	25	0.49	2.26	0.03	1.59	–	0.32	2.30	2.03	–	–	3.97	3.70
SSTL2 (I)	15	–	High	30	50	0.49	1.59	0.03	1.00	–	0.32	1.62	1.38	–	–	3.29	3.05
SSTL2 (II)	18	–	High	30	25	0.49	1.62	0.03	1.00	–	0.32	1.65	1.32	–	–	3.32	2.99
SSTL3 (I)	14	–	High	30	50	0.49	1.72	0.03	0.93	–	0.32	1.75	1.37	–	–	3.42	3.04
SSTL3 (II)	21	–	High	30	25	0.49	1.54	0.03	0.93	–	0.32	1.57	1.25	–	–	3.24	2.92
LVDS/B-LVDS/ M-LVDS	24	–	High	–	–	0.49	1.40	0.03	1.36	–	–	–	–	–	–	–	–
LVPECL	24	–	High	–	–	0.49	1.36	0.03	1.22	–	–	–	–	–	–	–	–

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3V wide range as specified in the JESD8b specification.*
3. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-38 for connectivity. This resistor is not required during normal operation.*
4. *Output drive strength is below JEDEC specification.*
5. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5.*

Table 2-21 • I/O Short Currents IOSH/IOSL

	Drive Strength	IOSH (mA)*	IOSL (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55

Notes:

1. *T_J = 100°C*
2. *Applicable to 3.3 V LVCMOS Wide Range. IOSL/IOSH dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.*

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-22 • Duration of Short Circuit Event Before Failure

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years

3.3 V LVCMOS Wide Range

Table 2-29 • Minimum and Maximum DC Input and Output Levels

3.3 V LVCMOS Wide Range	Equivalent Software Default Drive Strength Option[1]	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength		Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[4]	Max. mA[4]	µA[5]	µA[5]
100 µA	2 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	27	25	10	10
100 µA	4 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	27	25	10	10
100 µA	6 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	54	51	10	10
100 µA	8 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	54	51	10	10
100 µA	12 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	109	103	10	10
100 µA	16 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	127	132	10	10
100 µA	24 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	181	268	10	10

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN< VCCI. Input current is larger when operating outside recommended ranges.*
4. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

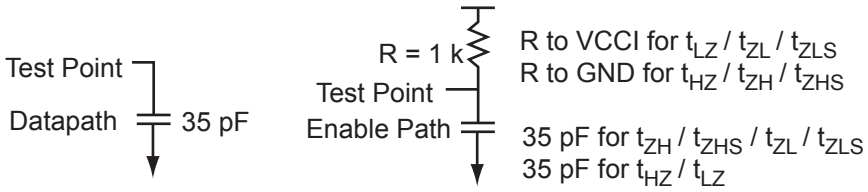

Figure 2-7 • AC Loading

Table 2-30 • 3.3 V LVCMOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	35

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-33 • Minimum and Maximum DC Input and Output Levels

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max., V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

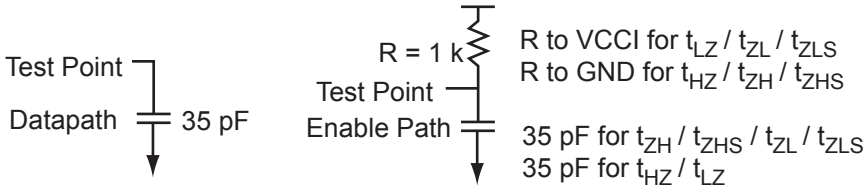

Figure 2-8 • AC Loading

Table 2-34 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-57 • Minimum and Maximum DC Input and Output Levels

2.5 V GTL+	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
33 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

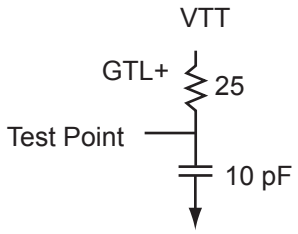

Figure 2-15 • AC Loading

Table 2-58 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-59 • 2.5 V GTL+
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.60	2.21	0.04	1.51	0.43	2.25	2.10			4.48	4.34	ns
–1	0.51	1.88	0.04	1.29	0.36	1.91	1.79			3.81	3.69	ns
–2	0.45	1.65	0.03	1.13	0.32	1.68	1.57			3.35	3.24	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-24. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

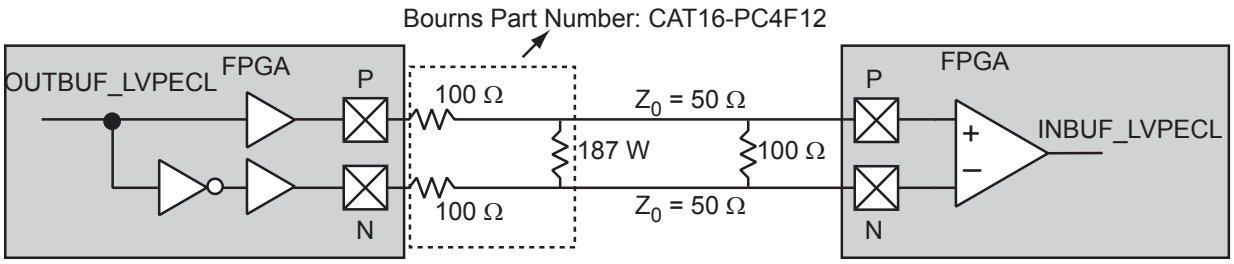

Figure 2-24 • **LVPECL Circuit Diagram and Board-Level Implementation**

Table 2-81 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

Table 2-82 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)
1.64	1.94	Cross point	–

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-83 • **LVPECL**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.66	1.83	0.04	1.63	ns
–1	0.56	1.55	0.04	1.39	ns
–2	0.49	1.36	0.03	1.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

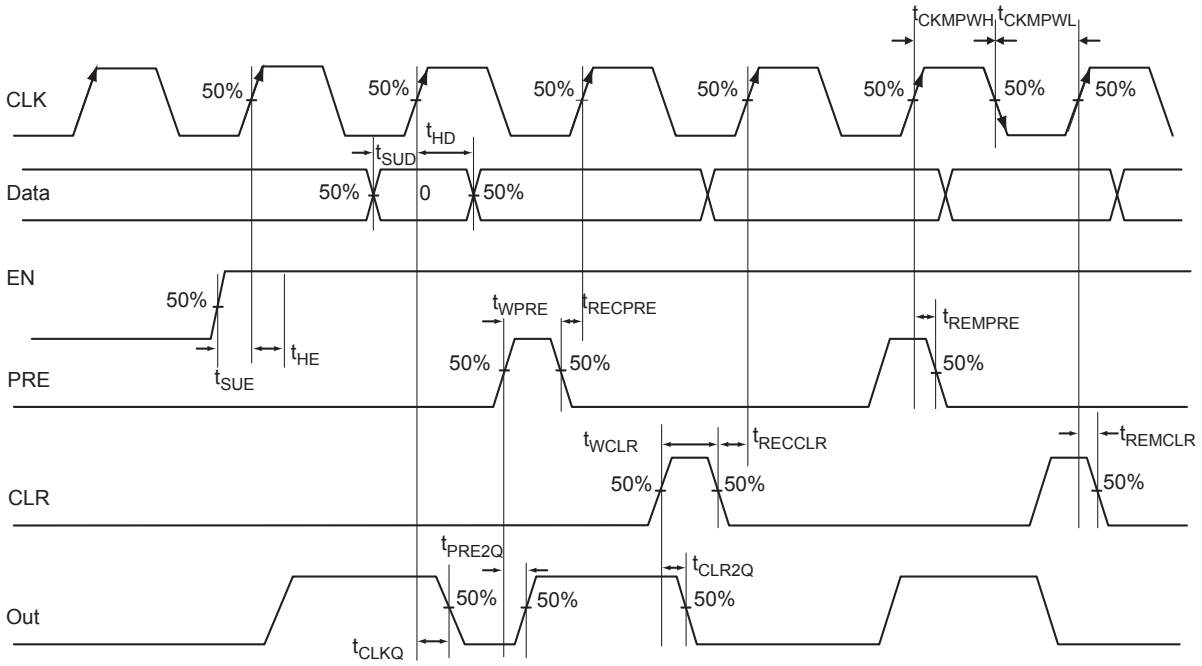

Figure 2-37 • **Timing Model and Waveforms**

Timing Characteristics

Table 2-94 • **Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.55	0.63	0.74	ns
t_{SUD}	Data Setup Time for the Core Register	0.43	0.49	0.57	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.45	0.52	0.61	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.40	0.45	0.53	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.40	0.45	0.53	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.22	0.25	0.30	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.22	0.25	0.30	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.22	0.25	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.22	0.25	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.32	0.37	0.43	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.36	0.41	0.48	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Global Resource Characteristics

A3PE600 Clock Tree Topology

Clock delays are device-specific. Figure 2-38 is an example of a global tree used for clock routing. The global tree presented in Figure 2-38 is driven by a CCC located on the west side of the A3PE600 device. It is used to drive all D-flip-flops in the device.

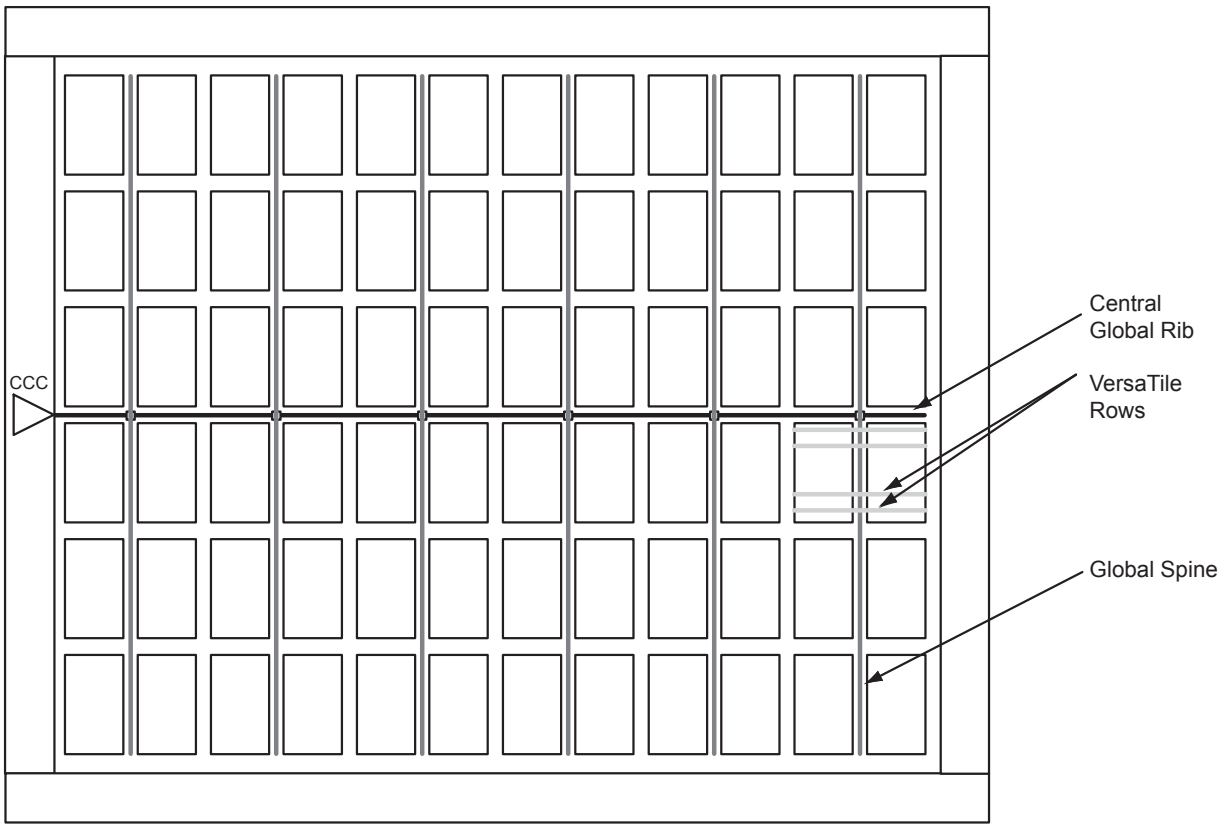

Figure 2-38 • **Example of Global Tree Use in an A3PE600 Device for Clock Routing**

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-70. Table 2-95 on page 2-69, Table 2-96 on page 2-69, and Table 2-97 on page 2-69 present minimum and maximum global clock delays within the device. Minimum and maximum delays are measured with minimum and maximum loading.

Table 2-100 • RAM512X18
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.28	0.33	ns
t_{AH}	Address hold time	0.00	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.18	0.20	0.24	ns
t_{ENH}	REN, WEN hold time	0.06	0.07	0.08	ns
t_{DS}	Input data (WD) setup time	0.18	0.21	0.25	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	2.16	2.46	2.89	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	0.90	1.02	1.20	ns
t_{C2CRWH} [1]	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.50	0.43	0.38	ns
t_{C2CWRH} [1]	Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge	0.59	0.50	0.44	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to data out Low on RD (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.21	0.24	0.29	ns
t_{CYC}	Clock cycle time	3.23	3.68	4.32	ns
F_{MAX}	Maximum frequency	310	272	231	MHz

Notes:

1. *For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

Timing Characteristics

Table 2-101 • FIFO
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.38	1.57	1.84	ns
t_{ENH}	REN, WEN Hold Time	0.02	0.02	0.02	ns
t_{BKS}	BLK Setup Time	0.19	0.22	0.26	ns
t_{BKH}	BLK Hold Time	0.00	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (pass-through)	2.36	2.68	3.15	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.89	1.02	1.20	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (pass-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on RD (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET Recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency	310	272	231	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

3 – Pin Descriptions and Packaging

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

VCCIBx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. In general, unused I/O banks should have their corresponding VCCIX pins tied to GND. If an output pad is terminated to ground through any resistor and if the corresponding VCCIX is left floating, then the leakage current to ground is ~ 0uA. However, if an output pad is terminated to ground through any resistor and the corresponding VCCIX grounded, then the leakage current to ground is ~ 3 uA. For unused banks the aforementioned behavior is to be taken into account while deciding if it’s better to float VCCIX of unused bank or tie it to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V.

When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *ProASIC3E FPGA Fabric User’s Guide* for a complete board solution for the PLL analog power supply and ground.

There are six VCCPLX pins on ProASIC3E devices.

VCOMPLA/B/C/D/E/F **PLL Ground**

Ground to analog PLL power supplies. When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There are six VCOMPL pins (PLL ground) on ProASIC3E devices.

FG256	
Pin Number	**A3PE600 Function**
G13	GCC1/IO50PPB2V1
G14	IO44NDB2V1
G15	IO44PDB2V1
G16	IO49NSB2V1
H1	GFB0/IO119NPB7V0
H2	GFA0/IO118NDB6V1
H3	GFB1/IO119PPB7V0
H4	VCOMPLF
H5	GFC0/IO120NPB7V0
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO50NPB2V1
H13	GCB1/IO51PPB2V1
H14	GCA0/IO52NPB3V0
H15	VCOMPLC
H16	GCB0/IO51NPB2V1
J1	GFA2/IO117PSB6V1
J2	GFA1/IO118PDB6V1
J3	VCCPLF
J4	IO116NDB6V1
J5	GFB2/IO116PDB6V1
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO54PPB3V0
J13	GCA1/IO52PPB3V0
J14	GCC2/IO55PPB3V0
J15	VCCPLC
J16	GCA2/IO53PSB3V0

FG256	
Pin Number	**A3PE600 Function**
K1	GFC2/IO115PSB6V1
K2	IO113PPB6V1
K3	IO112PDB6V1
K4	IO112NDB6V1
K5	VCCIB6
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB3
K13	IO54NPB3V0
K14	IO57NPB3V0
K15	IO55NPB3V0
K16	IO57PPB3V0
L1	IO113NPB6V1
L2	IO109PPB6V0
L3	IO108PDB6V0
L4	IO108NDB6V0
L5	VCCIB6
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB3
L13	GDB0/IO66NPB3V1
L14	IO60NDB3V1
L15	IO60PDB3V1
L16	IO61PDB3V1
M1	IO109NPB6V0
M2	IO106NDB6V0
M3	IO106PDB6V0
M4	GEC0/IO104NPB6V0

FG256	
Pin Number	**A3PE600 Function**
M5	VMV5
M6	VCCIB5
M7	VCCIB5
M8	IO84NDB5V0
M9	IO84PDB5V0
M10	VCCIB4
M11	VCCIB4
M12	VMV3
M13	VCCPLD
M14	GDB1/IO66PPB3V1
M15	GDC1/IO65PDB3V1
M16	IO61NDB3V1
N1	IO105PDB6V0
N2	IO105NDB6V0
N3	GEC1/IO104PPB6V0
N4	VCOMPLE
N5	GNDQ
N6	GEA2/IO101PPB5V2
N7	IO92NDB5V1
N8	IO90NDB5V1
N9	IO82NDB5V0
N10	IO74NDB4V1
N11	IO74PDB4V1
N12	GNDQ
N13	VCOMPLD
N14	VJTAG
N15	GDC0/IO65NDB3V1
N16	GDA1/IO67PDB3V1
P1	GEB1/IO103PDB6V0
P2	GEB0/IO103NDB6V0
P3	VMV6
P4	VCCPLE
P5	IO101NPB5V2
P6	IO95PPB5V1
P7	IO92PDB5V1
P8	IO90PDB5V1

FG484	
Pin Number	A3PE1500 Function
N17	IO91NPB3V0
N18	IO90NPB3V0
N19	IO91PPB3V0
N20	GNDQ
N21	IO93NDB3V0
N22	IO95PDB3V1
P1	NC
P2	IO183PDB6V2
P3	IO187NPB6V2
P4	IO184NPB6V2
P5	IO176PPB6V1
P6	IO182PDB6V1
P7	IO182NDB6V1
P8	VCCIB6
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB3
P16	GDB0/IO109NPB3V2
P17	IO97NDB3V1
P18	IO97PDB3V1
P19	IO99PDB3V1
P20	VMV3
P21	IO98PDB3V1
P22	IO95NDB3V1
R1	NC
R2	IO177PDB6V1
R3	VCC
R4	IO176NPB6V1
R5	IO174NDB6V0
R6	IO174PDB6V0
R7	GEC0/IO169NPB6V0
R8	VMV5

FG484	
Pin Number	A3PE1500 Function
R9	VCCIB5
R10	VCCIB5
R11	IO135NDB5V0
R12	IO135PDB5V0
R13	VCCIB4
R14	VCCIB4
R15	VMV3
R16	VCCPLD
R17	GDB1/IO109PPB3V2
R18	GDC1/IO108PDB3V2
R19	IO99NDB3V1
R20	VCC
R21	IO98NDB3V1
R22	IO101PDB3V1
T1	NC
T2	IO177NDB6V1
T3	NC
T4	IO171PDB6V0
T5	IO171NDB6V0
T6	GEC1/IO169PPB6V0
T7	VCOMPLE
T8	GNDQ
T9	GEA2/IO166PPB5V3
T10	IO145NDB5V1
T11	IO141NDB5V0
T12	IO139NDB5V0
T13	IO119NDB4V1
T14	IO119PDB4V1
T15	GNDQ
T16	VCOMPLD
T17	VJTAG
T18	GDC0/IO108NDB3V2
T19	GDA1/IO110PDB3V2
T20	NC
T21	IO103PDB3V2
T22	IO101NDB3V1

FG484	
Pin Number	A3PE1500 Function
U1	IO175PPB6V1
U2	IO173PDB6V0
U3	IO173NDB6V0
U4	GEB1/IO168PDB6V0
U5	GEB0/IO168NDB6V0
U6	VMV6
U7	VCCPLE
U8	IO166NPB5V3
U9	IO157PPB5V2
U10	IO145PDB5V1
U11	IO141PDB5V0
U12	IO139PDB5V0
U13	IO121NDB4V1
U14	IO121PDB4V1
U15	VMV4
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO110NDB3V2
U20	NC
U21	IO103NDB3V2
U22	IO105PDB3V2
V1	NC
V2	IO175NPB6V1
V3	GND
V4	GEA1/IO167PDB6V0
V5	GEA0/IO167NDB6V0
V6	GNDQ
V7	GEC2/IO164PDB5V3
V8	IO157NPB5V2
V9	IO151NDB5V2
V10	IO151PDB5V2
V11	IO137NDB5V0
V12	IO137PDB5V0
V13	IO123NDB4V1
V14	IO123PDB4V1

FG896	
Pin Number	A3PE3000 Function
AG9	IO225NPB5V3
AG10	IO223NPB5V3
AG11	IO221PDB5V3
AG12	IO221NDB5V3
AG13	IO205NPB5V1
AG14	IO199NDB5V0
AG15	IO199PDB5V0
AG16	IO187NDB4V4
AG17	IO187PDB4V4
AG18	IO181NDB4V3
AG19	IO171PPB4V2
AG20	IO165NPB4V1
AG21	IO161NPB4V0
AG22	IO159NDB4V0
AG23	IO159PDB4V0
AG24	IO158PPB4V0
AG25	GDB2/IO155PDB4V0
AG26	GDA2/IO154PPB4V0
AG27	GND
AG28	VJTAG
AG29	VCC
AG30	IO149NDB3V4
AH1	GND
AH2	IO233NPB5V4
AH3	VCC
AH4	GEB2/IO232PPB5V4
AH5	VCCIB5
AH6	IO219NDB5V3
AH7	IO219PDB5V3
AH8	IO227NDB5V4
AH9	IO227PDB5V4
AH10	IO225PPB5V3
AH11	IO223PPB5V3
AH12	IO211NDB5V2
AH13	IO211PDB5V2
AH14	IO205PPB5V1

FG896	
Pin Number	A3PE3000 Function
AH15	IO195NDB5V0
AH16	IO185NDB4V3
AH17	IO185PDB4V3
AH18	IO181PDB4V3
AH19	IO177NDB4V2
AH20	IO171NPB4V2
AH21	IO165PPB4V1
AH22	IO161PPB4V0
AH23	IO157NDB4V0
AH24	IO157PDB4V0
AH25	IO155NDB4V0
AH26	VCCIB4
AH27	TDI
AH28	VCC
AH29	VPUMP
AH30	GND
AJ1	GND
AJ2	GND
AJ3	GEA2/IO233PPB5V4
AJ4	VCC
AJ5	IO217NPB5V2
AJ6	VCC
AJ7	IO215NPB5V2
AJ8	IO213NDB5V2
AJ9	IO213PDB5V2
AJ10	IO209NDB5V1
AJ11	IO209PDB5V1
AJ12	IO203NDB5V1
AJ13	IO203PDB5V1
AJ14	IO197NDB5V0
AJ15	IO195PDB5V0
AJ16	IO183NDB4V3
AJ17	IO183PDB4V3
AJ18	IO179NPB4V3
AJ19	IO177PDB4V2
AJ20	IO173NDB4V2

FG896	
Pin Number	A3PE3000 Function
AJ21	IO173PDB4V2
AJ22	IO163NDB4V1
AJ23	IO163PDB4V1
AJ24	IO167NPB4V1
AJ25	VCC
AJ26	IO156NPB4V0
AJ27	VCC
AJ28	TMS
AJ29	GND
AJ30	GND
AK2	GND
AK3	GND
AK4	IO217PPB5V2
AK5	GND
AK6	IO215PPB5V2
AK7	GND
AK8	IO207NDB5V1
AK9	IO207PDB5V1
AK10	IO201NDB5V0
AK11	IO201PDB5V0
AK12	IO193NDB4V4
AK13	IO193PDB4V4
AK14	IO197PDB5V0
AK15	IO191NDB4V4
AK16	IO191PDB4V4
AK17	IO189NDB4V4
AK18	IO189PDB4V4
AK19	IO179PPB4V3
AK20	IO175NDB4V2
AK21	IO175PDB4V2
AK22	IO169NDB4V1
AK23	IO169PDB4V1
AK24	GND
AK25	IO167PPB4V1
AK26	GND
AK27	GDC2/IO156PPB4V0

FG896	
Pin Number	**A3PE3000 Function**
W29	IO131PDB3V2
W30	IO123NDB3V1
Y1	IO266PDB6V4
Y2	IO250PDB6V2
Y3	IO250NDB6V2
Y4	IO246PDB6V1
Y5	IO247NDB6V1
Y6	IO247PDB6V1
Y7	IO249NPB6V1
Y8	IO245PDB6V1
Y9	IO253NDB6V2
Y10	GEB0/IO235NPB6V0
Y11	VCC
Y12	VCC
Y13	VCC
Y14	VCC
Y15	VCC
Y16	VCC
Y17	VCC
Y18	VCC
Y19	VCC
Y20	VCC
Y21	IO142PPB3V3
Y22	IO134NDB3V2
Y23	IO138NDB3V3
Y24	IO140NDB3V3
Y25	IO140PDB3V3
Y26	IO136PPB3V2
Y27	IO141NDB3V3
Y28	IO135NDB3V2
Y29	IO131NDB3V2
Y30	IO133PDB3V2