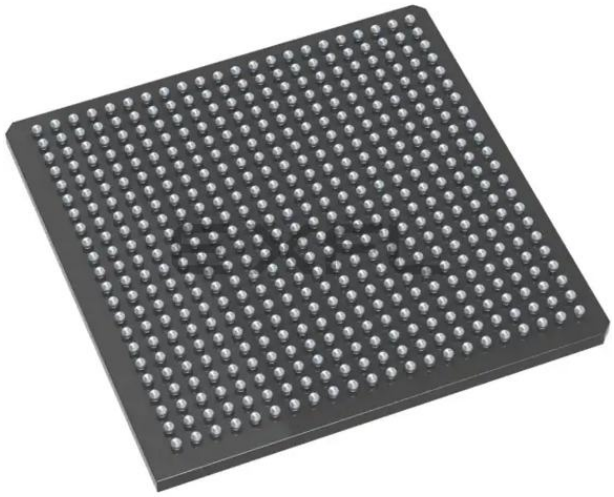

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 110592 |
| Number of I/O | 270 |
| Number of Gates | 600000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a3pe600-fg484 |

# 1 – ProASIC3E Device Family Overview

## General Description

ProASIC3E, the third-generation family of Microsemi flash FPGAs, offers performance, density, and features beyond those of the ProASIC PLUS® family. Nonvolatile flash technology gives ProASIC3E devices the advantage of being a secure, low power, single-chip solution that is Instant On. ProASIC3E is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

ProASIC3E devices offer 1 kbit of on-chip, programmable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on six integrated phase-locked loops (PLLs). ProASIC3E devices have up to three million system gates, supported with up to 504 kbits of true dual-port SRAM and up to 620 user I/Os.

Several ProASIC3E devices support the Cortex-M1 soft IP cores, and the ARM-Enabled devices have Microsemi ordering numbers that begin with M1A3PE.

### Flash Advantages

#### *Reduced Cost of Ownership*

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based ProASIC3E devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property (IP) cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The ProASIC3E family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the ProASIC3E family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/ communications, computing, and avionics markets.

#### *Security*

The nonvolatile, flash-based ProASIC3E devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. ProASIC3E devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

ProASIC3E devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of protection in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in ProASIC3E devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. ProASIC3E devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. ProASIC3E devices with AES-based security provide a high level of protection for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of the ProASIC3E family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The ProASIC3E family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. A ProASIC3E device provides the best available security for programmable logic designs.

**Table 2-4 • Overshoot and Undershoot Limits [1]**

| VCCI and VMV | Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2] | Maximum Overshoot/ Undershoot[2] |
|---|---|---|
| 2.7 V or less | 10% | 1.4 V |
| | 5% | 1.49 V |
| 3 V | 10% | 1.1 V |
| | 5% | 1.19 V |
| 3.3 V | 10% | 0.79 V |
| | 5% | 0.88 V |
| 3.6 V | 10% | 0.45 V |
| | 5% | 0.54 V |

*Notes:*

1. *Based on reliability requirements at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
3. *This table does not provide PCI overshoot/undershoot limits.*

## I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC®3E device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4.

There are five regions to consider during power-up.

ProASIC3E I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 on page 2-4).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

**VCCI Trip Point:**
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

**VCC Trip Point:**
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

## Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-11 on page 2-11.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-12 on page 2-11.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-12 on page 2-11. The calculation should be repeated for each clock domain defined in the design.

### Methodology

#### Total Power Consumption—$P_{TOTAL}$

$P_{TOTAL} = P_{STAT} + P_{DYN}$

$P_{STAT}$ is the total static power consumption.

$P_{DYN}$ is the total dynamic power consumption.

#### Total Static Power Consumption—$P_{STAT}$

$P_{STAT} = PDC1 + N_{INPUTS} * PDC2 + N_{OUTPUTS} * PDC3$

$N_{INPUTS}$ is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

#### Total Dynamic Power Consumption—$P_{DYN}$

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

#### Global Clock Contribution—$P_{CLOCK}$

$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S\text{-}CELL} * PAC4) * F_{CLK}$

$N_{SPINE}$ is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3E FPGA Fabric User's Guide*.

$N_{ROW}$ is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3E FPGA Fabric User's Guide*.

$F_{CLK}$ is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

#### Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-11 on page 2-11.

$F_{CLK}$ is the global clock signal frequency.

# User I/O Characteristics

## Timing Model

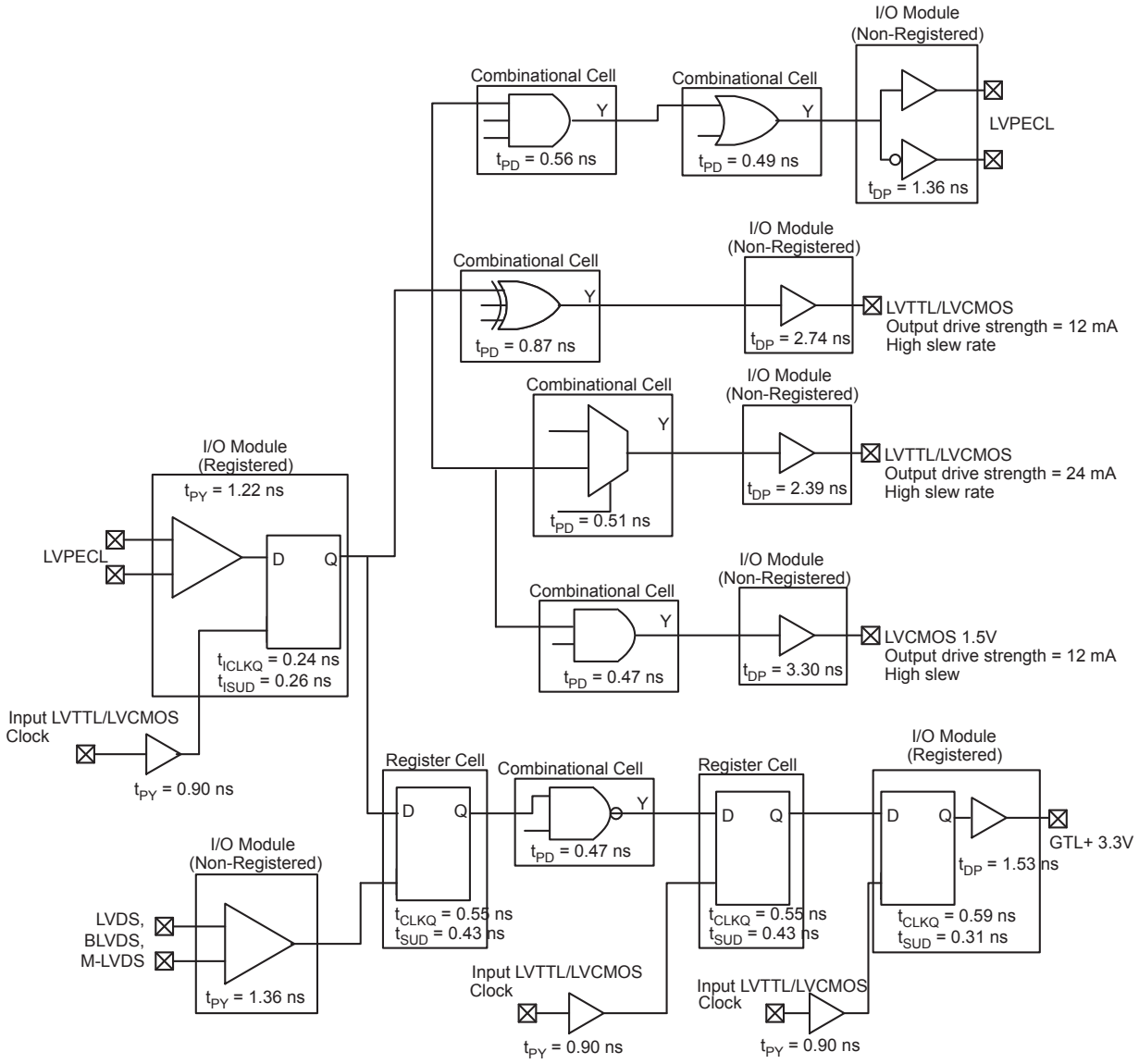


***Figure 2-2 •*** **Timing Model**
**Operating Conditions: –2 Speed, Commercial Temperature Range ($T_J$ = 70°C), Worst-Case VCC = 1.425 V**

### 1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

**Table 2-41 • Minimum and Maximum DC Input and Output Levels**

| 1.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.30 * VCCI | 0.7 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 16 | 13 | 10 | 10 |
| 4 mA | –0.3 | 0.30 * VCCI | 0.7 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 4 | 4 | 33 | 25 | 10 | 10 |
| 6 mA | –0.3 | 0.30 * VCCI | 0.7 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 6 | 6 | 39 | 32 | 10 | 10 |
| 8 mA | –0.3 | 0.30 * VCCI | 0.7 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 8 | 8 | 55 | 66 | 10 | 10 |
| 12 mA | –0.3 | 0.30 * VCCI | 0.7 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 | 55 | 66 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V< VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

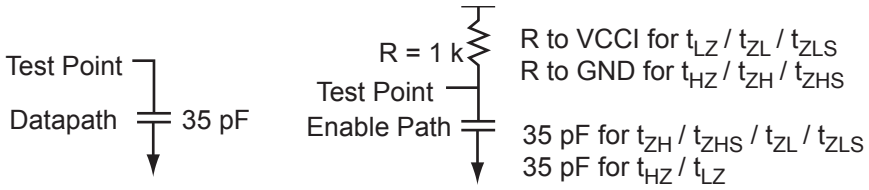


**Figure 2-10 • AC Loading**

**Table 2-42 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|
| 0 | 1.5 | 0.75 | – | 35 |

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

### 3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

**Table 2-45 • Minimum and Maximum DC Input and Output Levels**

| 3.3 V PCI/PCI-X | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| Per PCI specification | Per PCI curves | | | | | | | | | | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V< VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN< VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microsemi loadings for enable path characterization are described in Figure 2-11.

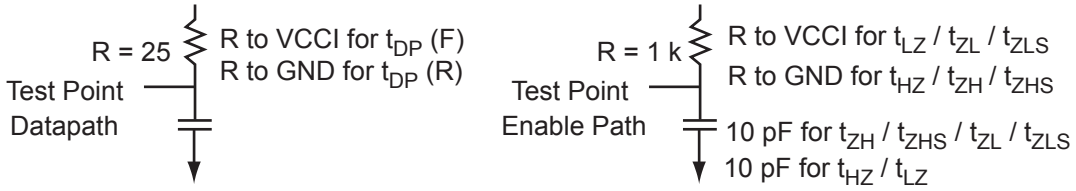


**Figure 2-11 • AC Loading**

AC loadings are defined per PCI/PCI-X specifications for the datapath; Microsemi loading for tristate is described in Table 2-46.

**Table 2-46 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|
| 0 | 3.3 | 0.285 * VCCI for $t_{DP(R)}$<br>0.615 * VCCI for $t_{DP(F)}$ | – | 10 |

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

### Timing Characteristics

**Table 2-47 • 3.3 V PCI/PCI-X**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 2.81 | 0.04 | 1.05 | 1.67 | 0.43 | 2.86 | 2.00 | 3.28 | 3.61 | 5.09 | 4.23 | ns |
| –1 | 0.56 | 2.39 | 0.04 | 0.89 | 1.42 | 0.36 | 2.43 | 1.70 | 2.79 | 3.07 | 4.33 | 3.60 | ns |
| –2 | 0.49 | 2.09 | 0.03 | 0.78 | 1.25 | 0.32 | 2.13 | 1.49 | 2.45 | 2.70 | 3.80 | 3.16 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

### SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-69 • Minimum and Maximum DC Input and Output Levels**

| SSTL2 Class II | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL | IIH |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[1] | Max. mA[1] | µA[2] | µA[2] |
| 18 mA | –0.3 | VREF – 0.2 | VREF + 0.2 | 3.6 | 0.35 | VCCI – 0.43 | 18 | 18 | 124 | 169 | 10 | 10 |

*Notes:*

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

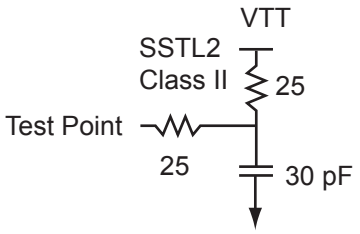


**Figure 2-19 • AC Loading**

**Table 2-70 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|---|
| VREF – 0.2 | VREF + 0.2 | 1.25 | 1.25 | 1.25 | 30 |

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

#### Timing Characteristics

**Table 2-71 • SSTL 2 Class II**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 0.66 | 2.17 | 0.04 | 1.33 | 0.43 | 2.21 | 1.77 | | | 4.44 | ns |
| –1 | 0.56 | 0.56 | 1.84 | 0.04 | 1.14 | 0.36 | 1.88 | 1.51 | | | 3.78 | ns |
| –2 | 0.49 | 0.49 | 1.62 | 0.03 | 1.00 | 0.32 | 1.65 | 1.32 | | | 3.32 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

## DDR Module Specifications

### *Input DDR Module*

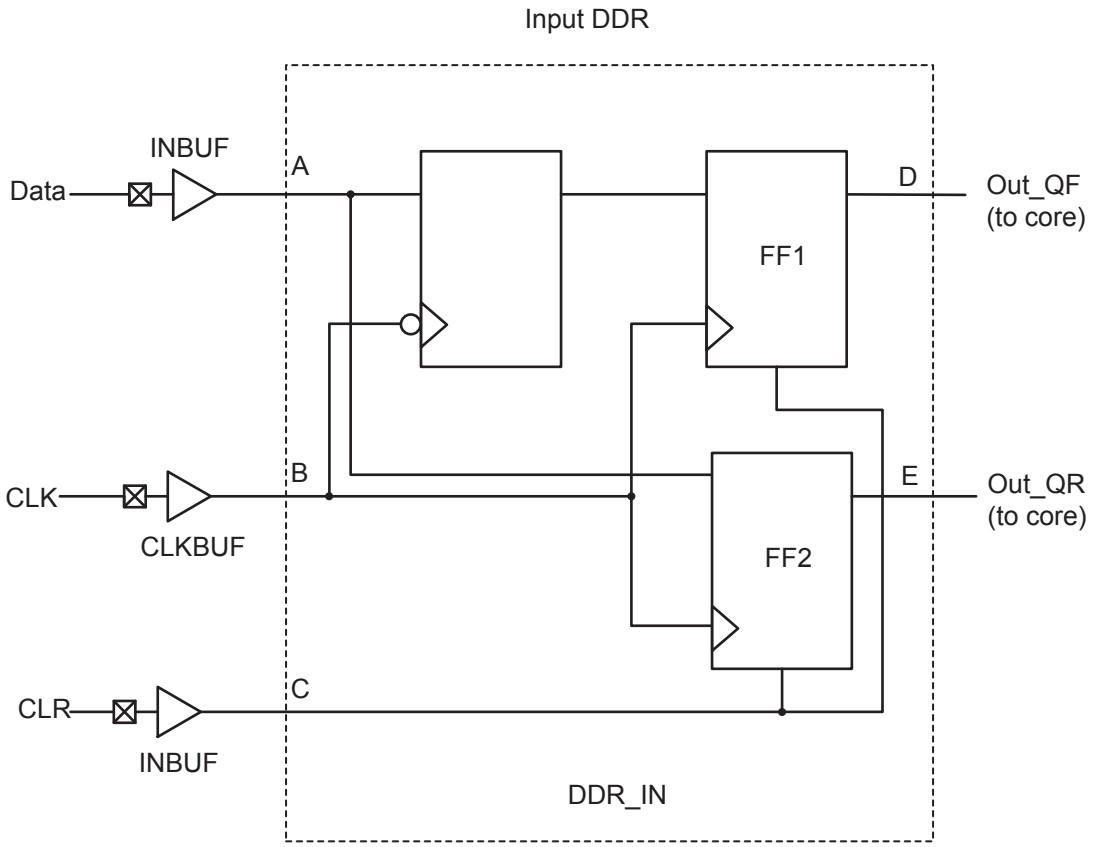


***Figure 2-30 •*** **Input DDR Timing Model**

***Table 2-89 •*** **Parameter Definitions**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|---|---|---|
| $t_{DDRICLKQ1}$ | Clock-to-Out Out_QR | B, D |
| $t_{DDRICLKQ2}$ | Clock-to-Out Out_QF | B, E |
| $t_{DDRISUD}$ | Data Setup Time of DDR input | A, B |
| $t_{DDRIHD}$ | Data Hold Time of DDR input | A, B |
| $t_{DDRICLR2Q1}$ | Clear-to-Out Out_QR | C, D |
| $t_{DDRICLR2Q2}$ | Clear-to-Out Out_QF | C, E |
| $t_{DDRIREMCLR}$ | Clear Removal | C, B |
| $t_{DDRIRECCLR}$ | Clear Recovery | C, B |

# VersaTile Characteristics

## VersaTile Specifications as a Combinatorial Module

The ProASIC3E library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO®/e, and ProASIC3/E Macro Library Guide*.

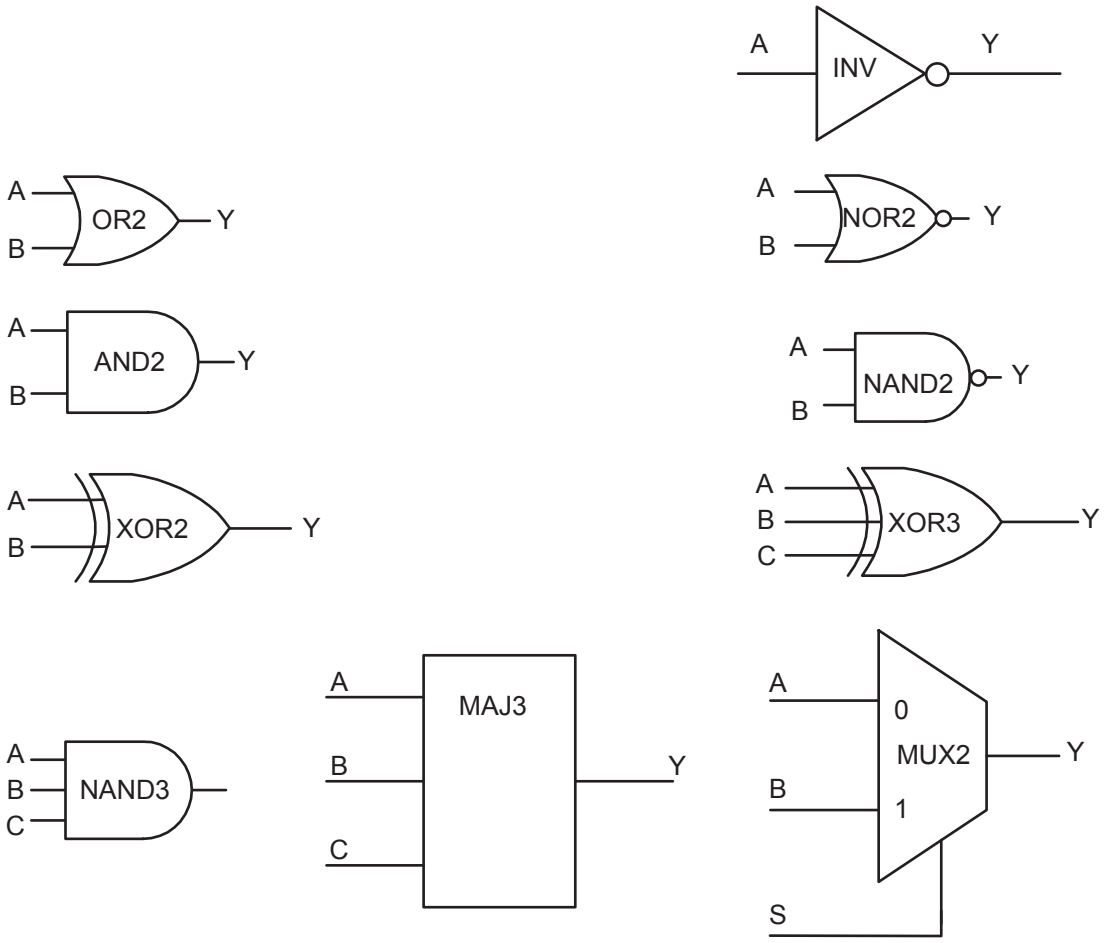


***Figure 2-34 •*** **Sample of Combinatorial Cells**

### Timing Characteristics

**Table 2-93 • Combinatorial Cell Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Combinatorial Cell | Equation | Parameter | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|---|
| INV | Y = !A | $t_{PD}$ | 0.40 | 0.46 | 0.54 | ns |
| AND2 | Y = A · B | $t_{PD}$ | 0.47 | 0.54 | 0.63 | ns |
| NAND2 | Y = !(A · B) | $t_{PD}$ | 0.47 | 0.54 | 0.63 | ns |
| OR2 | Y = A + B | $t_{PD}$ | 0.49 | 0.55 | 0.65 | ns |
| NOR2 | Y = !(A + B) | $t_{PD}$ | 0.49 | 0.55 | 0.65 | ns |
| XOR2 | Y = A ⊕ B | $t_{PD}$ | 0.74 | 0.84 | 0.99 | ns |
| MAJ3 | Y = MAJ(A , B, C) | $t_{PD}$ | 0.70 | 0.79 | 0.93 | ns |
| XOR3 | Y = A ⊕ B ⊕ C | $t_{PD}$ | 0.87 | 1.00 | 1.17 | ns |
| MUX2 | Y = A !S + B S | $t_{PD}$ | 0.51 | 0.58 | 0.68 | ns |
| AND3 | Y = A · B · C | $t_{PD}$ | 0.56 | 0.64 | 0.75 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

## VersaTile Specifications as a Sequential Module

The ProASIC3E library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.

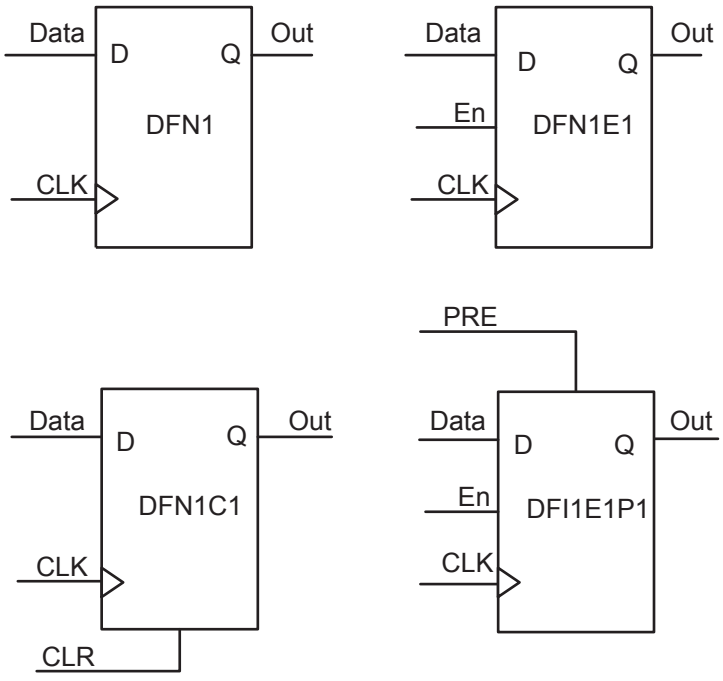


**Figure 2-36 • Sample of Sequential Cells**

## Timing Waveforms

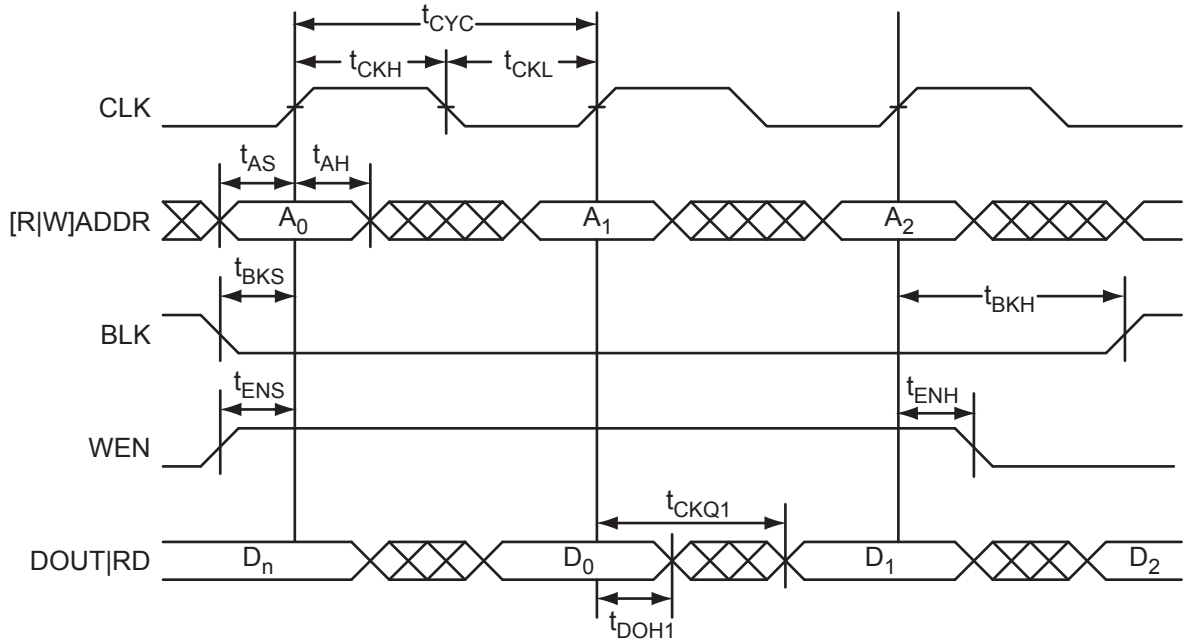


***Figure 2-41 •*** **RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.**

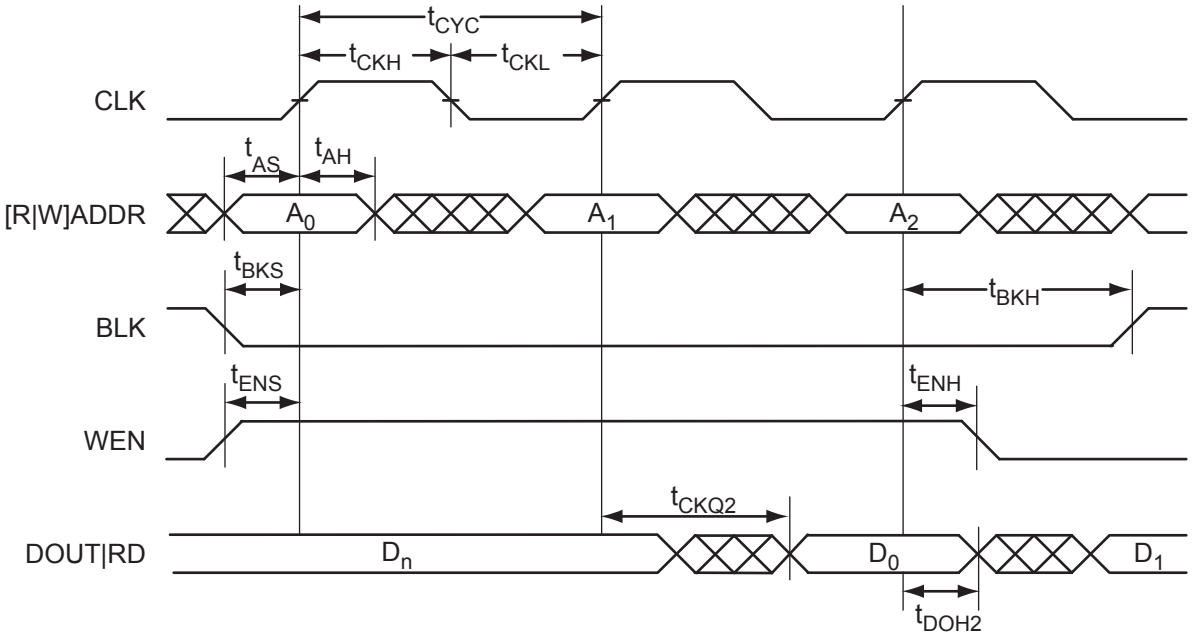


***Figure 2-42 •*** **RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.**

# 3 – Pin Descriptions and Packaging

## Supply Pins

**GND** **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

**GNDQ** **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

**VCC** **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

**VCCIBx** **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. In general, unused I/O banks should have their corresponding VCCIX pins tied to GND. If an output pad is terminated to ground through any resistor and if the corresponding VCCIX is left floating, then the leakage current to ground is ~ 0uA. However, if an output pad is terminated to ground through any resistor and the corresponding VCCIX grounded, then the leakage current to ground is ~ 3 uA. For unused banks the aforementioned behavior is to be taken into account while deciding if it’s better to float VCCIX of unused bank or tie it to GND.

**VMVx** **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

**VCCPLA/B/C/D/E/F** **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V.

When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *ProASIC3E FPGA Fabric User’s Guide* for a complete board solution for the PLL analog power supply and ground.

There are six VCCPLX pins on ProASIC3E devices.

**VCOMPLA/B/C/D/E/F** **PLL Ground**

Ground to analog PLL power supplies. When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There are six VCOMPL pins (PLL ground) on ProASIC3E devices.

| PQ208 | |
|---|---|
| Pin Number | A3PE1500 Function |
| 1 | GND |
| 2 | GNDQ |
| 3 | VMV7 |
| 4 | GAB2/IO220PSB7V3 |
| 5 | GAA2/IO221PDB7V3 |
| 6 | IO221NDB7V3 |
| 7 | GAC2/IO219PDB7V3 |
| 8 | IO219NDB7V3 |
| 9 | IO215PDB7V3 |
| 10 | IO215NDB7V3 |
| 11 | IO212PDB7V2 |
| 12 | IO212NDB7V2 |
| 13 | IO208PDB7V2 |
| 14 | IO208NDB7V2 |
| 15 | IO204PSB7V1 |
| 16 | VCC |
| 17 | GND |
| 18 | VCCIB7 |
| 19 | IO200PDB7V1 |
| 20 | IO200NDB7V1 |
| 21 | IO196PSB7V0 |
| 22 | GFC1/IO192PSB7V0 |
| 23 | GFB1/IO191PDB7V0 |
| 24 | GFB0/IO191NDB7V0 |
| 25 | VCOMPLF |
| 26 | GFA0/IO190NPB6V2 |
| 27 | VCCPLF |
| 28 | GFA1/IO190PPB6V2 |
| 29 | GND |
| 30 | GFA2/IO189PDB6V2 |
| 31 | IO189NDB6V2 |
| 32 | GFB2/IO188PPB6V2 |
| 33 | GFC2/IO187PPB6V2 |
| 34 | IO188NPB6V2 |
| 35 | IO187NPB6V2 |
| 36 | VCC |

| PQ208 | |
|---|---|
| Pin Number | A3PE1500 Function |
| 37 | IO184PDB6V2 |
| 38 | IO184NDB6V2 |
| 39 | IO180PSB6V1 |
| 40 | VCCIB6 |
| 41 | GND |
| 42 | IO176PDB6V1 |
| 43 | IO176NDB6V1 |
| 44 | GEC1/IO169PDB6V0 |
| 45 | GEC0/IO169NDB6V0 |
| 46 | GEB1/IO168PPB6V0 |
| 47 | GEA1/IO167PPB6V0 |
| 48 | GEB0/IO168NPB6V0 |
| 49 | GEA0/IO167NPB6V0 |
| 50 | VMV6 |
| 51 | GNDQ |
| 52 | GND |
| 53 | VMV5 |
| 54 | GNDQ |
| 55 | IO166NDB5V3 |
| 56 | GEA2/IO166PDB5V3 |
| 57 | IO165NDB5V3 |
| 58 | GEB2/IO165PDB5V3 |
| 59 | IO164NDB5V3 |
| 60 | GEC2/IO164PDB5V3 |
| 61 | IO163PSB5V3 |
| 62 | VCCIB5 |
| 63 | IO161PSB5V3 |
| 64 | IO157NDB5V2 |
| 65 | GND |
| 66 | IO157PDB5V2 |
| 67 | IO153NDB5V2 |
| 68 | IO153PDB5V2 |
| 69 | IO149NDB5V1 |
| 70 | IO149PDB5V1 |
| 71 | VCC |
| 72 | VCCIB5 |

| PQ208 | |
|---|---|
| Pin Number | A3PE1500 Function |
| 73 | IO145NDB5V1 |
| 74 | IO145PDB5V1 |
| 75 | IO143NDB5V1 |
| 76 | IO143PDB5V1 |
| 77 | IO137NDB5V0 |
| 78 | IO137PDB5V0 |
| 79 | IO135NDB5V0 |
| 80 | IO135PDB5V0 |
| 81 | GND |
| 82 | IO131NDB4V2 |
| 83 | IO131PDB4V2 |
| 84 | IO129NDB4V2 |
| 85 | IO129PDB4V2 |
| 86 | IO127NDB4V2 |
| 87 | IO127PDB4V2 |
| 88 | VCC |
| 89 | VCCIB4 |
| 90 | IO121NDB4V1 |
| 91 | IO121PDB4V1 |
| 92 | IO119NDB4V1 |
| 93 | IO119PDB4V1 |
| 94 | IO113NDB4V0 |
| 95 | GDC2/IO113PDB4V0 |
| 96 | IO112NDB4V0 |
| 97 | GND |
| 98 | GDB2/IO112PDB4V0 |
| 99 | GDA2/IO111PSB4V0 |
| 100 | GNDQ |
| 101 | TCK |
| 102 | TDI |
| 103 | TMS |
| 104 | VMV4 |
| 105 | GND |
| 106 | VPUMP |
| 107 | GNDQ |
| 108 | TDO |

| FG484 | |
|---|---|
| Pin Number | A3PE600 Function |
| H19 | IO41PDB2V0 |
| H20 | VCC |
| H21 | NC |
| H22 | NC |
| J1 | IO123NDB7V0 |
| J2 | IO123PDB7V0 |
| J3 | NC |
| J4 | IO124PDB7V0 |
| J5 | IO125PDB7V0 |
| J6 | IO126PDB7V0 |
| J7 | IO130NDB7V1 |
| J8 | VCCIB7 |
| J9 | GND |
| J10 | VCC |
| J11 | VCC |
| J12 | VCC |
| J13 | VCC |
| J14 | GND |
| J15 | VCCIB2 |
| J16 | IO38NDB2V0 |
| J17 | IO40NDB2V0 |
| J18 | IO40PDB2V0 |
| J19 | IO45PPB2V1 |
| J20 | NC |
| J21 | IO48PDB2V1 |
| J22 | IO46PDB2V1 |
| K1 | IO121NDB7V0 |
| K2 | IO121PDB7V0 |
| K3 | NC |
| K4 | IO124NDB7V0 |
| K5 | IO125NDB7V0 |
| K6 | IO126NDB7V0 |
| K7 | GFC1/IO120PPB7V0 |
| K8 | VCCIB7 |
| K9 | VCC |
| K10 | GND |

| FG484 | |
|---|---|
| Pin Number | A3PE600 Function |
| K11 | GND |
| K12 | GND |
| K13 | GND |
| K14 | VCC |
| K15 | VCCIB2 |
| K16 | GCC1/IO50PPB2V1 |
| K17 | IO44NDB2V1 |
| K18 | IO44PDB2V1 |
| K19 | IO49NPB2V1 |
| K20 | IO45NPB2V1 |
| K21 | IO48NDB2V1 |
| K22 | IO46NDB2V1 |
| L1 | NC |
| L2 | IO122PDB7V0 |
| L3 | IO122NDB7V0 |
| L4 | GFB0/IO119NPB7V0 |
| L5 | GFA0/IO118NDB6V1 |
| L6 | GFB1/IO119PPB7V0 |
| L7 | VCOMPLF |
| L8 | GFC0/IO120NPB7V0 |
| L9 | VCC |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L13 | GND |
| L14 | VCC |
| L15 | GCC0/IO50NPB2V1 |
| L16 | GCB1/IO51PPB2V1 |
| L17 | GCA0/IO52NPB3V0 |
| L18 | VCOMPLC |
| L19 | GCB0/IO51NPB2V1 |
| L20 | IO49PPB2V1 |
| L21 | IO47NDB2V1 |
| L22 | IO47PDB2V1 |
| M1 | NC |
| M2 | IO114NPB6V1 |

| FG484 | |
|---|---|
| Pin Number | A3PE600 Function |
| M3 | IO117NDB6V1 |
| M4 | GFA2/IO117PDB6V1 |
| M5 | GFA1/IO118PDB6V1 |
| M6 | VCCPLF |
| M7 | IO116NDB6V1 |
| M8 | GFB2/IO116PDB6V1 |
| M9 | VCC |
| M10 | GND |
| M11 | GND |
| M12 | GND |
| M13 | GND |
| M14 | VCC |
| M15 | GCB2/IO54PPB3V0 |
| M16 | GCA1/IO52PPB3V0 |
| M17 | GCC2/IO55PPB3V0 |
| M18 | VCCPLC |
| M19 | GCA2/IO53PDB3V0 |
| M20 | IO53NDB3V0 |
| M21 | IO56PDB3V0 |
| M22 | NC |
| N1 | IO114PPB6V1 |
| N2 | IO111NDB6V1 |
| N3 | NC |
| N4 | GFC2/IO115PPB6V1 |
| N5 | IO113PPB6V1 |
| N6 | IO112PDB6V1 |
| N7 | IO112NDB6V1 |
| N8 | VCCIB6 |
| N9 | VCC |
| N10 | GND |
| N11 | GND |
| N12 | GND |
| N13 | GND |
| N14 | VCC |
| N15 | VCCIB3 |
| N16 | IO54NPB3V0 |

| FG484 | |
|---|---|
| Pin Number | A3PE1500 Function |
| A1 | GND |
| A2 | GND |
| A3 | VCCIB0 |
| A4 | IO05NDB0V0 |
| A5 | IO05PDB0V0 |
| A6 | IO11NDB0V1 |
| A7 | IO11PDB0V1 |
| A8 | IO15PDB0V1 |
| A9 | IO17PDB0V2 |
| A10 | IO27NDB0V3 |
| A11 | IO27PDB0V3 |
| A12 | IO32PDB1V0 |
| A13 | IO43PDB1V1 |
| A14 | IO47NDB1V1 |
| A15 | IO47PDB1V1 |
| A16 | IO51NDB1V2 |
| A17 | IO51PDB1V2 |
| A18 | IO54NDB1V3 |
| A19 | NC |
| A20 | VCCIB1 |
| A21 | GND |
| A22 | GND |
| AA1 | GND |
| AA2 | VCCIB6 |
| AA3 | NC |
| AA4 | IO161PDB5V3 |
| AA5 | IO155NDB5V2 |
| AA6 | IO155PDB5V2 |
| AA7 | IO154NDB5V2 |
| AA8 | IO154PDB5V2 |
| AA9 | IO143PDB5V1 |
| AA10 | IO143NDB5V1 |
| AA11 | IO131PPB4V2 |
| AA12 | IO129NDB4V2 |
| AA13 | IO129PDB4V2 |
| AA14 | NC |

| FG484 | |
|---|---|
| Pin Number | A3PE1500 Function |
| AA15 | NC |
| AA16 | IO117NDB4V0 |
| AA17 | IO117PDB4V0 |
| AA18 | IO115NDB4V0 |
| AA19 | IO115PDB4V0 |
| AA20 | NC |
| AA21 | VCCIB3 |
| AA22 | GND |
| AB1 | GND |
| AB2 | GND |
| AB3 | VCCIB5 |
| AB4 | IO159NDB5V3 |
| AB5 | IO159PDB5V3 |
| AB6 | IO149NDB5V1 |
| AB7 | IO149PDB5V1 |
| AB8 | IO138NDB5V0 |
| AB9 | IO138PDB5V0 |
| AB10 | NC |
| AB11 | NC |
| AB12 | IO127NDB4V2 |
| AB13 | IO127PDB4V2 |
| AB14 | IO125NDB4V1 |
| AB15 | IO125PDB4V1 |
| AB16 | IO122NDB4V1 |
| AB17 | IO122PDB4V1 |
| AB18 | NC |
| AB19 | NC |
| AB20 | VCCIB4 |
| AB21 | GND |
| AB22 | GND |
| B1 | GND |
| B2 | VCCIB7 |
| B3 | NC |
| B4 | IO03NDB0V0 |
| B5 | IO03PDB0V0 |
| B6 | IO10NDB0V1 |

| FG484 | |
|---|---|
| Pin Number | A3PE1500 Function |
| B7 | IO10PDB0V1 |
| B8 | IO15NDB0V1 |
| B9 | IO17NDB0V2 |
| B10 | IO20PDB0V2 |
| B11 | IO29PDB0V3 |
| B12 | IO32NDB1V0 |
| B13 | IO43NDB1V1 |
| B14 | NC |
| B15 | NC |
| B16 | IO53NDB1V2 |
| B17 | IO53PDB1V2 |
| B18 | IO54PDB1V3 |
| B19 | NC |
| B20 | NC |
| B21 | VCCIB2 |
| B22 | GND |
| C1 | VCCIB7 |
| C2 | NC |
| C3 | NC |
| C4 | NC |
| C5 | GND |
| C6 | IO07NDB0V0 |
| C7 | IO07PDB0V0 |
| C8 | VCC |
| C9 | VCC |
| C10 | IO20NDB0V2 |
| C11 | IO29NDB0V3 |
| C12 | NC |
| C13 | NC |
| C14 | VCC |
| C15 | VCC |
| C16 | NC |
| C17 | NC |
| C18 | GND |
| C19 | NC |
| C20 | NC |

| FG484 | |
|---|---|
| **Pin Number** | **A3PE1500 Function** |
| V15 | IO112NDB4V0 |
| V16 | GDB2/IO112PDB4V0 |
| V17 | TDI |
| V18 | GNDQ |
| V19 | TDO |
| V20 | GND |
| V21 | NC |
| V22 | IO105NDB3V2 |
| W1 | NC |
| W2 | NC |
| W3 | NC |
| W4 | GND |
| W5 | IO165NDB5V3 |
| W6 | GEB2/IO165PDB5V3 |
| W7 | IO164NDB5V3 |
| W8 | IO153NDB5V2 |
| W9 | IO153PDB5V2 |
| W10 | IO147NDB5V1 |
| W11 | IO133NDB4V2 |
| W12 | IO130NDB4V2 |
| W13 | IO130PDB4V2 |
| W14 | IO113NDB4V0 |
| W15 | GDC2/IO113PDB4V0 |
| W16 | IO111NDB4V0 |
| W17 | GDA2/IO111PDB4V0 |
| W18 | TMS |
| W19 | GND |
| W20 | NC |
| W21 | NC |
| W22 | NC |
| Y1 | VCCIB6 |
| Y2 | NC |
| Y3 | NC |
| Y4 | IO161NDB5V3 |
| Y5 | GND |
| Y6 | IO163NDB5V3 |

| FG484 | |
|---|---|
| **Pin Number** | **A3PE1500 Function** |
| Y7 | IO163PDB5V3 |
| Y8 | VCC |
| Y9 | VCC |
| Y10 | IO147PDB5V1 |
| Y11 | IO133PDB4V2 |
| Y12 | IO131NPB4V2 |
| Y13 | NC |
| Y14 | VCC |
| Y15 | VCC |
| Y16 | NC |
| Y17 | NC |
| Y18 | GND |
| Y19 | NC |
| Y20 | NC |
| Y21 | NC |
| Y22 | VCCIB3 |

| Revision | Changes | Page |
|---|---|---|
| Revision 10 (continued) | "TBD" for 3.3 V LVCMOS Wide Range in Table 2-19 • I/O Output Buffer Maximum Resistances[1] and Table 2-21 • I/O Short Currents IOSH/IOSL was replaced by "Same as regular 3.3 V LVCMOS" (SAR 33853).<br>3.3 V LVCMOS Wide Range information was separated from regular 3.3 V LVCMOS and placed into its own new section, "3.3 V LVCMOS Wide Range". Values of IOSH and IOSL were added in Table 2-29 • Minimum and Maximum DC Input and Output Levels (SAR 33853). | 2-20, 2-27 |
| | The formulas in the table notes for Table 2-20 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 34755). | 2-21 |
| | The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34889). | 2-24 |
| | The titles and subtitles for Table 2-31 • 3.3 V LVCMOS Wide Range High Slew and Table 2-32 • 3.3 V LVCMOS Wide Range Low Slew were corrected (SAR 37227). | 2-28, 2-29 |
| | The following notes were removed from Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels (SAR 34812):<br>±5%<br>Differential input voltage = ±350 mV | 2-50 |
| | Minimum pulse width High and Low values were added to the tables in the "Global Tree Timing Characteristics" section. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 36957). | 2-68 |
| | A note was added to Table 2-98 • ProASIC3E CCC/PLL Specification indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34824). | 2-70 |
| | The following figures were deleted. Reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 34872).<br>Figure 2-44 • Write Access after Write onto Same Address<br>Figure 2-45 • Read Access after Write onto Same Address<br>Figure 2-46 • Write Access after Read onto Same Address<br>The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-49 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35750). | 2-74, 2-75, 2-79, 2-82 |
| | The "Pin Descriptions and Packaging" chapter is new (SAR 34771). | 3-1 |
| | Package names used in the "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 34771). | 4-1 |
| | Pin E6 for the FG256 package was corrected from VvB0 to VCCIB0 (SARs 30364, 31597, 26243). | 4-9 |
| July 2010 | The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "ProASIC3E Device Status" table on page II indicates the status for each device in the device family. | N/A |

| Revision | Changes | Page |
|---|---|---|
| **Revision 9 (Aug 2009)**<br>Product Brief v1.2 | All references to speed grade –F have been removed from this document. | N/A |
| | The "Pro I/Os with Advanced I/O Standards" section was revised to add definitions of hot-swap and cold-sparing. | 1-6 |
| DC and Switching Characteristics v1.3 | 3.3 V LVCMOS and 1.2 V LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained 3.3 V LVCMOS and 1.2 V LVCMOS data. | N/A |
| | IIL and IIH input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables. | N/A |
| | –F was removed from the datasheet. The speed grade is no longer supported. | N/A |
| | In the Table 2-2 • Recommended Operating Conditions [1] "3.0 V DC supply voltage" and note 4 are new. | 2-2 |
| | The Table 2-4 • Overshoot and Undershoot Limits [1] table was updated. | 2-3 |
| | The Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays table was updated. | 2-5 |
| | There are new parameters and data was updated in the Table 2-99 • RAM4K9 table. | 2-76 |
| | There are new parameters and data was updated in the Table 2-100 • RAM512X18 table. | 2-77 |
| **Revision 8 (Feb 2008)**<br>Product Brief v1.1 | Table 1-2 • ProASIC3E FPGAs Package Sizes Dimensions is new. | 1-II |
| **Revision 7 (Jun 2008)**<br>DC and Switching Characteristics v1.2 | The title of Table 2-4 • Overshoot and Undershoot Limits [1] was modified to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted. | 2-3 |
| | Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels was updated. | 2-50 |
| **Revision 6 (Jun 2008)** | The A3PE600 "FG484" table was missing G22. The pin and its function were added to the table. | 4-27 |
| **Revision 5 (Jun 2008)**<br>Packaging v1.4 | The naming conventions changed for the following pins in the "FG484" for the A3PE600:<br>**Pin Number** — **New Function Name**<br>J19 — IO45PPB2V1<br>K20 — IO45NPB2V1<br>M2 — IO114NPB6V1<br>N1 — IO114PPB6V1<br>N4 — GFC2/IO115PPB6V1<br>P3 — IO115NPB6V1 | 4-22 |
| **Revision 4 (Apr 2008)**<br>Product Brief v1.0 | The product brief portion of the datasheet was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview. | N/A |
| Packaging v1.3 | The "FG324" package diagram was replaced. | 4-12 |

| Revision | Changes | Page |
|---|---|---|
| v2.1 (continued) | The words "ambient temperature" were added to the temperature range in the "Temperature Grade Offerings", "Speed Grade and Temperature Grade Matrix", and "Speed Grade and Temperature Grade Matrix" sections. | 1-I |
| | The "Clock Conditioning Circuit (CCC) and PLL" section was updated. | 1-I |
| | The caption "Main (chip)" in Figure 2-9 • Overview of Automotive ProASIC3 VersaNet Global Network was changed to "Chip (main)." | 2-9 |
| | The $T_J$ parameter in Table 3-2 • Recommended Operating Conditions was changed to $T_A$, ambient temperature, and table notes 4–6 were added. | 3-2 |
| | The "PLL Macro" section was updated to add information on the VCO and PLL outputs during power-up. | 2-15 |
| v2.0 (April 2007) | In the "Temperature Grade Offerings" section, Ambient was deleted. | iii |
| | Ambient was deleted from "Temperature Grade Offerings". | iii |
| | Ambient was deleted from the "Speed Grade and Temperature Grade Matrix". | iv |
| | The "PLL Macro" section was updated to include power-up information. | 2-15 |
| | Table 2-13 • ProASIC3E CCC/PLL Specification was updated. | 2-30 |
| | Figure 2-19 • Peak-to-Peak Jitter Definition is new. | 2-18 |
| | The "SRAM and FIFO" section was updated with operation and timing requirement information. | 2-21 |
| | The "RESET" section was updated with read and write information. | 2-25 |
| | The "RESET" section was updated with read and write information. | 2-25 |
| | The "Introduction" in the "Advanced I/Os" section was updated to include information on input and output buffers being disabled. | 2-28 |
| | In the Table 2-15 • Levels of Hot-Swap Support, the ProASIC3 compliance descriptions were updated for levels 3 and 4. | 2-34 |
| | Table 2-45 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3E Devices was updated. | 2-64 |
| | Notes 3, 4, and 5 were added to Table 2-17 • Comparison Table for 5 V–Compliant Receiver Scheme. 5 x 52.72 was changed to 52.7 and the Maximum current was updated from 4 x 52.7 to 5 x 52.7. | 2-40 |
| | The "VCCPLF PLL Supply Voltage" section was updated. | 2-50 |
| | The "VPUMP Programming Supply Voltage" section was updated. | 2-50 |
| | The "GL Globals" section was updated to include information about direct input into quadrant clocks. | 2-51 |
| | VJTAG was deleted from the "TCK Test Clock" section. | 2-51 |
| | In Table 2-22 • Recommended Tie-Off Values for the TCK and TRST Pins, TSK was changed to TCK in note 2. Note 3 was also updated. | 2-51 |
| | Ambient was deleted from Table 3-2 • Recommended Operating Conditions. VPUMP programming mode was changed from "3.0 to 3.6" to "3.15 to 3.45". | 3-2 |
| | Note 3 is new in Table 3-4 • Overshoot and Undershoot Limits (as measured on quiet I/Os). | 3-2 |
| | In EQ 3-2, 150 was changed to 110 and the result changed to 5.88. | 3-5 |

| Revision | Changes | Page |
|---|---|---|
| Advance v0.3 (continued) | The "Methodology" section was updated. | 3-9 |
| | The A3PE3000 "208-Pin PQFP" pin table was updated. | 4-6 |