Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	444
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3pe1500-1fg676i

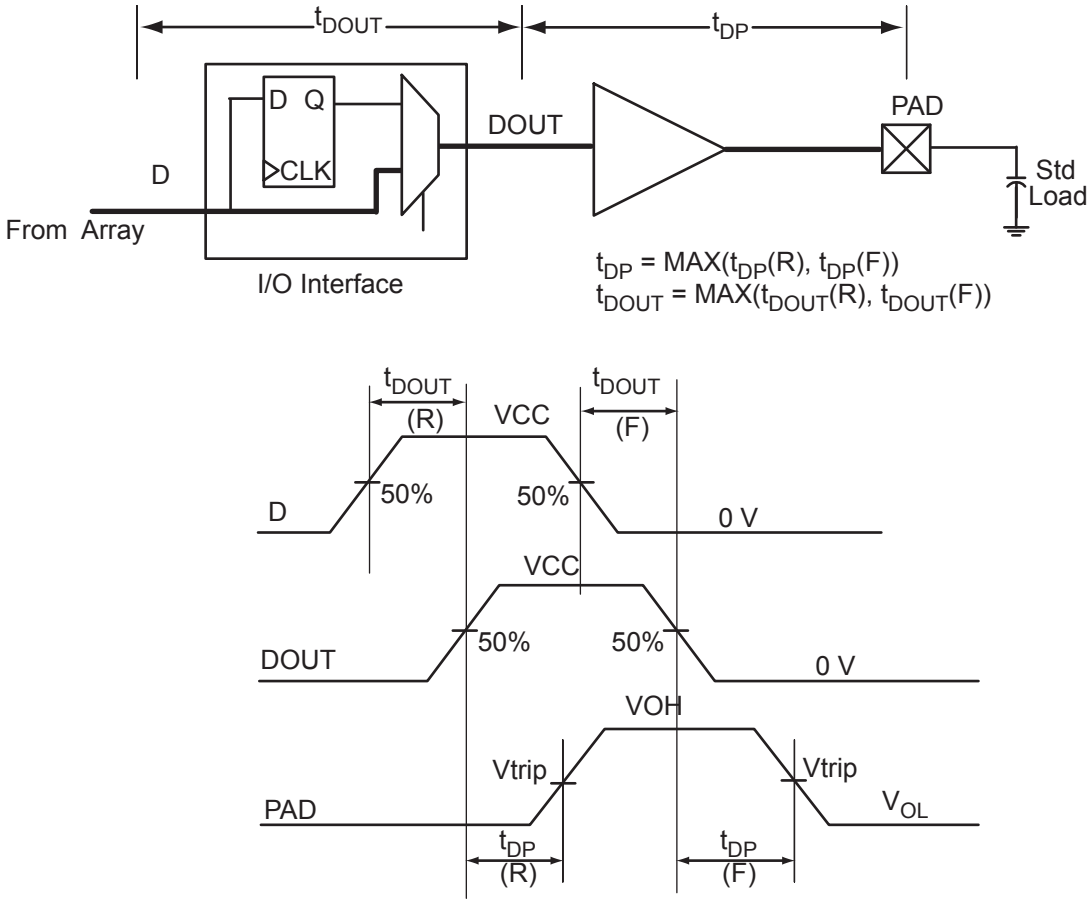


Figure 2-4 • **Output Buffer Model and Delays (example)**

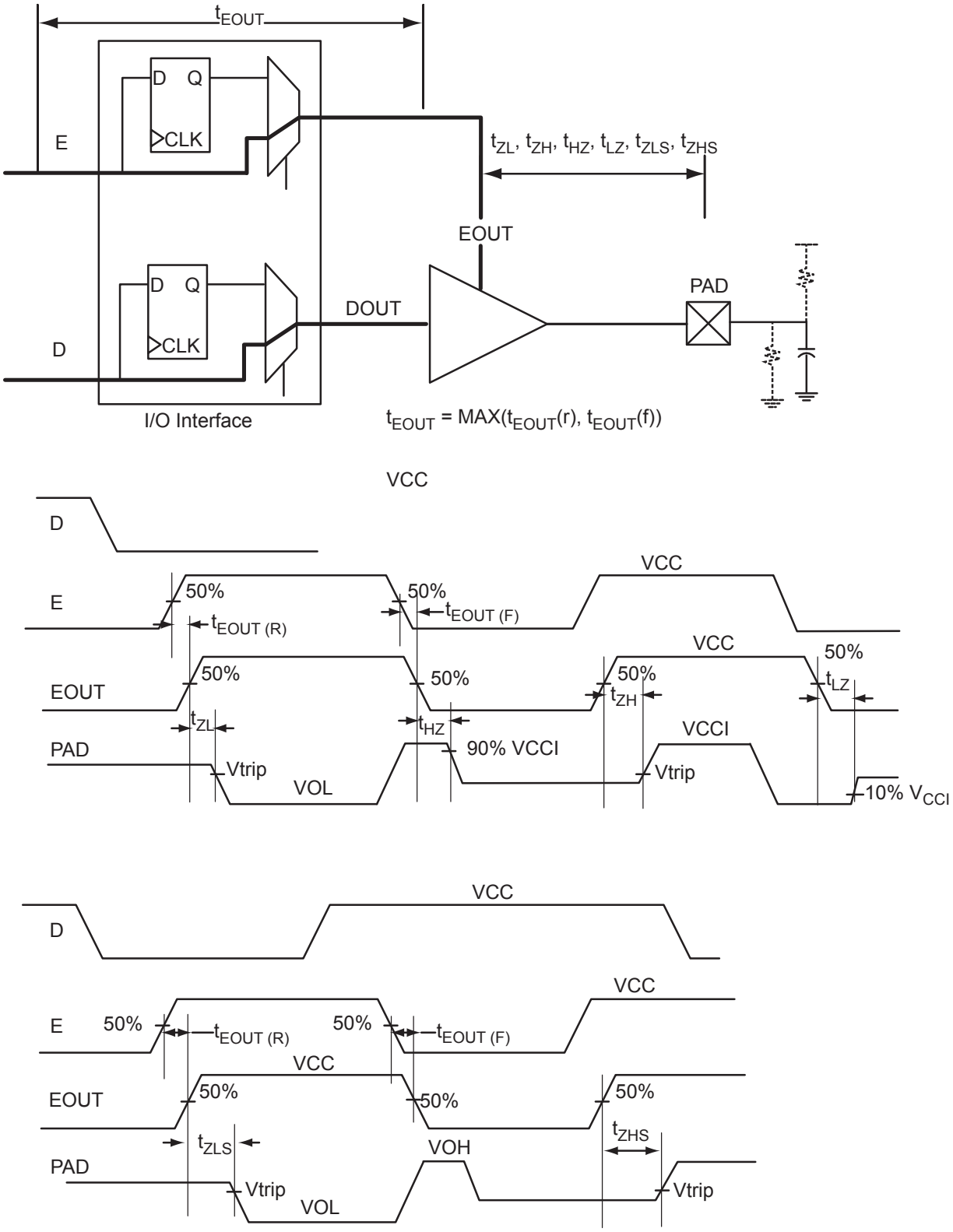


Figure 2-5 • **Tristate Output Buffer Timing Model and Delays (example)**

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-33 • Minimum and Maximum DC Input and Output Levels

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max., V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

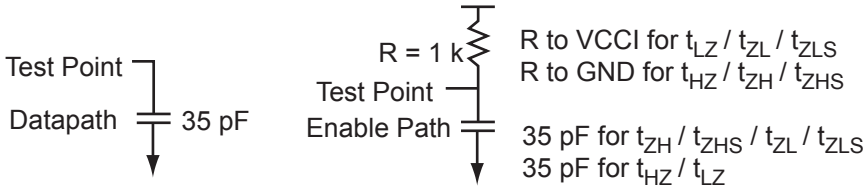


Figure 2-8 • AC Loading

Table 2-34 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-39 • 1.8 V LVCMOS High Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	12.10	0.04	1.45	1.91	0.43	9.59	12.10	2.78	1.64	11.83	14.34	ns
	–1	0.56	10.30	0.04	1.23	1.62	0.36	8.16	10.30	2.37	1.39	10.06	12.20	ns
	–2	0.49	9.04	0.03	1.08	1.42	0.32	7.16	9.04	2.08	1.22	8.83	10.71	ns
4 mA	Std.	0.66	7.05	0.04	1.45	1.91	0.43	6.20	7.05	3.25	2.86	8.44	9.29	ns
	–1	0.56	6.00	0.04	1.23	1.62	0.36	5.28	6.00	2.76	2.44	7.18	7.90	ns
	–2	0.49	5.27	0.03	1.08	1.42	0.32	4.63	5.27	2.43	2.14	6.30	6.94	ns
6 mA	Std.	0.66	4.52	0.04	1.45	1.91	0.43	4.47	4.52	3.57	3.47	6.70	6.76	ns
	–1	0.56	3.85	0.04	1.23	1.62	0.36	3.80	3.85	3.04	2.95	5.70	5.75	ns
	–2	0.49	3.38	0.03	1.08	1.42	0.32	3.33	3.38	2.66	2.59	5.00	5.05	ns
8 mA	Std.	0.66	4.12	0.04	1.45	1.91	0.43	4.20	3.99	3.63	3.62	6.43	6.23	ns
	–1	0.56	3.51	0.04	1.23	1.62	0.36	3.57	3.40	3.09	3.08	5.47	5.30	ns
	–2	0.49	3.08	0.03	1.08	1.42	0.32	3.14	2.98	2.71	2.71	4.81	4.65	ns
12 mA	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	–1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	–2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns
16 mA	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	–1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	–2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-41 • Minimum and Maximum DC Input and Output Levels

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10
6 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	6	6	39	32	10	10
8 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	8	8	55	66	10	10
12 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12	55	66	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V< VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

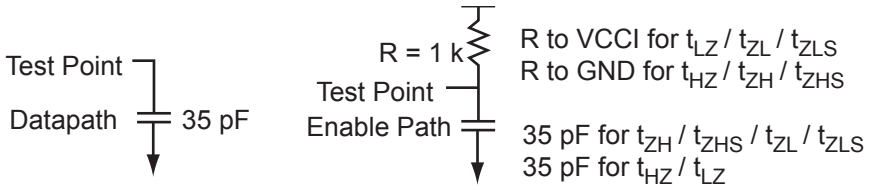


Figure 2-10 • AC Loading

Table 2-42 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	1.5	0.75	–	35

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-45 • Minimum and Maximum DC Input and Output Levels

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
Per PCI specification	Per PCI curves										10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V< VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN< VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microsemi loadings for enable path characterization are described in Figure 2-11.

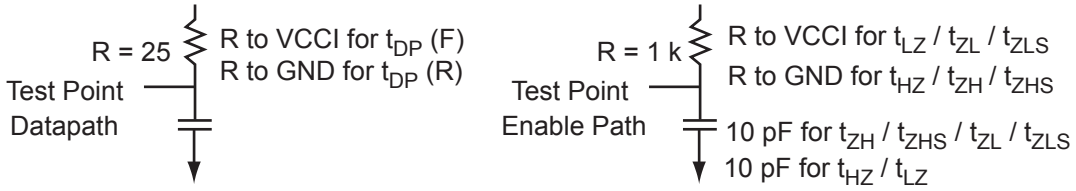


Figure 2-11 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the datapath; Microsemi loading for tristate is described in Table 2-46.

Table 2-46 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	3.3	0.285 * VCCI for $t_{DP(R)}$ 0.615 * VCCI for $t_{DP(F)}$	–	10

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-47 • 3.3 V PCI/PCI-X
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.81	0.04	1.05	1.67	0.43	2.86	2.00	3.28	3.61	5.09	4.23	ns
–1	0.56	2.39	0.04	0.89	1.42	0.36	2.43	1.70	2.79	3.07	4.33	3.60	ns
–2	0.49	2.09	0.03	0.78	1.25	0.32	2.13	1.49	2.45	2.70	3.80	3.16	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL[1]	Output Lower Current	0.65	0.91	1.16	mA
IOH[1]	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
IIH[2]	Input High Leakage Current			10	µA
IIL[2]	Input Low Leakage Current			10	µA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage [2]	100	350		mV

Notes:

1. *IOL/IOH defined by VODIFF/(Resistor Network).*
2. *Currents are measured at 85°C junction temperature.*

Table 2-79 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)
1.075	1.325	Cross point	–

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Output Enable Register

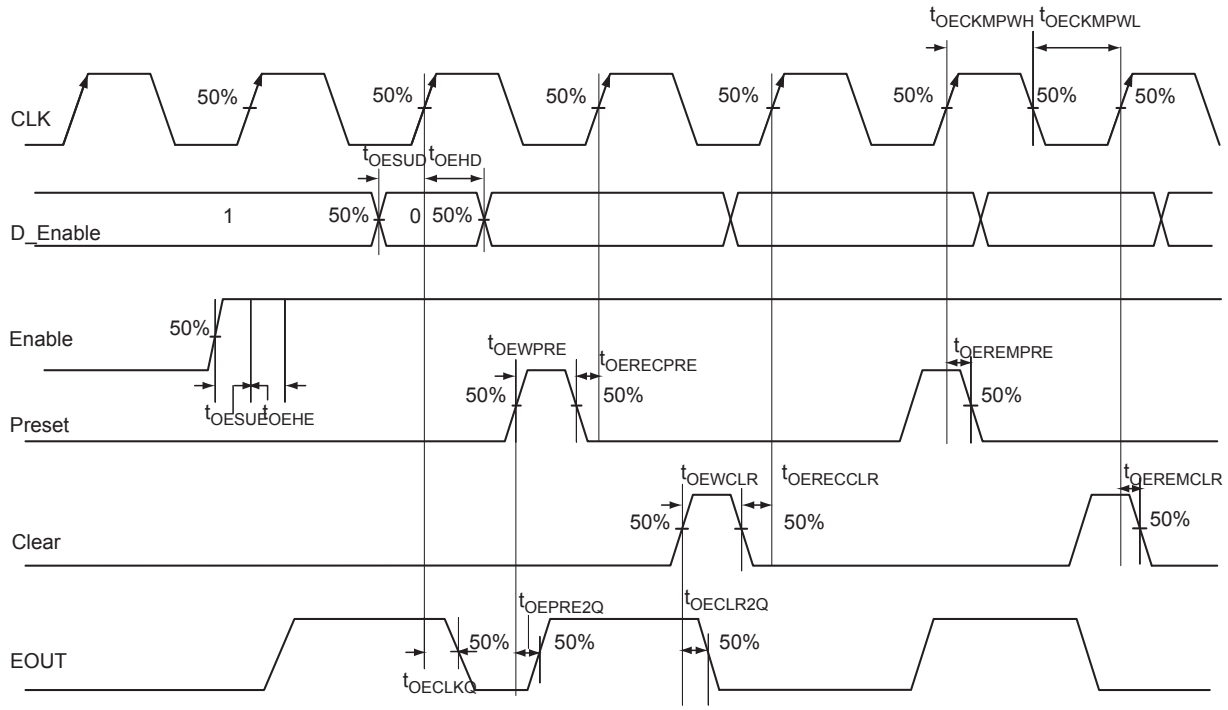


Figure 2-29 • **Output Enable Register Timing Diagram**

Timing Characteristics

Table 2-88 • **Output Enable Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.59	0.67	0.79	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.31	0.36	0.42	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.44	0.50	0.58	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.67	0.76	0.89	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.67	0.76	0.89	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.22	0.25	0.30	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.22	0.25	0.30	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.32	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Table 2-100 • RAM512X18
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.28	0.33	ns
t_{AH}	Address hold time	0.00	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.18	0.20	0.24	ns
t_{ENH}	REN, WEN hold time	0.06	0.07	0.08	ns
t_{DS}	Input data (WD) setup time	0.18	0.21	0.25	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	2.16	2.46	2.89	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	0.90	1.02	1.20	ns
t_{C2CRWH} [1]	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.50	0.43	0.38	ns
t_{C2CWRH} [1]	Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge	0.59	0.50	0.44	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to data out Low on RD (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.21	0.24	0.29	ns
t_{CYC}	Clock cycle time	3.23	3.68	4.32	ns
F_{MAX}	Maximum frequency	310	272	231	MHz

Notes:

1. *For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

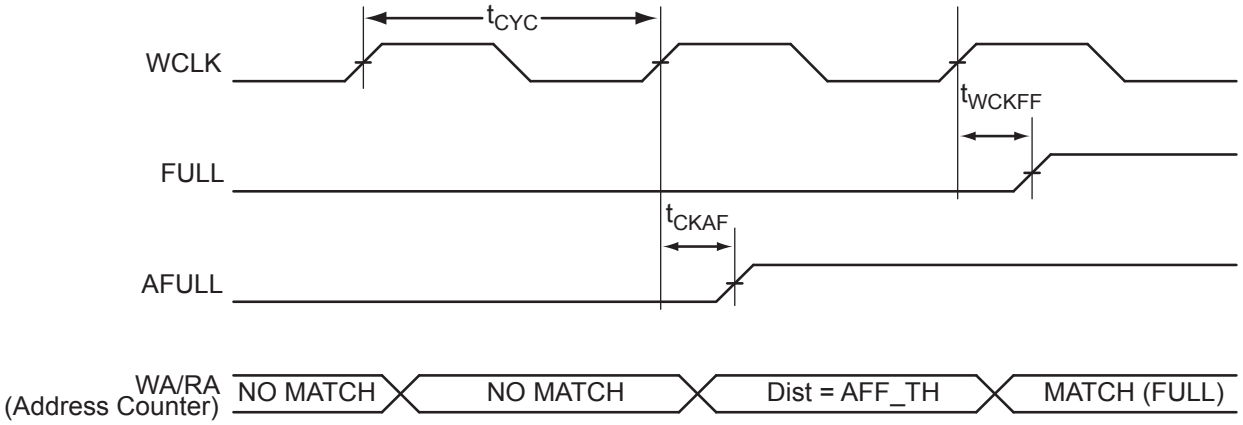


Figure 2-51 • **FIFO FULL Flag and AFULL Flag Assertion**

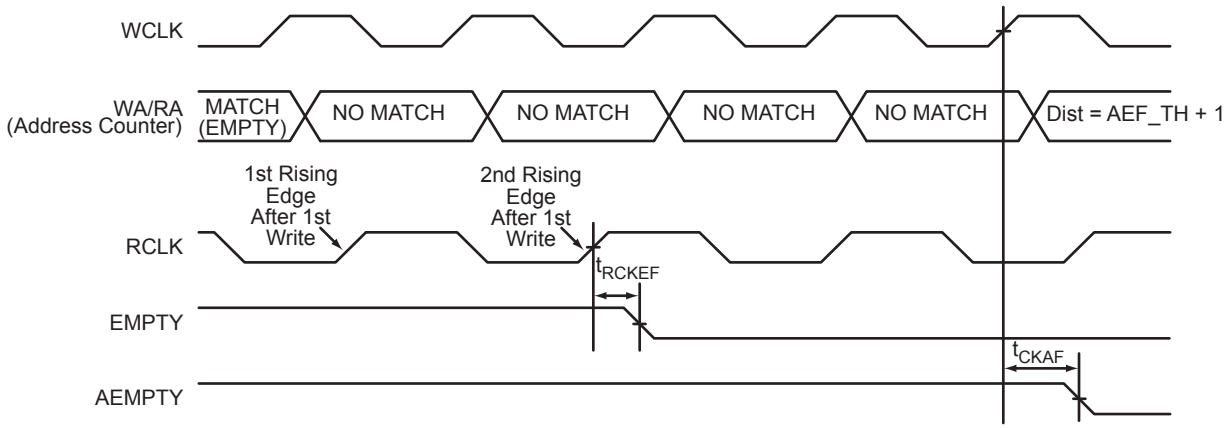


Figure 2-52 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

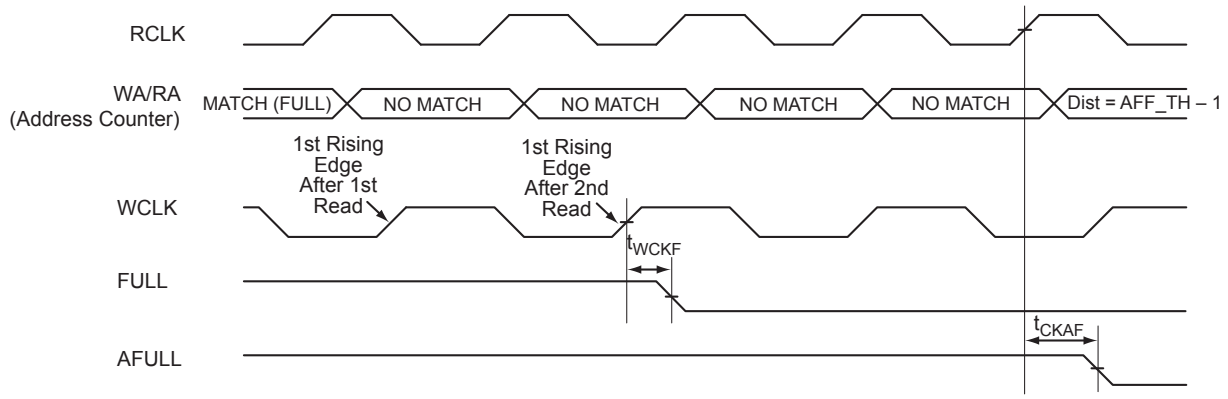


Figure 2-53 • **FIFO FULL Flag and AFULL Flag Deassertion**

Refer to the I/O Structure section of the *ProASIC3E FPGA Fabric User's Guide* for an explanation of the naming of global pins.

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 W to 1 kΩ will satisfy the requirements. Refer to Table 3-1 for more information.

***Table 3-1* • Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on the JTAG chain*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin is pulled down.*

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-1 and must satisfy the parallel resistance value requirement. The values in Table 3-1 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

FG484	
Pin Number	A3PE600 Function
N17	IO57NPB3V0
N18	IO55NPB3V0
N19	IO57PPB3V0
N20	NC
N21	IO56NDB3V0
N22	IO58PDB3V0
P1	NC
P2	IO111PDB6V1
P3	IO115NPB6V1
P4	IO113NPB6V1
P5	IO109PPB6V0
P6	IO108PDB6V0
P7	IO108NDB6V0
P8	VCCIB6
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB3
P16	GDB0/IO66NPB3V1
P17	IO60NDB3V1
P18	IO60PDB3V1
P19	IO61PDB3V1
P20	NC
P21	IO59PDB3V0
P22	IO58NDB3V0
R1	NC
R2	IO110PDB6V0
R3	VCC
R4	IO109NPB6V0
R5	IO106NDB6V0
R6	IO106PDB6V0
R7	GEC0/IO104NPB6V0
R8	VMV5

FG484	
Pin Number	A3PE600 Function
R9	VCCIB5
R10	VCCIB5
R11	IO84NDB5V0
R12	IO84PDB5V0
R13	VCCIB4
R14	VCCIB4
R15	VMV3
R16	VCCPLD
R17	GDB1/IO66PPB3V1
R18	GDC1/IO65PDB3V1
R19	IO61NDB3V1
R20	VCC
R21	IO59NDB3V0
R22	IO62PDB3V1
T1	NC
T2	IO110NDB6V0
T3	NC
T4	IO105PDB6V0
T5	IO105NDB6V0
T6	GEC1/IO104PPB6V0
T7	VCOMPLE
T8	GNDQ
T9	GEA2/IO101PPB5V2
T10	IO92NDB5V1
T11	IO90NDB5V1
T12	IO82NDB5V0
T13	IO74NDB4V1
T14	IO74PDB4V1
T15	GNDQ
T16	VCOMPLD
T17	VJTAG
T18	GDC0/IO65NDB3V1
T19	GDA1/IO67PDB3V1
T20	NC
T21	IO64PDB3V1
T22	IO62NDB3V1

FG484	
Pin Number	A3PE600 Function
U1	NC
U2	IO107PDB6V0
U3	IO107NDB6V0
U4	GEB1/IO103PDB6V0
U5	GEB0/IO103NDB6V0
U6	VMV6
U7	VCCPLE
U8	IO101NPB5V2
U9	IO95PPB5V1
U10	IO92PDB5V1
U11	IO90PDB5V1
U12	IO82PDB5V0
U13	IO76NDB4V1
U14	IO76PDB4V1
U15	VMV4
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO67NDB3V1
U20	NC
U21	IO64NDB3V1
U22	IO63PDB3V1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO102PDB6V0
V5	GEA0/IO102NDB6V0
V6	GNDQ
V7	GEC2/IO99PDB5V2
V8	IO95NPB5V1
V9	IO91NDB5V1
V10	IO91PDB5V1
V11	IO83NDB5V0
V12	IO83PDB5V0
V13	IO77NDB4V1
V14	IO77PDB4V1

FG484	
Pin Number	A3PE1500 Function
A1	GND
A2	GND
A3	VCCIB0
A4	IO05NDB0V0
A5	IO05PDB0V0
A6	IO11NDB0V1
A7	IO11PDB0V1
A8	IO15PDB0V1
A9	IO17PDB0V2
A10	IO27NDB0V3
A11	IO27PDB0V3
A12	IO32PDB1V0
A13	IO43PDB1V1
A14	IO47NDB1V1
A15	IO47PDB1V1
A16	IO51NDB1V2
A17	IO51PDB1V2
A18	IO54NDB1V3
A19	NC
A20	VCCIB1
A21	GND
A22	GND
AA1	GND
AA2	VCCIB6
AA3	NC
AA4	IO161PDB5V3
AA5	IO155NDB5V2
AA6	IO155PDB5V2
AA7	IO154NDB5V2
AA8	IO154PDB5V2
AA9	IO143PDB5V1
AA10	IO143NDB5V1
AA11	IO131PPB4V2
AA12	IO129NDB4V2
AA13	IO129PDB4V2
AA14	NC

FG484	
Pin Number	A3PE1500 Function
AA15	NC
AA16	IO117NDB4V0
AA17	IO117PDB4V0
AA18	IO115NDB4V0
AA19	IO115PDB4V0
AA20	NC
AA21	VCCIB3
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB5
AB4	IO159NDB5V3
AB5	IO159PDB5V3
AB6	IO149NDB5V1
AB7	IO149PDB5V1
AB8	IO138NDB5V0
AB9	IO138PDB5V0
AB10	NC
AB11	NC
AB12	IO127NDB4V2
AB13	IO127PDB4V2
AB14	IO125NDB4V1
AB15	IO125PDB4V1
AB16	IO122NDB4V1
AB17	IO122PDB4V1
AB18	NC
AB19	NC
AB20	VCCIB4
AB21	GND
AB22	GND
B1	GND
B2	VCCIB7
B3	NC
B4	IO03NDB0V0
B5	IO03PDB0V0
B6	IO10NDB0V1

FG484	
Pin Number	A3PE1500 Function
B7	IO10PDB0V1
B8	IO15NDB0V1
B9	IO17NDB0V2
B10	IO20PDB0V2
B11	IO29PDB0V3
B12	IO32NDB1V0
B13	IO43NDB1V1
B14	NC
B15	NC
B16	IO53NDB1V2
B17	IO53PDB1V2
B18	IO54PDB1V3
B19	NC
B20	NC
B21	VCCIB2
B22	GND
C1	VCCIB7
C2	NC
C3	NC
C4	NC
C5	GND
C6	IO07NDB0V0
C7	IO07PDB0V0
C8	VCC
C9	VCC
C10	IO20NDB0V2
C11	IO29NDB0V3
C12	NC
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC

FG484	
Pin Number	A3PE3000 Function
N17	IO132NPB3V2
N18	IO117NPB3V0
N19	IO132PPB3V2
N20	GNDQ
N21	IO126NDB3V1
N22	IO128PDB3V1
P1	IO247PDB6V1
P2	IO253PDB6V2
P3	IO270NPB6V4
P4	IO261NPB6V3
P5	IO249PPB6V1
P6	IO259PDB6V3
P7	IO259NDB6V3
P8	VCCIB6
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB3
P16	GDB0/IO152NPB3V4
P17	IO136NDB3V2
P18	IO136PDB3V2
P19	IO138PDB3V3
P20	VMV3
P21	IO130PDB3V2
P22	IO128NDB3V1
R1	IO247NDB6V1
R2	IO245PDB6V1
R3	VCC
R4	IO249NPB6V1
R5	IO251NDB6V2
R6	IO251PDB6V2
R7	GEC0/IO236NPB6V0
R8	VMV5

FG484	
Pin Number	A3PE3000 Function
R9	VCCIB5
R10	VCCIB5
R11	IO196NDB5V0
R12	IO196PDB5V0
R13	VCCIB4
R14	VCCIB4
R15	VMV3
R16	VCCPLD
R17	GDB1/IO152PPB3V4
R18	GDC1/IO151PDB3V4
R19	IO138NDB3V3
R20	VCC
R21	IO130NDB3V2
R22	IO134PDB3V2
T1	IO243PPB6V1
T2	IO245NDB6V1
T3	IO243NPB6V1
T4	IO241PDB6V0
T5	IO241NDB6V0
T6	GEC1/IO236PPB6V0
T7	VCOMPLE
T8	GNDQ
T9	GEA2/IO233PPB5V4
T10	IO206NDB5V1
T11	IO202NDB5V1
T12	IO194NDB5V0
T13	IO186NDB4V4
T14	IO186PDB4V4
T15	GNDQ
T16	VCOMPLD
T17	VJTAG
T18	GDC0/IO151NDB3V4
T19	GDA1/IO153PDB3V4
T20	IO144PDB3V3
T21	IO140PDB3V3
T22	IO134NDB3V2

FG484	
Pin Number	A3PE3000 Function
U1	IO240PPB6V0
U2	IO238PDB6V0
U3	IO238NDB6V0
U4	GEB1/IO235PDB6V0
U5	GEB0/IO235NDB6V0
U6	VMV6
U7	VCCPLE
U8	IO233NPB5V4
U9	IO222PPB5V3
U10	IO206PDB5V1
U11	IO202PDB5V1
U12	IO194PDB5V0
U13	IO176NDB4V2
U14	IO176PDB4V2
U15	VMV4
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO153NDB3V4
U20	IO144NDB3V3
U21	IO140NDB3V3
U22	IO142PDB3V3
V1	IO239PDB6V0
V2	IO240NPB6V0
V3	GND
V4	GEA1/IO234PDB6V0
V5	GEA0/IO234NDB6V0
V6	GNDQ
V7	GEC2/IO231PDB5V4
V8	IO222NPB5V3
V9	IO204NDB5V1
V10	IO204PDB5V1
V11	IO195NDB5V0
V12	IO195PDB5V0
V13	IO178NDB4V3
V14	IO178PDB4V3

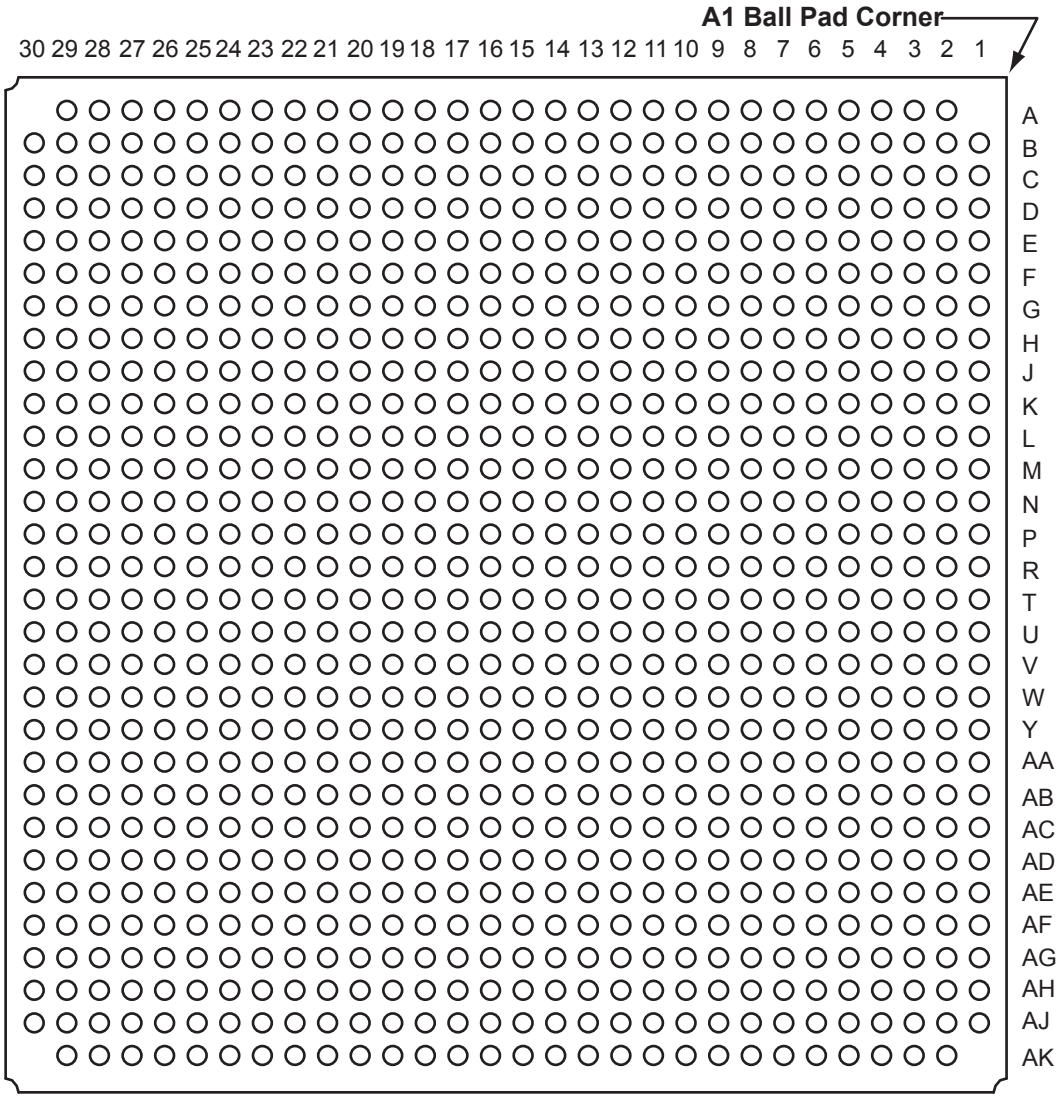
FG676	
Pin Number	A3PE1500 Function
C9	IO10PDB0V1
C10	IO16PDB0V2
C11	IO20PDB0V2
C12	IO24PDB0V3
C13	IO23PDB0V2
C14	IO28PDB0V3
C15	IO31PDB0V3
C16	IO32NDB1V0
C17	IO36NDB1V0
C18	IO37NDB1V0
C19	IO45NDB1V1
C20	IO42PPB1V1
C21	IO46NPB1V1
C22	IO48NPB1V2
C23	GBB0/IO56NPB1V3
C24	VMV1
C25	GBC2/IO60PDB2V0
C26	IO60NDB2V0
D1	IO218NDB7V3
D2	IO218PDB7V3
D3	GND
D4	VMV7
D5	IO221NDB7V3
D6	GAC0/IO02NDB0V0
D7	GAC1/IO02PDB0V0
D8	IO05NDB0V0
D9	IO08PDB0V1
D10	IO12NDB0V1
D11	IO18NDB0V2
D12	IO17NDB0V2
D13	IO25NDB0V3
D14	IO29NDB0V3
D15	IO33NDB1V0
D16	IO40PDB1V1
D17	IO43NDB1V1
D18	IO47PDB1V1

FG676	
Pin Number	A3PE1500 Function
D19	IO45PDB1V1
D20	IO46PPB1V1
D21	IO48PPB1V2
D22	GBA0/IO57NPB1V3
D23	GNDQ
D24	GBB1/IO56PPB1V3
D25	GBB2/IO59PDB2V0
D26	IO59NDB2V0
E1	IO212PDB7V2
E2	IO211NDB7V2
E3	IO211PDB7V2
E4	IO220NPB7V3
E5	GNDQ
E6	GAB2/IO220PPB7V3
E7	GAB1/IO01PDB0V0
E8	IO05PDB0V0
E9	IO08NDB0V1
E10	IO12PDB0V1
E11	IO18PDB0V2
E12	IO17PDB0V2
E13	IO25PDB0V3
E14	IO29PDB0V3
E15	IO33PDB1V0
E16	IO40NDB1V1
E17	IO43PDB1V1
E18	IO47NDB1V1
E19	IO54NDB1V3
E20	IO52NDB1V2
E21	IO52PDB1V2
E22	VCCPLB
E23	GBA1/IO57PPB1V3
E24	IO63PDB2V0
E25	IO63NDB2V0
E26	IO68PDB2V1
F1	IO212NDB7V2
F2	IO203PPB7V1

FG676	
Pin Number	A3PE1500 Function
F3	IO213NDB7V2
F4	IO213PDB7V2
F5	GND
F6	VCCPLA
F7	GAB0/IO01NDB0V0
F8	GNDQ
F9	IO03PDB0V0
F10	IO13PDB0V1
F11	IO15PDB0V1
F12	IO19PDB0V2
F13	IO21PDB0V2
F14	IO27NDB0V3
F15	IO35PDB1V0
F16	IO39NDB1V0
F17	IO51PDB1V2
F18	IO53PDB1V2
F19	IO54PDB1V3
F20	VMV2
F21	VCOMPLB
F22	IO61PDB2V0
F23	IO61NDB2V0
F24	IO66PDB2V1
F25	IO66NDB2V1
F26	IO68NDB2V1
G1	IO203NPB7V1
G2	IO207NDB7V2
G3	IO207PDB7V2
G4	IO216NDB7V3
G5	IO216PDB7V3
G6	VCOMPLA
G7	VMV0
G8	VCC
G9	IO03NDB0V0
G10	IO13NDB0V1
G11	IO15NDB0V1
G12	IO19NDB0V2

FG676	
Pin Number	**A3PE1500 Function**
W25	IO96PDB3V1
W26	IO94NDB3V0
Y1	IO175NDB6V1
Y2	IO175PDB6V1
Y3	IO173NDB6V0
Y4	IO173PDB6V0
Y5	GEC1/IO169PPB6V0
Y6	GNDQ
Y7	VMV6
Y8	VCCIB5
Y9	IO163NDB5V3
Y10	IO159PDB5V3
Y11	IO153PDB5V2
Y12	IO147PDB5V1
Y13	IO139PDB5V0
Y14	IO137PDB5V0
Y15	IO125NDB4V1
Y16	IO125PDB4V1
Y17	IO115NDB4V0
Y18	IO115PDB4V0
Y19	VCC
Y20	VPUMP
Y21	VCOMPLD
Y22	VCCPLD
Y23	IO100NDB3V1
Y24	IO100PDB3V1
Y25	IO96NDB3V1
Y26	IO98PDB3V1

FG896



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/products/fpga-soc/solutions*.

FG896	
Pin Number	A3PE3000 Function
A2	GND
A3	GND
A4	IO14NPB0V1
A5	GND
A6	IO07NPB0V0
A7	GND
A8	IO09NDB0V1
A9	IO17NDB0V2
A10	IO17PDB0V2
A11	IO21NDB0V2
A12	IO21PDB0V2
A13	IO33NDB0V4
A14	IO33PDB0V4
A15	IO35NDB0V4
A16	IO35PDB0V4
A17	IO41NDB1V0
A18	IO43NDB1V0
A19	IO43PDB1V0
A20	IO45NDB1V0
A21	IO45PDB1V0
A22	IO57NDB1V2
A23	IO57PDB1V2
A24	GND
A25	IO69PPB1V3
A26	GND
A27	GBC1/IO79PPB1V4
A28	GND
A29	GND
AA1	IO256PDB6V2
AA2	IO248PDB6V1
AA3	IO248NDB6V1
AA4	IO246NDB6V1
AA5	GEA1/IO234PDB6V0
AA6	GEA0/IO234NDB6V0
AA7	IO243PPB6V1
AA8	IO245NDB6V1

FG896	
Pin Number	A3PE3000 Function
AA9	GEB1/IO235PPB6V0
AA10	VCC
AA11	IO226PPB5V4
AA12	VCCIB5
AA13	VCCIB5
AA14	VCCIB5
AA15	VCCIB5
AA16	VCCIB4
AA17	VCCIB4
AA18	VCCIB4
AA19	VCCIB4
AA20	IO174PDB4V2
AA21	VCC
AA22	IO142NPB3V3
AA23	IO144NDB3V3
AA24	IO144PDB3V3
AA25	IO146NDB3V4
AA26	IO146PDB3V4
AA27	IO147PDB3V4
AA28	IO139NDB3V3
AA29	IO139PDB3V3
AA30	IO133NDB3V2
AB1	IO256NDB6V2
AB2	IO244PDB6V1
AB3	IO244NDB6V1
AB4	IO241PDB6V0
AB5	IO241NDB6V0
AB6	IO243NPB6V1
AB7	VCCIB6
AB8	VCCPLE
AB9	VCC
AB10	IO222PDB5V3
AB11	IO218PPB5V3
AB12	IO206NDB5V1
AB13	IO206PDB5V1
AB14	IO198NDB5V0

FG896	
Pin Number	A3PE3000 Function
AB15	IO198PDB5V0
AB16	IO192NDB4V4
AB17	IO192PDB4V4
AB18	IO178NDB4V3
AB19	IO178PDB4V3
AB20	IO174NDB4V2
AB21	IO162NPB4V1
AB22	VCC
AB23	VCCPLD
AB24	VCCIB3
AB25	IO150PDB3V4
AB26	IO148PDB3V4
AB27	IO147NDB3V4
AB28	IO145PDB3V3
AB29	IO143PDB3V3
AB30	IO137PDB3V2
AC1	IO254PDB6V2
AC2	IO254NDB6V2
AC3	IO240PDB6V0
AC4	GEC1/IO236PDB6V0
AC5	IO237PDB6V0
AC6	IO237NDB6V0
AC7	VCOMPLE
AC8	GND
AC9	IO226NPB5V4
AC10	IO222NDB5V3
AC11	IO216NPB5V2
AC12	IO210NPB5V2
AC13	IO204NDB5V1
AC14	IO204PDB5V1
AC15	IO194NDB5V0
AC16	IO188NDB4V4
AC17	IO188PDB4V4
AC18	IO182PPB4V3
AC19	IO170NPB4V2
AC20	IO164NDB4V1

FG896	
Pin Number	A3PE3000 Function
E17	IO49PDB1V1
E18	IO50PDB1V1
E19	IO58PDB1V2
E20	IO60NDB1V2
E21	IO77PDB1V4
E22	IO68NDB1V3
E23	IO68PDB1V3
E24	VCCIB1
E25	IO74PDB1V4
E26	VCC
E27	GBB1/IO80PPB1V4
E28	VCCIB2
E29	IO82NPB2V0
E30	GND
F1	IO296PPB7V2
F2	VCC
F3	IO306PDB7V4
F4	IO297PDB7V2
F5	VMV7
F6	GND
F7	GNDQ
F8	IO12NDB0V1
F9	IO12PDB0V1
F10	IO10PDB0V1
F11	IO16PDB0V1
F12	IO22NDB0V2
F13	IO30NDB0V3
F14	IO30PDB0V3
F15	IO36PDB0V4
F16	IO48NDB1V0
F17	IO48PDB1V0
F18	IO50NDB1V1
F19	IO58NDB1V2
F20	IO60PDB1V2
F21	IO77NDB1V4
F22	IO72NDB1V3

FG896	
Pin Number	A3PE3000 Function
F23	IO72PDB1V3
F24	GNDQ
F25	GND
F26	VMV2
F27	IO86PDB2V0
F28	IO92PDB2V1
F29	VCC
F30	IO100NPB2V2
G1	GND
G2	IO296NPB7V2
G3	IO306NDB7V4
G4	IO297NDB7V2
G5	VCCIB7
G6	GNDQ
G7	VCC
G8	VMV0
G9	VCCIB0
G10	IO10NDB0V1
G11	IO16NDB0V1
G12	IO22PDB0V2
G13	IO26PPB0V3
G14	IO38NPB0V4
G15	IO36NDB0V4
G16	IO46NDB1V0
G17	IO46PDB1V0
G18	IO56NDB1V1
G19	IO56PDB1V1
G20	IO66NDB1V3
G21	IO66PDB1V3
G22	VCCIB1
G23	VMV1
G24	VCC
G25	GNDQ
G26	VCCIB2
G27	IO86NDB2V0
G28	IO92NDB2V1

FG896	
Pin Number	A3PE3000 Function
G29	IO100PPB2V2
G30	GND
H1	IO294PDB7V2
H2	IO294NDB7V2
H3	IO300NDB7V3
H4	IO300PDB7V3
H5	IO295PDB7V2
H6	IO299PDB7V3
H7	VCOMPLA
H8	GND
H9	IO08NDB0V0
H10	IO08PDB0V0
H11	IO18PDB0V2
H12	IO26NPB0V3
H13	IO28NDB0V3
H14	IO28PDB0V3
H15	IO38PPB0V4
H16	IO42NDB1V0
H17	IO52NDB1V1
H18	IO52PDB1V1
H19	IO62NDB1V2
H20	IO62PDB1V2
H21	IO70NDB1V3
H22	IO70PDB1V3
H23	GND
H24	VCOMPLB
H25	GBC2/IO84PDB2V0
H26	IO84NDB2V0
H27	IO96PDB2V1
H28	IO96NDB2V1
H29	IO89PDB2V0
H30	IO89NDB2V0
J1	IO290NDB7V2
J2	IO290PDB7V2
J3	IO302NDB7V3
J4	IO302PDB7V3

Revision	Changes	Page
v2.1 (continued)	The words "ambient temperature" were added to the temperature range in the "Temperature Grade Offerings", "Speed Grade and Temperature Grade Matrix", and "Speed Grade and Temperature Grade Matrix" sections.	1-I
	The "Clock Conditioning Circuit (CCC) and PLL" section was updated.	1-I
	The caption "Main (chip)" in Figure 2-9 • Overview of Automotive ProASIC3 VersaNet Global Network was changed to "Chip (main)."	2-9
	The T_J parameter in Table 3-2 • Recommended Operating Conditions was changed to T_A, ambient temperature, and table notes 4–6 were added.	3-2
	The "PLL Macro" section was updated to add information on the VCO and PLL outputs during power-up.	2-15
v2.0 (April 2007)	In the "Temperature Grade Offerings" section, Ambient was deleted.	iii
	Ambient was deleted from "Temperature Grade Offerings".	iii
	Ambient was deleted from the "Speed Grade and Temperature Grade Matrix".	iv
	The "PLL Macro" section was updated to include power-up information.	2-15
	Table 2-13 • ProASIC3E CCC/PLL Specification was updated.	2-30
	Figure 2-19 • Peak-to-Peak Jitter Definition is new.	2-18
	The "SRAM and FIFO" section was updated with operation and timing requirement information.	2-21
	The "RESET" section was updated with read and write information.	2-25
	The "RESET" section was updated with read and write information.	2-25
	The "Introduction" in the "Advanced I/Os" section was updated to include information on input and output buffers being disabled.	2-28
	In the Table 2-15 • Levels of Hot-Swap Support, the ProASIC3 compliance descriptions were updated for levels 3 and 4.	2-34
	Table 2-45 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3E Devices was updated.	2-64
	Notes 3, 4, and 5 were added to Table 2-17 • Comparison Table for 5 V–Compliant Receiver Scheme. 5 x 52.72 was changed to 52.7 and the Maximum current was updated from 4 x 52.7 to 5 x 52.7.	2-40
	The "VCCPLF PLL Supply Voltage" section was updated.	2-50
	The "VPUMP Programming Supply Voltage" section was updated.	2-50
	The "GL Globals" section was updated to include information about direct input into quadrant clocks.	2-51
	VJTAG was deleted from the "TCK Test Clock" section.	2-51
	In Table 2-22 • Recommended Tie-Off Values for the TCK and TRST Pins, TSK was changed to TCK in note 2. Note 3 was also updated.	2-51
	Ambient was deleted from Table 3-2 • Recommended Operating Conditions. VPUMP programming mode was changed from "3.0 to 3.6" to "3.15 to 3.45".	3-2
	Note 3 is new in Table 3-4 • Overshoot and Undershoot Limits (as measured on quiet I/Os).	3-2
	In EQ 3-2, 150 was changed to 110 and the result changed to 5.88.	3-5