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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

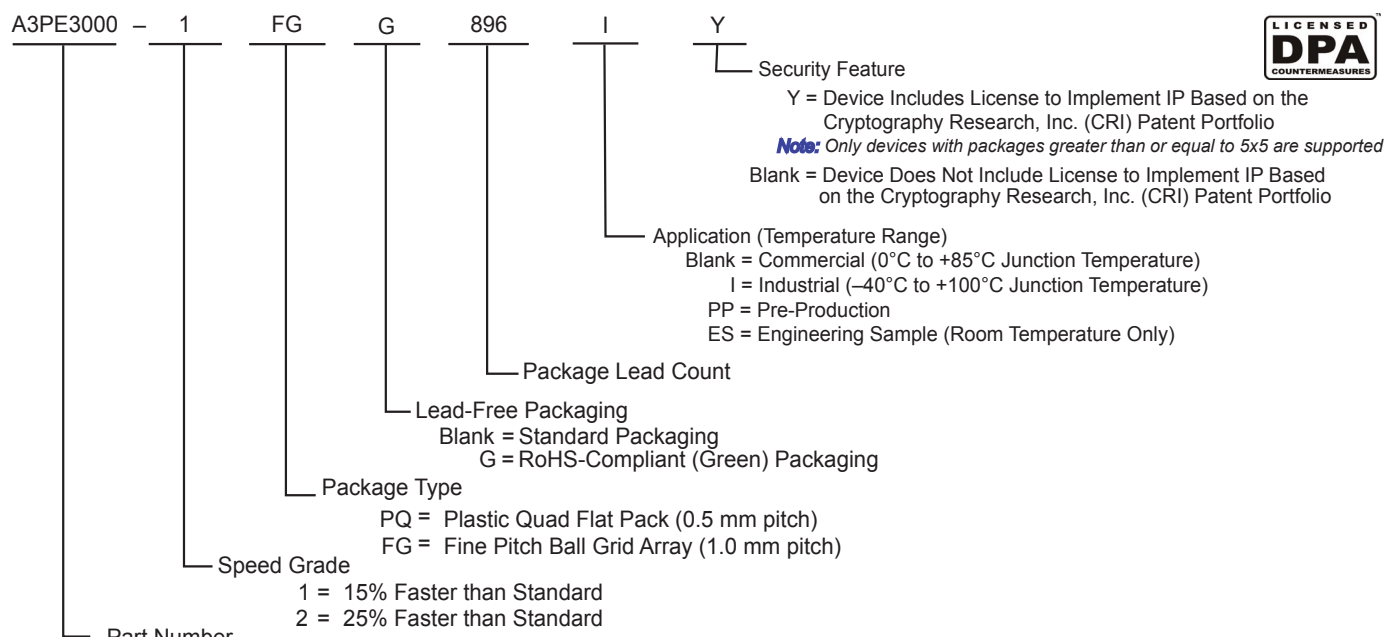
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	444
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3pe1500-2fg676

ProASIC3E Ordering Information



ProASIC3E Devices

A3PE600 = 600,000 System Gates
A3PE1500 = 1,500,000 System Gates
A3PE3000 = 3,000,000 System Gates

ProASIC3E Devices with Cortex-M1

M1A3PE1500 = 1,500,000 System Gates
M1A3PE3000 = 3,000,000 System Gates

Combinatorial Cells Contribution— P_{C-CELL}

$$P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-11 on page 2-11](#).

F_{CLK} is the global clock signal frequency.

Routing Net Contribution— P_{NET}

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-11 on page 2-11](#).

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution— P_{INPUTS}

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-11 on page 2-11](#).

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution— $P_{OUTPUTS}$

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-11 on page 2-11](#).

β_1 is the I/O buffer enable rate—guidelines are provided in [Table 2-12 on page 2-11](#).

F_{CLK} is the global clock signal frequency.

RAM Contribution— P_{MEMORY}

$$P_{MEMORY} = PAC11 * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in [Table 2-12 on page 2-11](#).

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in [Table 2-12 on page 2-11](#).

PLL Contribution— P_{PLL}

$$P_{PLL} = PAC13 + PAC14 * F_{CLKOUT}$$

F_{CLKOUT} is the output clock frequency.¹

1. The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($PAC14 * F_{CLKOUT}$ product) to the total PLL contribution.

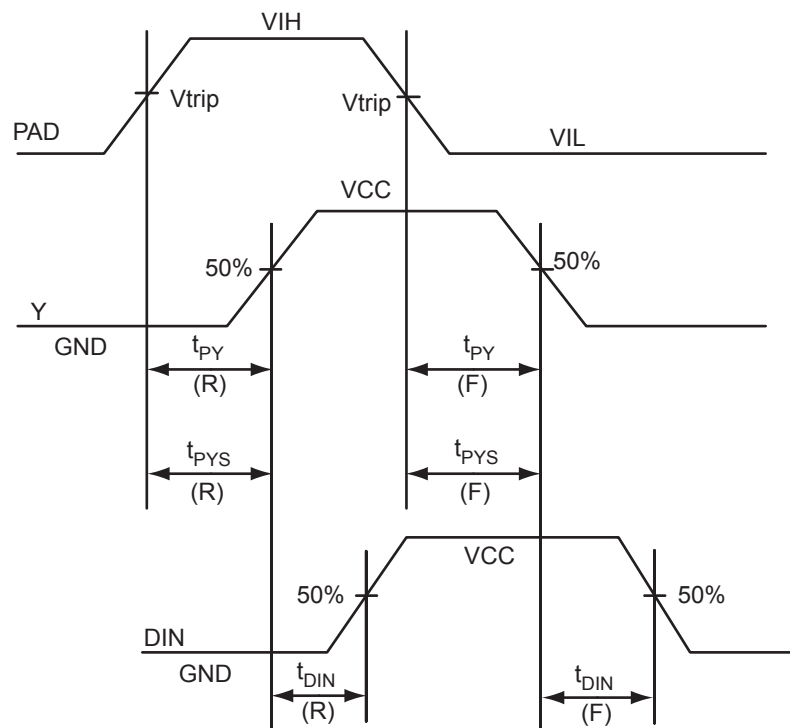
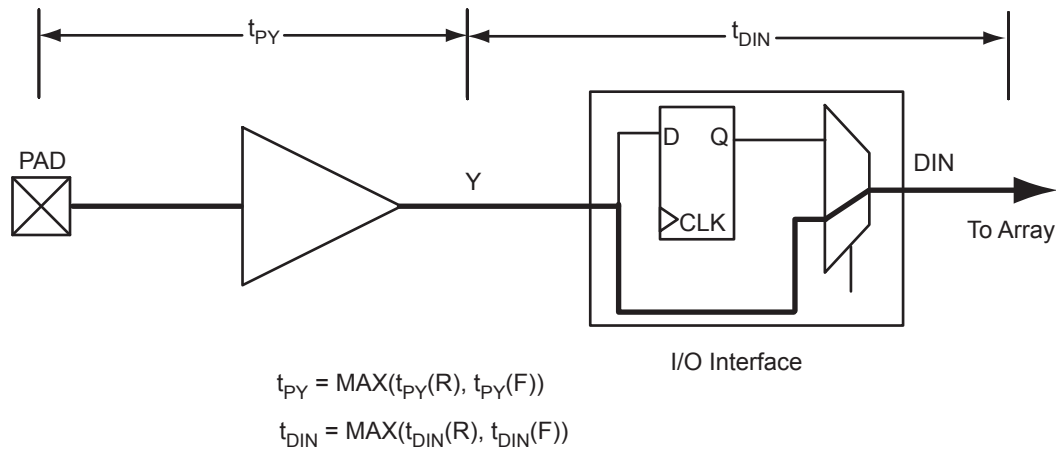


Figure 2-3 • Input Buffer Timing Model and Delays (example)

Single-Ended I/O Characteristics

3.3 V LVTTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTTL support.

Table 2-25 • Minimum and Maximum DC Input and Output Levels

3.3 V LVTTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min., V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	−0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	−0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	−0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

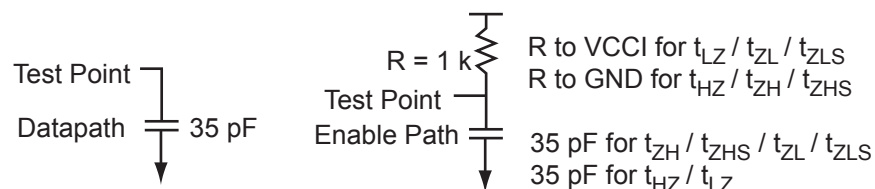


Figure 2-6 • AC Loading

Table 2-26 • 3.3 V LVTTTL / 3.3 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	3.3	1.4	–	35

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

1.8 V LVCMOS

Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-37 • Minimum and Maximum DC Input and Output Levels

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	2	2	11	9	10	10
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	4	4	22	17	10	10
6 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	6	6	44	35	10	10
8 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	8	8	51	45	10	10
12 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	12	12	74	91	10	10
16 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	16	16	74	91	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

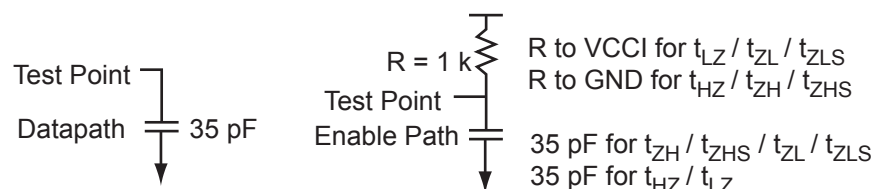


Figure 2-9 • AC Loading

Table 2-38 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	1.8	0.9	–	35

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-51 • Minimum and Maximum DC Input and Output Levels

2.5 GTL	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min., V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
20 mA ³	−0.3	VREF − 0.05	VREF + 0.05	3.6	0.4	−	20	20	124	169	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Output drive strength is below JEDEC specification.

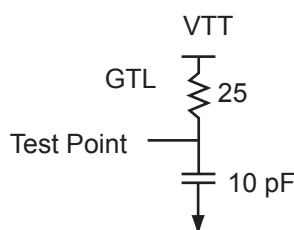


Figure 2-13 • AC Loading

Table 2-52 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF − 0.05	VREF + 0.05	0.8	0.8	1.2	10

Note: *Measuring point = Vtrip. See [Table 2-15 on page 2-18](#) for a complete table of trip points.

Timing Characteristics

Table 2-53 • 2.5 V GTL

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V VREF = 0.8 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.60	2.13	0.04	2.46	0.43	2.16	2.13			4.40	4.36	ns
−1	0.51	1.81	0.04	2.09	0.36	1.84	1.81			3.74	3.71	ns
−2	0.45	1.59	0.03	1.83	0.32	1.61	1.59			3.28	3.26	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-75 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
21 mA	−0.3	VREF − 0.2	VREF + 0.2	3.6	0.5	VCCI − 0.9	21	21	109	103	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.

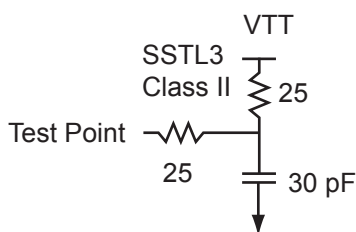


Figure 2-21 • AC Loading

Table 2-76 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF − 0.2	VREF + 0.2	1.5	1.5	1.485	30

Note: *Measuring point = V_{trip}. See [Table 2-15 on page 2-18](#) for a complete table of trip points.

Timing Characteristics

Table 2-77 • SSTL3 Class II

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 1.5 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.66	2.07	0.04	1.25	0.43	2.10	1.67			4.34	3.91	ns
−1	0.56	1.76	0.04	1.06	0.36	1.79	1.42			3.69	3.32	ns
−2	0.49	1.54	0.03	0.93	0.32	1.57	1.25			3.24	2.92	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

Timing Characteristics

Table 2-80 • LVDS

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.66	1.87	0.04	1.82	ns
-1	0.56	1.59	0.04	1.55	ns
-2	0.49	1.40	0.03	1.36	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in [Figure 2-23](#). The input and output buffer delays are available in the LVDS section in [Table 2-80](#).

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: $R_S = 60\ \Omega$ and $R_T = 70\ \Omega$, given $Z_0 = 50\ \Omega$ (2") and $Z_{stub} = 50\ \Omega$ (~1.5").

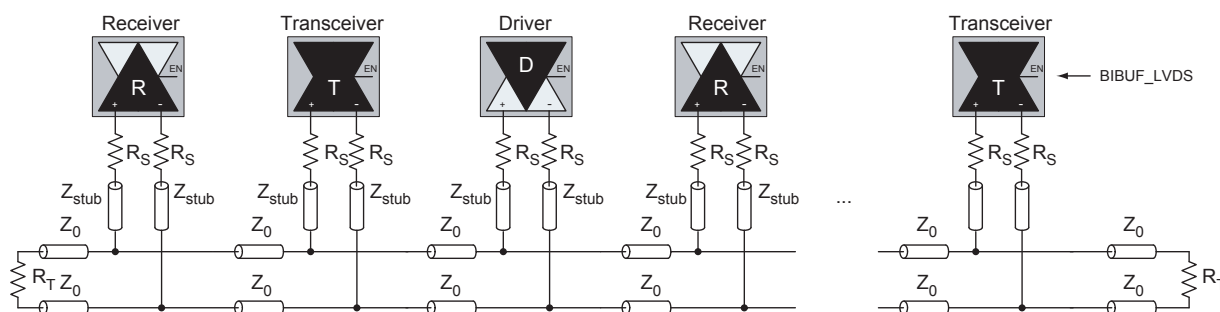


Figure 2-23 • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers

Embedded SRAM and FIFO Characteristics

SRAM

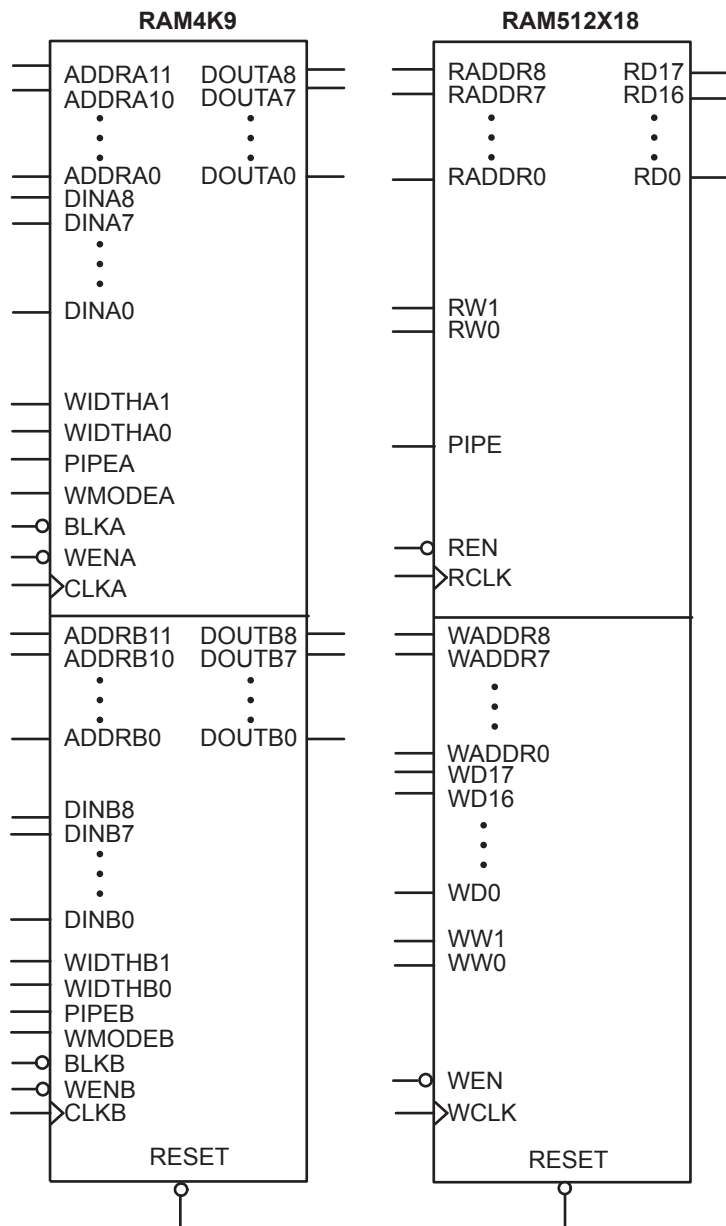


Figure 2-40 • RAM Models

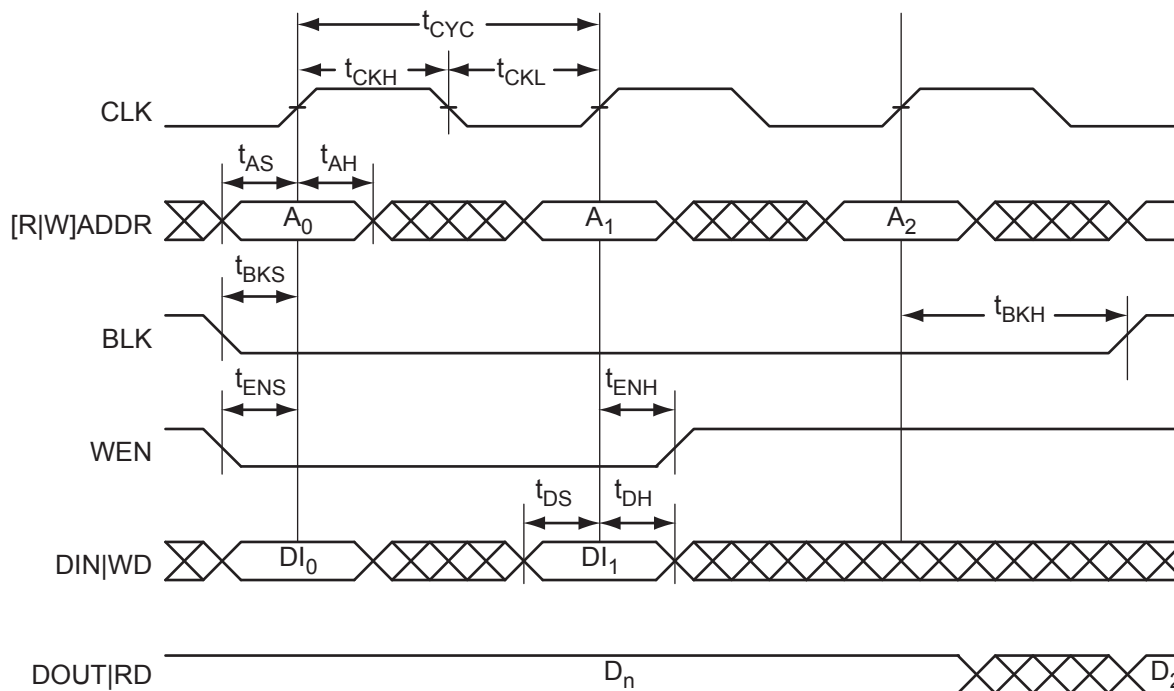


Figure 2-43 • RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.

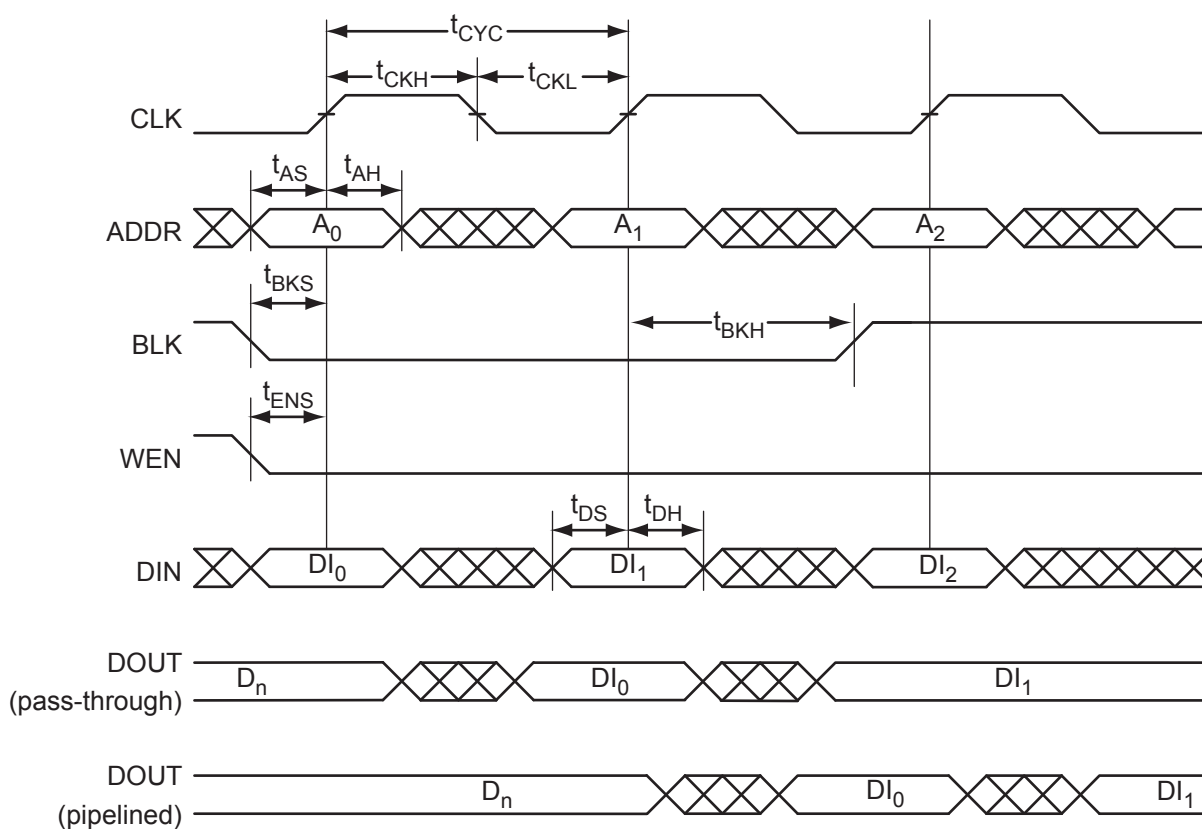
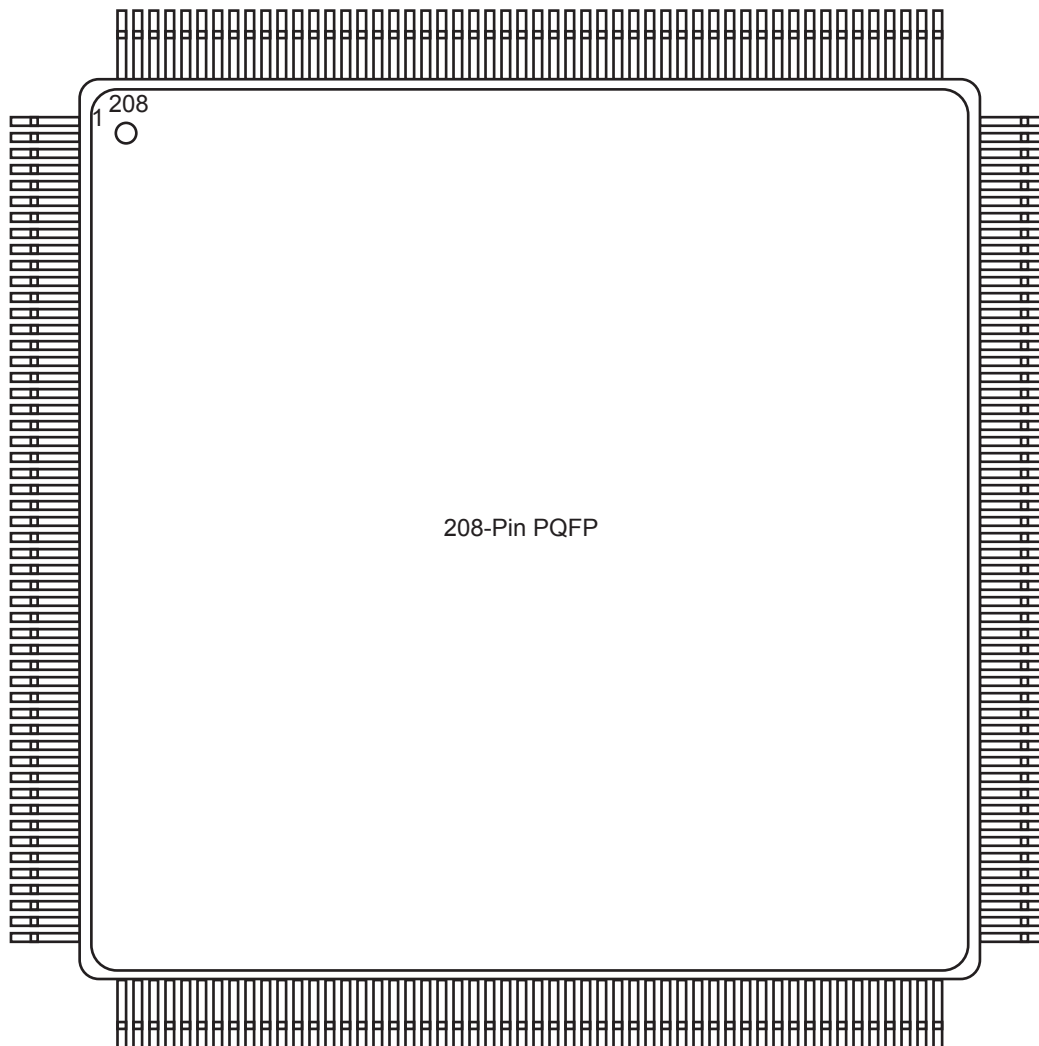


Figure 2-44 • RAM Write, Output as Write Data. Applicable to RAM4K9 Only.

4 – Package Pin Assignments

PQ208



Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/products/fpga-soc/solutions>.

PQ208	
Pin Number	A3PE3000 Function
1	GND
2	GNDQ
3	VMV7
4	GAB2/IO308PSB7V4
5	GAA2/IO309PDB7V4
6	IO309NDB7V4
7	GAC2/IO307PDB7V4
8	IO307NDB7V4
9	IO303PDB7V3
10	IO303NDB7V3
11	IO299PDB7V3
12	IO299NDB7V3
13	IO295PDB7V2
14	IO295NDB7V2
15	IO291PSB7V2
16	VCC
17	GND
18	VCCIB7
19	IO285PDB7V1
20	IO285NDB7V1
21	IO279PSB7V0
22	GFC1/IO275PSB7V0
23	GFB1/IO274PDB7V0
24	GFB0/IO274NDB7V0
25	VCOMPLF
26	GFA0/IO273NPB6V4
27	VCCPLF
28	GFA1/IO273PPB6V4
29	GND
30	GFA2/IO272PDB6V4
31	IO272NDB6V4
32	GFB2/IO271PPB6V4
33	GFC2/IO270PPB6V4
34	IO271NPB6V4
35	IO270NPB6V4
36	VCC
37	IO252PDB6V2
38	IO252NDB6V2
39	IO248PSB6V1

PQ208	
Pin Number	A3PE3000 Function
40	VCCIB6
41	GND
42	IO244PDB6V1
43	IO244NDB6V1
44	GEC1/IO236PDB6V0
45	GEC0/IO236NDB6V0
46	GEB1/IO235PPB6V0
47	GEA1/IO234PPB6V0
48	GEB0/IO235NPB6V0
49	GEA0/IO234NPB6V0
50	VMV6
51	GNDQ
52	GND
53	VMV5
54	GNDQ
55	IO233NDB5V4
56	GEA2/IO233PDB5V4
57	IO232NDB5V4
58	GEB2/IO232PDB5V4
59	IO231NDB5V4
60	GEC2/IO231PDB5V4
61	IO230PSB5V4
62	VCCIB5
63	IO218NDB5V3
64	IO218PDB5V3
65	GND
66	IO214PSB5V2
67	IO212NDB5V2
68	IO212PDB5V2
69	IO208NDB5V1
70	IO208PDB5V1
71	VCC
72	VCCIB5
73	IO202NDB5V1
74	IO202PDB5V1
75	IO198NDB5V0
76	IO198PDB5V0
77	IO197NDB5V0
78	IO197PDB5V0

PQ208	
Pin Number	A3PE3000 Function
79	IO194NDB5V0
80	IO194PDB5V0
81	GND
82	IO184NDB4V3
83	IO184PDB4V3
84	IO180NDB4V3
85	IO180PDB4V3
86	IO176NDB4V2
87	IO176PDB4V2
88	VCC
89	VCCIB4
90	IO170NDB4V2
91	IO170PDB4V2
92	IO166NDB4V1
93	IO166PDB4V1
94	IO156NDB4V0
95	GDC2/IO156PDB4V0
96	IO154NPB4V0
97	GND
98	GDB2/IO155PSB4V0
99	GDA2/IO154PPB4V0
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV4
105	GND
106	VPUMP
107	GNDQ
108	TDO
109	TRST
110	VJTAG
111	VMV3
112	GDA0/IO153NPB3V4
113	GDB0/IO152NPB3V4
114	GDA1/IO153PPB3V4
115	GDB1/IO152PPB3V4
116	GDC0/IO151NDB3V4
117	GDC1/IO151PDB3V4

FG484		FG484		FG484	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
A1	GND	AA15	IO170PDB4V2	B7	IO14PDB0V1
A2	GND	AA16	IO166NDB4V1	B8	IO18NDB0V2
A3	VCCIB0	AA17	IO166PDB4V1	B9	IO24NDB0V2
A4	IO10NDB0V1	AA18	IO160NDB4V0	B10	IO34PDB0V4
A5	IO10PDB0V1	AA19	IO160PDB4V0	B11	IO40PDB0V4
A6	IO16NDB0V1	AA20	IO158NPB4V0	B12	IO46NDB1V0
A7	IO16PDB0V1	AA21	VCCIB3	B13	IO54NDB1V1
A8	IO18PDB0V2	AA22	GND	B14	IO62NDB1V2
A9	IO24PDB0V2	AB1	GND	B15	IO62PDB1V2
A10	IO28NDB0V3	AB2	GND	B16	IO68NDB1V3
A11	IO28PDB0V3	AB3	VCCIB5	B17	IO68PDB1V3
A12	IO46PDB1V0	AB4	IO216NDB5V2	B18	IO72PDB1V3
A13	IO54PDB1V1	AB5	IO216PDB5V2	B19	IO74PDB1V4
A14	IO56NDB1V1	AB6	IO210NDB5V2	B20	IO76NPB1V4
A15	IO56PDB1V1	AB7	IO210PDB5V2	B21	VCCIB2
A16	IO64NDB1V2	AB8	IO208NDB5V1	B22	GND
A17	IO64PDB1V2	AB9	IO208PDB5V1	C1	VCCIB7
A18	IO72NDB1V3	AB10	IO197NDB5V0	C2	IO303PDB7V3
A19	IO74NDB1V4	AB11	IO197PDB5V0	C3	IO305PDB7V3
A20	VCCIB1	AB12	IO174NDB4V2	C4	IO06NPB0V0
A21	GND	AB13	IO174PDB4V2	C5	GND
A22	GND	AB14	IO172NDB4V2	C6	IO12NDB0V1
AA1	GND	AB15	IO172PDB4V2	C7	IO12PDB0V1
AA2	VCCIB6	AB16	IO168NDB4V1	C8	VCC
AA3	IO228PDB5V4	AB17	IO168PDB4V1	C9	VCC
AA4	IO224PDB5V3	AB18	IO162NDB4V1	C10	IO34NDB0V4
AA5	IO218NDB5V3	AB19	IO162PDB4V1	C11	IO40NDB0V4
AA6	IO218PDB5V3	AB20	VCCIB4	C12	IO48NDB1V0
AA7	IO212NDB5V2	AB21	GND	C13	IO48PDB1V0
AA8	IO212PDB5V2	AB22	GND	C14	VCC
AA9	IO198PDB5V0	B1	GND	C15	VCC
AA10	IO198NDB5V0	B2	VCCIB7	C16	IO70NDB1V3
AA11	IO188PPB4V4	B3	IO06PPB0V0	C17	IO70PDB1V3
AA12	IO180NDB4V3	B4	IO08NDB0V0	C18	GND
AA13	IO180PDB4V3	B5	IO08PDB0V0	C19	IO76PPB1V4
AA14	IO170NDB4V2	B6	IO14NDB0V1	C20	IO88NDB2V0

FG676	
Pin Number	A3PE1500 Function
A1	GND
A2	GND
A3	GAA0/IO00NDB0V0
A4	GAA1/IO00PDB0V0
A5	IO06NDB0V0
A6	IO09NDB0V1
A7	IO09PDB0V1
A8	IO14NDB0V1
A9	IO14PDB0V1
A10	IO22NDB0V2
A11	IO22PDB0V2
A12	IO26NDB0V3
A13	IO26PDB0V3
A14	IO30NDB0V3
A15	IO30PDB0V3
A16	IO34NDB1V0
A17	IO34PDB1V0
A18	IO38NDB1V0
A19	IO38PDB1V0
A20	IO41PDB1V1
A21	IO44PDB1V1
A22	IO49PDB1V2
A23	IO50PDB1V2
A24	GBC1/IO55PDB1V3
A25	GND
A26	GND
AA1	IO174PDB6V0
AA2	IO171PDB6V0
AA3	GEA1/IO167PPB6V0
AA4	GEC0/IO169NPB6V0
AA5	VCOMPLE
AA6	GND
AA7	IO165NDB5V3
AA8	GEB2/IO165PDB5V3
AA9	IO163PDB5V3
AA10	IO159NDB5V3

FG676	
Pin Number	A3PE1500 Function
AA11	IO153NDB5V2
AA12	IO147NDB5V1
AA13	IO139NDB5V0
AA14	IO137NDB5V0
AA15	IO123NDB4V1
AA16	IO123PDB4V1
AA17	IO117NDB4V0
AA18	IO117PDB4V0
AA19	GDB2/IO112PDB4V0
AA20	GNDQ
AA21	TDO
AA22	GND
AA23	GND
AA24	IO102NDB3V1
AA25	IO102PDB3V1
AA26	IO98NDB3V1
AB1	IO174NDB6V0
AB2	IO171NDB6V0
AB3	GEB1/IO168PPB6V0
AB4	GEA0/IO167NPB6V0
AB5	VCCPLE
AB6	GND
AB7	GND
AB8	IO156NDB5V2
AB9	IO156PDB5V2
AB10	IO150PDB5V1
AB11	IO155PDB5V2
AB12	IO142PDB5V0
AB13	IO135NDB5V0
AB14	IO135PDB5V0
AB15	IO132PDB4V2
AB16	IO129PDB4V2
AB17	IO121PDB4V1
AB18	IO119NDB4V1
AB19	IO112NDB4V0
AB20	VMV4

FG676	
Pin Number	A3PE1500 Function
AB21	TCK
AB22	TRST
AB23	GDC0/IO108NDB3V2
AB24	GDC1/IO108PDB3V2
AB25	IO104NDB3V2
AB26	IO104PDB3V2
AC1	IO170PDB6V0
AC2	GEB0/IO168NPB6V0
AC3	IO166NPB5V3
AC4	GNDQ
AC5	GND
AC6	IO160PDB5V3
AC7	IO161PDB5V3
AC8	IO154PDB5V2
AC9	GND
AC10	IO150NDB5V1
AC11	IO155NDB5V2
AC12	IO142NDB5V0
AC13	IO138NDB5V0
AC14	IO138PDB5V0
AC15	IO132NDB4V2
AC16	IO129NDB4V2
AC17	IO121NDB4V1
AC18	IO119PDB4V1
AC19	IO118NDB4V0
AC20	IO118PDB4V0
AC21	IO114PPB4V0
AC22	TMS
AC23	VJTAG
AC24	VMV3
AC25	IO106NDB3V2
AC26	IO106PDB3V2
AD1	IO170NDB6V0
AD2	GEA2/IO166PPB5V3
AD3	VMV5
AD4	GEC2/IO164PDB5V3

FG676	
Pin Number	A3PE1500 Function
C9	IO10PDB0V1
C10	IO16PDB0V2
C11	IO20PDB0V2
C12	IO24PDB0V3
C13	IO23PDB0V2
C14	IO28PDB0V3
C15	IO31PDB0V3
C16	IO32NDB1V0
C17	IO36NDB1V0
C18	IO37NDB1V0
C19	IO45NDB1V1
C20	IO42PPB1V1
C21	IO46NPB1V1
C22	IO48NPB1V2
C23	GBB0/IO56NPB1V3
C24	VMV1
C25	GBC2/IO60PDB2V0
C26	IO60NDB2V0
D1	IO218NDB7V3
D2	IO218PDB7V3
D3	GND
D4	VMV7
D5	IO221NDB7V3
D6	GAC0/IO02NDB0V0
D7	GAC1/IO02PDB0V0
D8	IO05NDB0V0
D9	IO08PDB0V1
D10	IO12NDB0V1
D11	IO18NDB0V2
D12	IO17NDB0V2
D13	IO25NDB0V3
D14	IO29NDB0V3
D15	IO33NDB1V0
D16	IO40PDB1V1
D17	IO43NDB1V1
D18	IO47PDB1V1

FG676	
Pin Number	A3PE1500 Function
D19	IO45PDB1V1
D20	IO46PPB1V1
D21	IO48PPB1V2
D22	GBA0/IO57NPB1V3
D23	GNDQ
D24	GBB1/IO56PPB1V3
D25	GBB2/IO59PDB2V0
D26	IO59NDB2V0
E1	IO212PDB7V2
E2	IO211NDB7V2
E3	IO211PDB7V2
E4	IO220NPB7V3
E5	GNDQ
E6	GAB2/IO220PPB7V3
E7	GAB1/IO01PDB0V0
E8	IO05PDB0V0
E9	IO08NDB0V1
E10	IO12PDB0V1
E11	IO18PDB0V2
E12	IO17PDB0V2
E13	IO25PDB0V3
E14	IO29PDB0V3
E15	IO33PDB1V0
E16	IO40NDB1V1
E17	IO43PDB1V1
E18	IO47NDB1V1
E19	IO54NDB1V3
E20	IO52NDB1V2
E21	IO52PDB1V2
E22	VCCPLB
E23	GBA1/IO57PPB1V3
E24	IO63PDB2V0
E25	IO63NDB2V0
E26	IO68PDB2V1
F1	IO212NDB7V2
F2	IO203PPB7V1

FG676	
Pin Number	A3PE1500 Function
F3	IO213NDB7V2
F4	IO213PDB7V2
F5	GND
F6	VCCPLA
F7	GAB0/IO01NDB0V0
F8	GNDQ
F9	IO03PDB0V0
F10	IO13PDB0V1
F11	IO15PDB0V1
F12	IO19PDB0V2
F13	IO21PDB0V2
F14	IO27NDB0V3
F15	IO35PDB1V0
F16	IO39NDB1V0
F17	IO51PDB1V2
F18	IO53PDB1V2
F19	IO54PDB1V3
F20	VMV2
F21	VCOMPLB
F22	IO61PDB2V0
F23	IO61NDB2V0
F24	IO66PDB2V1
F25	IO66NDB2V1
F26	IO68NDB2V1
G1	IO203NPB7V1
G2	IO207NDB7V2
G3	IO207PDB7V2
G4	IO216NDB7V3
G5	IO216PDB7V3
G6	VCOMPLA
G7	VMV0
G8	VCC
G9	IO03NDB0V0
G10	IO13NDB0V1
G11	IO15NDB0V1
G12	IO19NDB0V2

FG676	
Pin Number	A3PE1500 Function
G13	IO21NDB0V2
G14	IO27PDB0V3
G15	IO35NDB1V0
G16	IO39PDB1V0
G17	IO51NDB1V2
G18	IO53NDB1V2
G19	VCCIB1
G20	GBA2/IO58PPB2V0
G21	GNDQ
G22	IO64NDB2V1
G23	IO64PDB2V1
G24	IO72PDB2V2
G25	IO72NDB2V2
G26	IO78PDB2V2
H1	IO208NDB7V2
H2	IO208PDB7V2
H3	IO209NDB7V2
H4	IO209PDB7V2
H5	IO219NDB7V3
H6	GAC2/IO219PDB7V3
H7	VCCIB7
H8	VCC
H9	VCCIB0
H10	VCCIB0
H11	VCCIB0
H12	VCCIB0
H13	VCCIB0
H14	VCCIB1
H15	VCCIB1
H16	VCCIB1
H17	VCCIB1
H18	VCCIB1
H19	VCC
H20	VCC
H21	IO58NPB2V0
H22	IO70PDB2V1

FG676	
Pin Number	A3PE1500 Function
H23	IO69PDB2V1
H24	IO76PDB2V2
H25	IO76NDB2V2
H26	IO78NDB2V2
J1	IO197NDB7V0
J2	IO197PDB7V0
J3	VMV7
J4	IO215NDB7V3
J5	IO215PDB7V3
J6	IO214PDB7V3
J7	IO214NDB7V3
J8	VCCIB7
J9	VCC
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	VCC
J15	VCC
J16	VCC
J17	VCC
J18	VCC
J19	VCCIB2
J20	IO62PDB2V0
J21	IO62NDB2V0
J22	IO70NDB2V1
J23	IO69NDB2V1
J24	VMV2
J25	IO80PDB2V3
J26	IO80NDB2V3
K1	IO195PDB7V0
K2	IO199NDB7V1
K3	IO199PDB7V1
K4	IO205NDB7V1
K5	IO205PDB7V1
K6	IO217PDB7V3

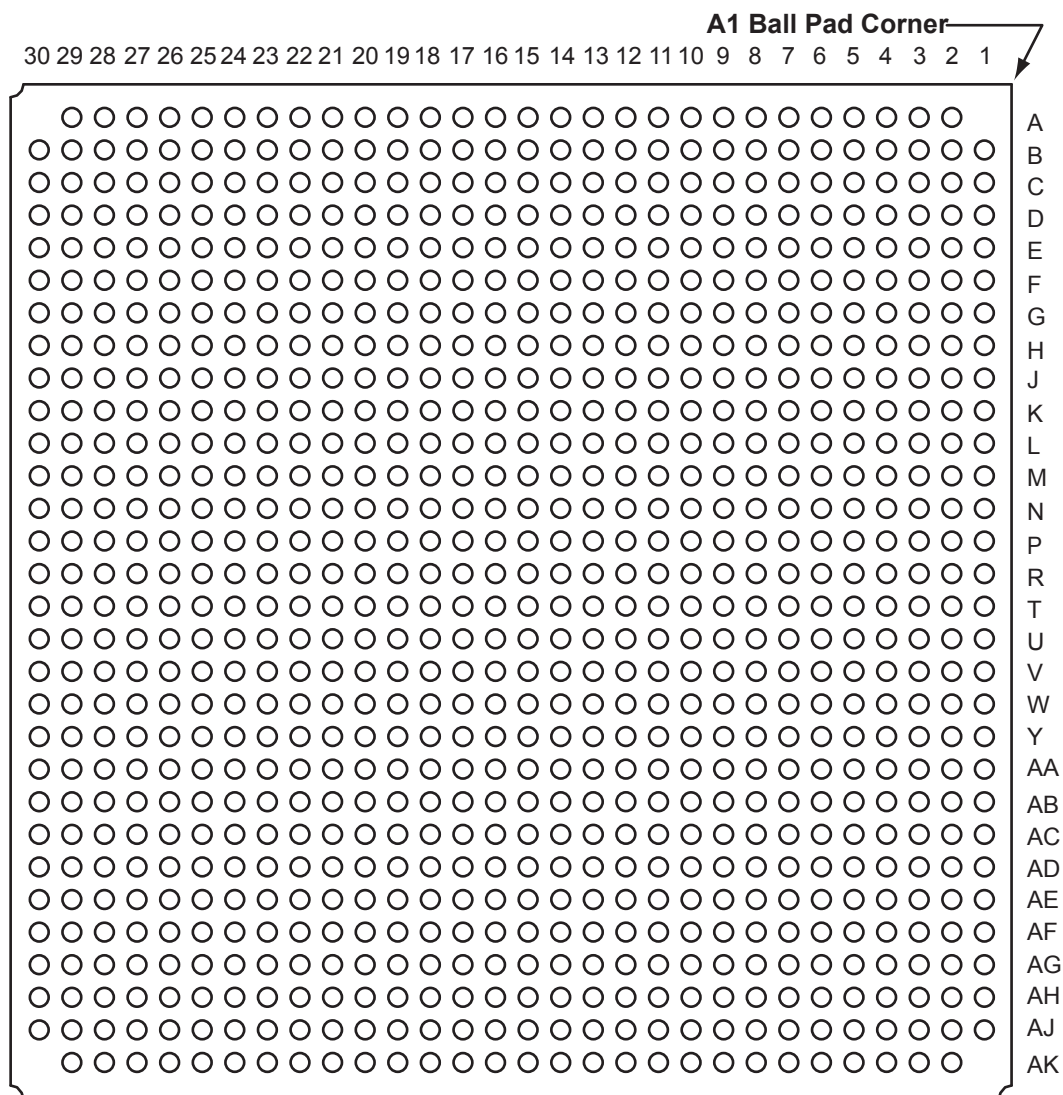
FG676	
Pin Number	A3PE1500 Function
K7	IO217NDB7V3
K8	VCCIB7
K9	VCC
K10	GND
K11	GND
K12	GND
K13	GND
K14	GND
K15	GND
K16	GND
K17	GND
K18	VCC
K19	VCCIB2
K20	IO65PDB2V1
K21	IO65NDB2V1
K22	IO74PDB2V2
K23	IO74NDB2V2
K24	IO75PDB2V2
K25	IO75NDB2V2
K26	IO84PDB2V3
L1	IO195NDB7V0
L2	IO198PPB7V0
L3	GNDQ
L4	IO201PDB7V1
L5	IO201NDB7V1
L6	IO210NDB7V2
L7	IO210PDB7V2
L8	VCCIB7
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	GND
L15	GND
L16	GND

FG676	
Pin Number	A3PE1500 Function
R21	IO89NDB3V0
R22	GCB2/IO89PDB3V0
R23	IO90NDB3V0
R24	GCC2/IO90PDB3V0
R25	IO91PDB3V0
R26	IO91NDB3V0
T1	IO186PDB6V2
T2	IO185NDB6V2
T3	GNDQ
T4	IO180PDB6V1
T5	IO180NDB6V1
T6	IO188NDB6V2
T7	GFB2/IO188PDB6V2
T8	VCCIB6
T9	VCC
T10	GND
T11	GND
T12	GND
T13	GND
T14	GND
T15	GND
T16	GND
T17	GND
T18	VCC
T19	VCCIB3
T20	IO99PDB3V1
T21	IO99NDB3V1
T22	IO97PDB3V1
T23	IO97NDB3V1
T24	GNDQ
T25	IO93PPB3V0
T26	NC
U1	IO186NDB6V2
U2	IO184NDB6V2
U3	IO184PDB6V2
U4	IO182NDB6V1

FG676	
Pin Number	A3PE1500 Function
U5	IO182PDB6V1
U6	IO178PDB6V1
U7	IO178NDB6V1
U8	VCCIB6
U9	VCC
U10	GND
U11	GND
U12	GND
U13	GND
U14	GND
U15	GND
U16	GND
U17	GND
U18	VCC
U19	VCCIB3
U20	NC
U21	IO101NDB3V1
U22	IO101PDB3V1
U23	IO92NDB3V0
U24	IO92PDB3V0
U25	IO95PDB3V1
U26	IO93NPB3V0
V1	IO183PDB6V2
V2	IO183NDB6V2
V3	VMV6
V4	IO181PDB6V1
V5	IO181NDB6V1
V6	IO176PDB6V1
V7	IO176NDB6V1
V8	VCCIB6
V9	VCC
V10	VCC
V11	VCC
V12	VCC
V13	VCC
V14	VCC

FG676	
Pin Number	A3PE1500 Function
V15	VCC
V16	VCC
V17	VCC
V18	VCC
V19	VCCIB3
V20	IO107PDB3V2
V21	IO107NDB3V2
V22	IO103NDB3V2
V23	IO103PDB3V2
V24	VMV3
V25	IO95NDB3V1
V26	IO94PDB3V0
W1	IO179NDB6V1
W2	IO179PDB6V1
W3	IO177NDB6V1
W4	IO177PDB6V1
W5	IO172PDB6V0
W6	IO172NDB6V0
W7	VCC
W8	VCC
W9	VCCIB5
W10	VCCIB5
W11	VCCIB5
W12	VCCIB5
W13	VCCIB5
W14	VCCIB4
W15	VCCIB4
W16	VCCIB4
W17	VCCIB4
W18	VCCIB4
W19	VCC
W20	VCCIB3
W21	GDB0/IO109NDB3V2
W22	GDB1/IO109PDB3V2
W23	IO105NDB3V2
W24	IO105PDB3V2

FG896



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/products/fpga-soc/solutions>.

FG896		FG896		FG896	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
J5	IO295NDB7V2	K11	IO04PPB0V0	L17	VCC
J6	IO299NDB7V3	K12	VCCIB0	L18	VCC
J7	VCCIB7	K13	VCCIB0	L19	VCC
J8	VCCPLA	K14	VCCIB0	L20	VCC
J9	VCC	K15	VCCIB0	L21	IO78NPB1V4
J10	IO04NPB0V0	K16	VCCIB1	L22	IO104NPB2V2
J11	IO18NDB0V2	K17	VCCIB1	L23	IO98NDB2V2
J12	IO20NDB0V2	K18	VCCIB1	L24	IO98PDB2V2
J13	IO20PDB0V2	K19	VCCIB1	L25	IO87PDB2V0
J14	IO32NDB0V3	K20	IO76PPB1V4	L26	IO87NDB2V0
J15	IO32PDB0V3	K21	VCC	L27	IO97PDB2V1
J16	IO42PDB1V0	K22	IO78PPB1V4	L28	IO101PDB2V2
J17	IO44NDB1V0	K23	IO88NDB2V0	L29	IO103PDB2V2
J18	IO44PDB1V0	K24	IO88PDB2V0	L30	IO119NDB3V0
J19	IO54NDB1V1	K25	IO94PDB2V1	M1	IO282NDB7V1
J20	IO54PDB1V1	K26	IO94NDB2V1	M2	IO282PDB7V1
J21	IO76NPB1V4	K27	IO85PDB2V0	M3	IO292NDB7V2
J22	VCC	K28	IO85NDB2V0	M4	IO292PDB7V2
J23	VCCPLB	K29	IO93PDB2V1	M5	IO283NDB7V1
J24	VCCIB2	K30	IO93NDB2V1	M6	IO285PDB7V1
J25	IO90PDB2V1	L1	IO286NDB7V1	M7	IO287PDB7V1
J26	IO90NDB2V1	L2	IO286PDB7V1	M8	IO289PDB7V1
J27	GBB2/IO83PDB2V0	L3	IO298NDB7V3	M9	IO289NDB7V1
J28	IO83NDB2V0	L4	IO298PDB7V3	M10	VCCIB7
J29	IO91PDB2V1	L5	IO283PDB7V1	M11	VCC
J30	IO91NDB2V1	L6	IO291NDB7V2	M12	GND
K1	IO288NDB7V1	L7	IO291PDB7V2	M13	GND
K2	IO288PDB7V1	L8	IO293PDB7V2	M14	GND
K3	IO304NDB7V3	L9	IO293NDB7V2	M15	GND
K4	IO304PDB7V3	L10	IO307NPB7V4	M16	GND
K5	GAB2/IO308PDB7V4	L11	VCC	M17	GND
K6	IO308NDB7V4	L12	VCC	M18	GND
K7	IO301PDB7V3	L13	VCC	M19	GND
K8	IO301NDB7V3	L14	VCC	M20	VCC
K9	GAC2/IO307PPB7V4	L15	VCC	M21	VCCIB2
K10	VCC	L16	VCC	M22	NC

Revision	Changes	Page
v2.1 (continued)	The words "ambient temperature" were added to the temperature range in the "Temperature Grade Offerings", "Speed Grade and Temperature Grade Matrix", and "Speed Grade and Temperature Grade Matrix" sections.	1-I
	The "Clock Conditioning Circuit (CCC) and PLL" section was updated.	1-I
	The caption "Main (chip)" in Figure 2-9 • Overview of Automotive ProASIC3 VersaNet Global Network was changed to "Chip (main)."	2-9
	The T_J parameter in Table 3-2 • Recommended Operating Conditions was changed to T_A , ambient temperature, and table notes 4–6 were added.	3-2
	The "PLL Macro" section was updated to add information on the VCO and PLL outputs during power-up.	2-15
v2.0 (April 2007)	In the "Temperature Grade Offerings" section, Ambient was deleted.	iii
	Ambient was deleted from "Temperature Grade Offerings".	iii
	Ambient was deleted from the "Speed Grade and Temperature Grade Matrix".	iv
	The "PLL Macro" section was updated to include power-up information.	2-15
	Table 2-13 • ProASIC3E CCC/PLL Specification was updated.	2-30
	Figure 2-19 • Peak-to-Peak Jitter Definition is new.	2-18
	The "SRAM and FIFO" section was updated with operation and timing requirement information.	2-21
	The "RESET" section was updated with read and write information.	2-25
	The "RESET" section was updated with read and write information.	2-25
	The "Introduction" in the "Advanced I/Os" section was updated to include information on input and output buffers being disabled.	2-28
	In the Table 2-15 • Levels of Hot-Swap Support, the ProASIC3 compliance descriptions were updated for levels 3 and 4.	2-34
	Table 2-45 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3E Devices was updated.	2-64
	Notes 3, 4, and 5 were added to Table 2-17 • Comparison Table for 5 V–Compliant Receiver Scheme. 5 x 52.72 was changed to 52.7 and the Maximum current was updated from 4 x 52.7 to 5 x 52.7.	2-40
	The "VCCPLF PLL Supply Voltage" section was updated.	2-50
	The "VPUMP Programming Supply Voltage" section was updated.	2-50
	The "GL Globals" section was updated to include information about direct input into quadrant clocks.	2-51
	VJTAG was deleted from the "TCK Test Clock" section.	2-51
	In Table 2-22 • Recommended Tie-Off Values for the TCK and TRST Pins, TSK was changed to TCK in note 2. Note 3 was also updated.	2-51
	Ambient was deleted from Table 3-2 • Recommended Operating Conditions. VPUMP programming mode was changed from "3.0 to 3.6" to "3.15 to 3.45".	3-2
	Note 3 is new in Table 3-4 • Overshoot and Undershoot Limits (as measured on quiet I/Os).	3-2
	In EQ 3-2, 150 was changed to 110 and the result changed to 5.88.	3-5