# Microchip Technology - M1A3PE1500-2PQ208I Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

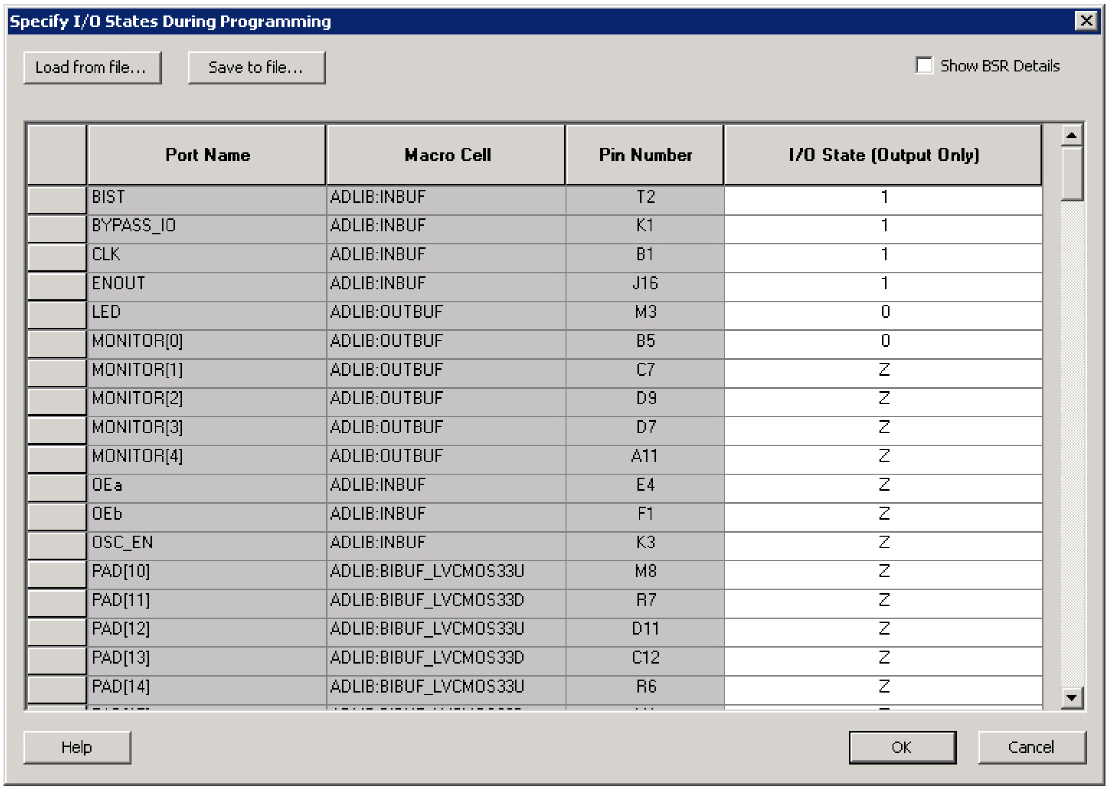
## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 276480 |
| Number of I/O | 147 |
| Number of Gates | 1500000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m1a3pe1500-2pq208i |

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



☐ Show BSR Details

| Port Name | Macro Cell | Pin Number | I/O State (Output Only) |
|---|---|---|---|
| BIST | ADLIB:INBUF | T2 | 1 |
| BYPASS_IO | ADLIB:INBUF | K1 | 1 |
| CLK | ADLIB:INBUF | B1 | 1 |
| ENOUT | ADLIB:INBUF | J16 | 1 |
| LED | ADLIB:OUTBUF | M3 | 0 |
| MONITOR[0] | ADLIB:OUTBUF | B5 | 0 |
| MONITOR[1] | ADLIB:OUTBUF | C7 | Z |
| MONITOR[2] | ADLIB:OUTBUF | D9 | Z |
| MONITOR[3] | ADLIB:OUTBUF | D7 | Z |
| MONITOR[4] | ADLIB:OUTBUF | A11 | Z |
| OEa | ADLIB:INBUF | E4 | Z |
| OEb | ADLIB:INBUF | F1 | Z |
| OSC_EN | ADLIB:INBUF | K3 | Z |
| PAD[10] | ADLIB:BIBUF_LVCMOS33U | M8 | Z |
| PAD[11] | ADLIB:BIBUF_LVCMOS33D | R7 | Z |
| PAD[12] | ADLIB:BIBUF_LVCMOS33U | D11 | Z |
| PAD[13] | ADLIB:BIBUF_LVCMOS33D | C12 | Z |
| PAD[14] | ADLIB:BIBUF_LVCMOS33U | R6 | Z |

*Figure 1-3 •* **I/O States During Programming Window**

6. Click OK to return to the FlashPoint – Programming File Generator window.

   I/O States during programming are saved to the ADB and resulting programming files after completing programming file generation.

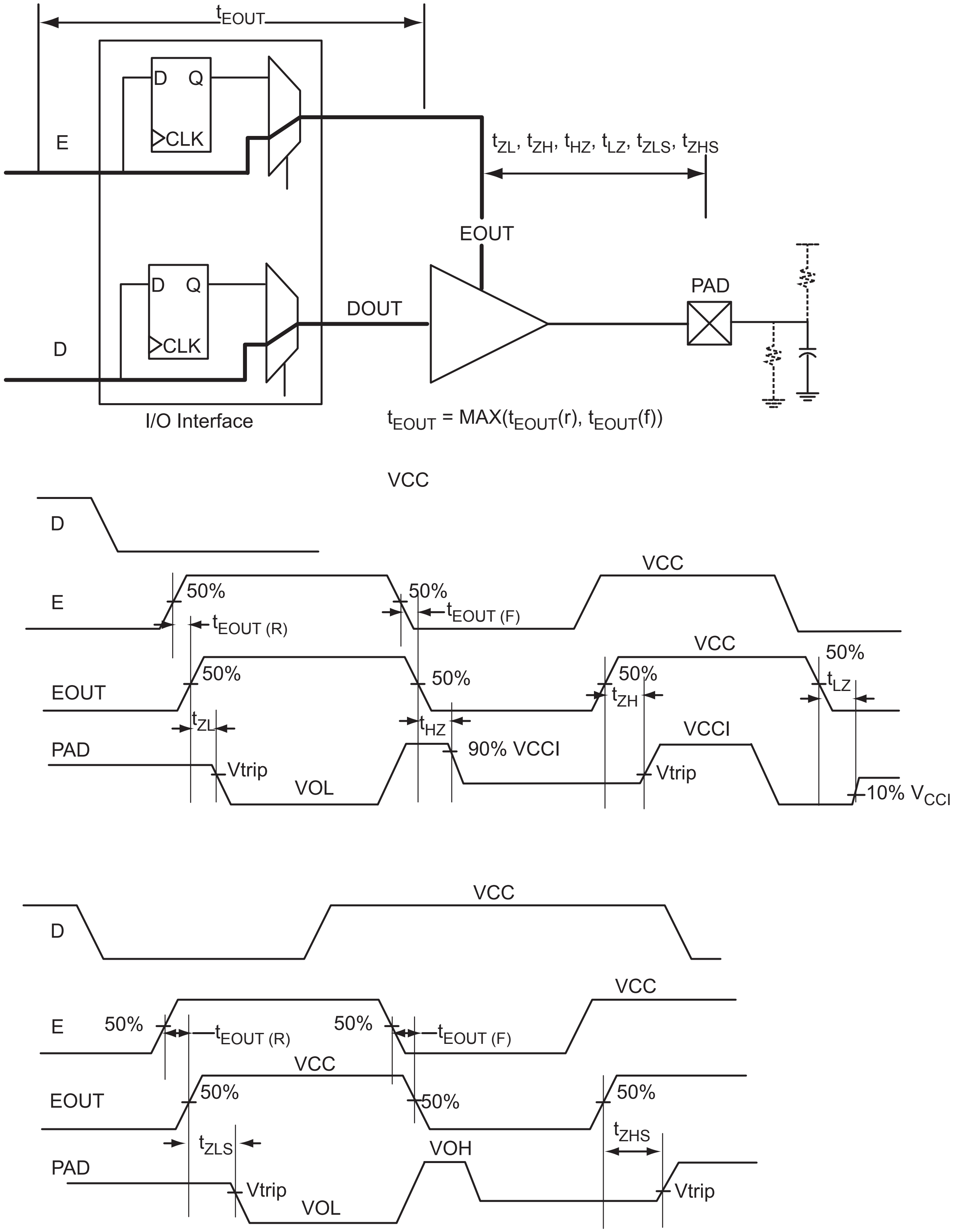


**Figure 2-5 • Tristate Output Buffer Timing Model and Delays (example)**

## Summary of I/O Timing Characteristics – Default I/O Software Settings

***Table 2-15* • Summary of AC Measuring Points**

| Standard | Input Reference Voltage (VREF_TYP) | Board Termination Voltage (VTT_REF) | Measuring Trip Point (Vtrip) |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | – | – | 1.4 V |
| 3.3 V LVCMOS Wide Range | – | – | 1.4 V |
| 2.5 V LVCMOS | – | – | 1.2 V |
| 1.8 V LVCMOS | – | – | 0.90 V |
| 1.5 V LVCMOS | – | – | 0.75 V |
| 3.3 V PCI | – | – | 0.285 * VCCI (RR)<br>0.615 * VCCI (FF)) |
| 3.3 V PCI-X | – | – | 0.285 * VCCI (RR)<br>0.615 * VCCI (FF) |
| 3.3 V GTL | 0.8 V | 1.2 V | VREF |
| 2.5 V GTL | 0.8 V | 1.2 V | VREF |
| 3.3 V GTL+ | 1.0 V | 1.5 V | VREF |
| 2.5 V GTL+ | 1.0 V | 1.5 V | VREF |
| HSTL (I) | 0.75 V | 0.75 V | VREF |
| HSTL (II) | 0.75 V | 0.75 V | VREF |
| SSTL2 (I) | 1.25 V | 1.25 V | VREF |
| SSTL2 (II) | 1.25 V | 1.25 V | VREF |
| SSTL3 (I) | 1.5 V | 1.485 V | VREF |
| SSTL3 (II) | 1.5 V | 1.485 V | VREF |
| LVDS | – | – | Cross point |
| LVPECL | – | – | Cross point |

***Table 2-16* • I/O AC Parameter Definitions**

| Parameter | Definition |
|---|---|
| $t_{DP}$ | Data to Pad delay through the Output Buffer |
| $t_{PY}$ | Pad to Data delay through the Input Buffer with Schmitt trigger disabled |
| $t_{DOUT}$ | Data to Output Buffer delay through the I/O interface |
| $t_{EOUT}$ | Enable to Output Buffer Tristate Control delay through the I/O interface |
| $t_{DIN}$ | Input Buffer to Data delay through the I/O interface |
| $t_{PYS}$ | Pad to Data delay through the Input Buffer with Schmitt trigger enabled |
| $t_{HZ}$ | Enable to Pad delay through the Output Buffer—High to Z |
| $t_{ZH}$ | Enable to Pad delay through the Output Buffer—Z to High |
| $t_{LZ}$ | Enable to Pad delay through the Output Buffer—Low to Z |
| $t_{ZL}$ | Enable to Pad delay through the Output Buffer—Z to Low |
| $t_{ZHS}$ | Enable to Pad delay through the Output Buffer with delayed enable—Z to High |
| $t_{ZLS}$ | Enable to Pad delay through the Output Buffer with delayed enable—Z to Low |

***Table 2-17*** **• Summary of I/O Timing Characteristics—Software Default Settings**
**–2 Speed Grade, Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V,**
**Worst-Case VCCI = 3.0 V**

| I/O Standard | Drive Strength (mA) | Equivalent Software Default Drive Strength Option)[1] | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | $t_{DOUT}$ (ns) | $t_{DP}$ (ns) | $t_{DIN}$ (ns) | $t_{PY}$ (ns) | $t_{PYS}$ (ns) | $t_{EOUT}$ (ns) | $t_{ZL}$ (ns) | $t_{ZH}$ (ns) | $t_{LZ}$ (ns) | $t_{HZ}$ (ns) | $t_{ZLS}$ (ns) | $t_{ZHS}$ (ns) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 12 | 12 | High | 35 | – | 0.49 | 2.74 | 0.03 | 0.90 | 1.17 | 0.32 | 2.79 | 2.14 | 2.45 | 2.70 | 4.46 | 3.81 |
| 3.3 V LVCMOS Wide Range[2] | 100 µA | 12 | High | 35 | – | 0.49 | 4.24 | 0.03 | 1.36 | 1.78 | 0.32 | 4.24 | 3.25 | 3.78 | 4.17 | 6.77 | 5.79 |
| 2.5 V LVCMOS | 12 | 12 | High | 35 | – | 0.49 | 2.80 | 0.03 | 1.13 | 1.24 | 0.32 | 2.85 | 2.61 | 2.51 | 2.61 | 4.52 | 4.28 |
| 1.8 V LVCMOS | 12 | 12 | High | 35 | – | 0.49 | 2.83 | 0.03 | 1.08 | 1.42 | 0.32 | 2.89 | 2.31 | 2.79 | 3.16 | 4.56 | 3.98 |
| 1.5 V LVCMOS | 12 | 12 | High | 35 | – | 0.49 | 3.30 | 0.03 | 1.27 | 1.60 | 0.32 | 3.36 | 2.70 | 2.96 | 3.27 | 5.03 | 4.37 |
| 3.3 V PCI | Per PCI spec | – | High | 10 | 25[3] | 0.49 | 2.09 | 0.03 | 0.78 | 1.17 | 0.32 | 2.13 | 1.49 | 2.45 | 2.70 | 3.80 | 3.16 |
| 3.3 V PCI-X | Per PCI-X spec | – | High | 10 | 25[3] | 0.49 | 2.09 | 0.03 | 0.78 | 1.17 | 0.32 | 2.13 | 1.49 | 2.45 | 2.70 | 3.80 | 3.16 |
| 3.3 V GTL | 20[4] | – | High | 10 | 25 | 0.45 | 1.55 | 0.03 | 2.19 | – | 0.32 | 1.52 | 1.55 | – | – | 3.19 | 3.22 |
| 2.5 V GTL | 20[4] | – | High | 10 | 25 | 0.45 | 1.59 | 0.03 | 1.83 | – | 0.32 | 1.61 | 1.59 | – | – | 3.28 | 3.26 |
| 3.3 V GTL+ | 35 | – | High | 10 | 25 | 0.45 | 1.53 | 0.03 | 1.19 | – | 0.32 | 1.56 | 1.53 | – | – | 3.23 | 3.20 |
| 2.5 V GTL+ | 33 | – | High | 10 | 25 | 0.45 | 1.65 | 0.03 | 1.13 | – | 0.32 | 1.68 | 1.57 | – | – | 3.35 | 3.24 |
| HSTL (I) | 8 | – | High | 20 | 50 | 0.49 | 2.37 | 0.03 | 1.59 | – | 0.32 | 2.42 | 2.35 | – | – | 4.09 | 4.02 |
| HSTL (II) | 15[4] | – | High | 20 | 25 | 0.49 | 2.26 | 0.03 | 1.59 | – | 0.32 | 2.30 | 2.03 | – | – | 3.97 | 3.70 |
| SSTL2 (I) | 15 | – | High | 30 | 50 | 0.49 | 1.59 | 0.03 | 1.00 | – | 0.32 | 1.62 | 1.38 | – | – | 3.29 | 3.05 |
| SSTL2 (II) | 18 | – | High | 30 | 25 | 0.49 | 1.62 | 0.03 | 1.00 | – | 0.32 | 1.65 | 1.32 | – | – | 3.32 | 2.99 |
| SSTL3 (I) | 14 | – | High | 30 | 50 | 0.49 | 1.72 | 0.03 | 0.93 | – | 0.32 | 1.75 | 1.37 | – | – | 3.42 | 3.04 |
| SSTL3 (II) | 21 | – | High | 30 | 25 | 0.49 | 1.54 | 0.03 | 0.93 | – | 0.32 | 1.57 | 1.25 | – | – | 3.24 | 2.92 |
| LVDS/B-LVDS/ M-LVDS | 24 | – | High | – | – | 0.49 | 1.40 | 0.03 | 1.36 | – | – | – | – | – | – | – | – |
| LVPECL | 24 | – | High | – | – | 0.49 | 1.36 | 0.03 | 1.22 | – | – | – | – | – | – | – | – |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3V wide range as specified in the JESD8b specification.*
3. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-38 for connectivity. This resistor is not required during normal operation.*
4. *Output drive strength is below JEDEC specification.*
5. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5.*

## Timing Characteristics

**Table 2-31 • 3.3 V LVCMOS Wide Range High Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V**

| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 4 mA | Std. | 0.66 | 12.19 | 0.04 | 1.83 | 2.38 | 0.43 | 12.19 | 10.17 | 4.16 | 4.00 | 15.58 | 13.57 | ns |
| | | –1 | 0.56 | 10.37 | 0.04 | 1.55 | 2.02 | 0.36 | 10.37 | 8.66 | 3.54 | 3.41 | 13.26 | 11.54 | ns |
| | | –2 | 0.49 | 9.10 | 0.03 | 1.36 | 1.78 | 0.32 | 9.10 | 7.60 | 3.11 | 2.99 | 11.64 | 10.13 | ns |
| 100 µA | 8 mA | Std. | 0.66 | 7.85 | 0.04 | 1.83 | 2.38 | 0.43 | 7.85 | 6.29 | 4.71 | 4.97 | 11.24 | 9.68 | ns |
| | | –1 | 0.56 | 6.68 | 0.04 | 1.55 | 2.02 | 0.36 | 6.68 | 5.35 | 4.01 | 4.22 | 9.57 | 8.24 | ns |
| | | –2 | 0.49 | 5.86 | 0.03 | 1.36 | 1.78 | 0.32 | 5.86 | 4.70 | 3.52 | 3.71 | 8.40 | 7.23 | ns |
| 100 µA | 12 mA | Std. | 0.66 | 5.67 | 0.04 | 1.83 | 2.38 | 0.43 | 5.67 | 4.36 | 5.06 | 5.59 | 9.07 | 7.75 | ns |
| | | –1 | 0.56 | 4.82 | 0.04 | 1.55 | 2.02 | 0.36 | 4.82 | 3.71 | 4.31 | 4.75 | 7.71 | 6.59 | ns |
| | | –2 | 0.49 | 4.24 | 0.03 | 1.36 | 1.78 | 0.32 | 4.24 | 3.25 | 3.78 | 4.17 | 6.77 | 5.79 | ns |
| 100 µA | 16 mA | Std. | 0.66 | 5.35 | 0.04 | 1.83 | 2.38 | 0.43 | 5.35 | 3.96 | 5.15 | 5.76 | 8.75 | 7.35 | ns |
| | | –1 | 0.56 | 4.55 | 0.04 | 1.55 | 2.02 | 0.36 | 4.55 | 3.36 | 4.38 | 4.90 | 7.44 | 6.25 | ns |
| | | –2 | 0.49 | 4.00 | 0.03 | 1.36 | 1.78 | 0.32 | 4.00 | 2.95 | 3.85 | 4.30 | 6.53 | 5.49 | ns |
| 100 µA | 24 mA | Std. | 0.66 | 4.96 | 0.04 | 1.83 | 2.38 | 0.43 | 4.96 | 3.27 | 5.23 | 6.38 | 8.35 | 6.67 | ns |
| | | –1 | 0.56 | 4.22 | 0.04 | 1.55 | 2.02 | 0.36 | 4.22 | 2.78 | 4.45 | 5.43 | 7.11 | 5.67 | ns |
| | | –2 | 0.49 | 3.70 | 0.03 | 1.36 | 1.78 | 0.32 | 3.70 | 2.44 | 3.91 | 4.76 | 6.24 | 4.98 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *Software default selection highlighted in gray.*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

**Table 2-84 • Parameter Definition and Measuring Nodes**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | H, DOUT |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | F, H |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | F, H |
| $t_{OSUE}$ | Enable Setup Time for the Output Data Register | G, H |
| $t_{OHE}$ | Enable Hold Time for the Output Data Register | G, H |
| $t_{OPRE2Q}$ | Asynchronous Preset-to-Q of the Output Data Register | L, DOUT |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | L, H |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | L, H |
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | H, EOUT |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | J, H |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | J, H |
| $t_{OESUE}$ | Enable Setup Time for the Output Enable Register | K, H |
| $t_{OEHE}$ | Enable Hold Time for the Output Enable Register | K, H |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | I, EOUT |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | I, H |
| $t_{OERECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | I, H |
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | A, E |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | C, A |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | C, A |
| $t_{ISUE}$ | Enable Setup Time for the Input Data Register | B, A |
| $t_{IHE}$ | Enable Hold Time for the Input Data Register | B, A |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | D, E |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | D, A |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | D, A |

*Note: *See Figure 2-25 on page 2-53 for more information.*

*Table 2-85* • **Parameter Definition and Measuring Nodes**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | HH, DOUT |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | FF, HH |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | FF, HH |
| $t_{OSUE}$ | Enable Setup Time for the Output Data Register | GG, HH |
| $t_{OHE}$ | Enable Hold Time for the Output Data Register | GG, HH |
| $t_{OCLR2Q}$ | Asynchronous Clear-to-Q of the Output Data Register | LL, DOUT |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | LL, HH |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | LL, HH |
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | HH, EOUT |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | JJ, HH |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | JJ, HH |
| $t_{OESUE}$ | Enable Setup Time for the Output Enable Register | KK, HH |
| $t_{OEHE}$ | Enable Hold Time for the Output Enable Register | KK, HH |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | II, EOUT |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | II, HH |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | II, HH |
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | AA, EE |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | CC, AA |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | CC, AA |
| $t_{ISUE}$ | Enable Setup Time for the Input Data Register | BB, AA |
| $t_{IHE}$ | Enable Hold Time for the Input Data Register | BB, AA |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | DD, EE |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | DD, AA |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | DD, AA |

Note: *See Figure 2-26 on page 2-55 for more information.

### Output DDR Module

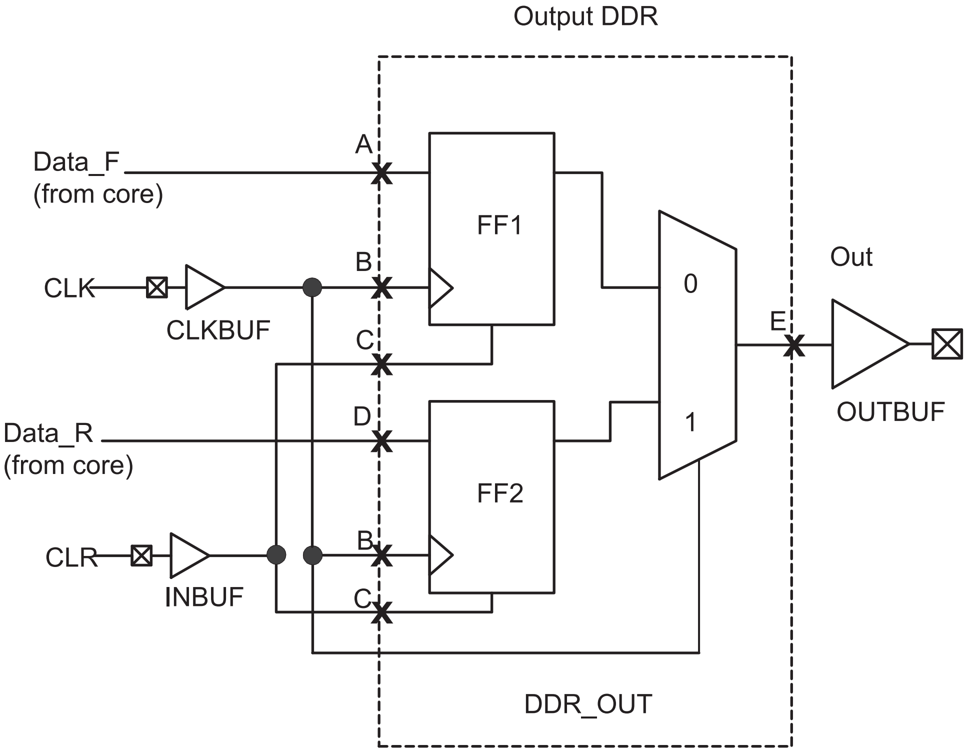


***Figure 2-32*** **• Output DDR Timing Model**

***Table 2-91*** **• Parameter Definitions**

| **Parameter Name** | **Parameter Definition** | **Measuring Nodes (from, to)** |
|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out | B, E |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out | C, E |
| $t_{DDROREMCLR}$ | Clear Removal | C, B |
| $t_{DDRORECCLR}$ | Clear Recovery | C, B |
| $t_{DDROSUD1}$ | Data Setup Data_F | A, B |
| $t_{DDROSUD2}$ | Data Setup Data_R | D, B |
| $t_{DDROHD1}$ | Data Hold Data_F | A, B |
| $t_{DDROHD2}$ | Data Hold Data_R | D, B |

### Timing Characteristics

***Table 2-93*** **• Combinatorial Cell Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Combinatorial Cell | Equation | Parameter | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|---|
| INV | Y = !A | $t_{PD}$ | 0.40 | 0.46 | 0.54 | ns |
| AND2 | Y = A · B | $t_{PD}$ | 0.47 | 0.54 | 0.63 | ns |
| NAND2 | Y = !(A · B) | $t_{PD}$ | 0.47 | 0.54 | 0.63 | ns |
| OR2 | Y = A + B | $t_{PD}$ | 0.49 | 0.55 | 0.65 | ns |
| NOR2 | Y = !(A + B) | $t_{PD}$ | 0.49 | 0.55 | 0.65 | ns |
| XOR2 | Y = A ⊕ B | $t_{PD}$ | 0.74 | 0.84 | 0.99 | ns |
| MAJ3 | Y = MAJ(A , B, C) | $t_{PD}$ | 0.70 | 0.79 | 0.93 | ns |
| XOR3 | Y = A ⊕ B ⊕ C | $t_{PD}$ | 0.87 | 1.00 | 1.17 | ns |
| MUX2 | Y = A !S + B S | $t_{PD}$ | 0.51 | 0.58 | 0.68 | ns |
| AND3 | Y = A · B · C | $t_{PD}$ | 0.56 | 0.64 | 0.75 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

## VersaTile Specifications as a Sequential Module

The ProASIC3E library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.

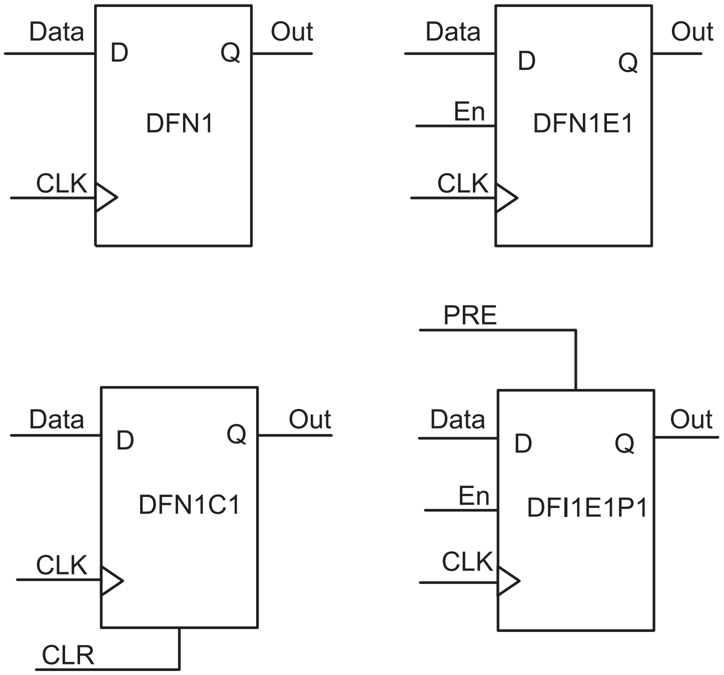


***Figure 2-36*** **• Sample of Sequential Cells**

### Timing Characteristics

**Table 2-95 • A3PE600 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | –2 | | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.83 | 1.04 | 0.94 | 1.18 | 1.11 | 1.39 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 0.81 | 1.06 | 0.93 | 1.21 | 1.09 | 1.42 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.75 | | 0.85 | | 1.00 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | | 0.96 | | 1.13 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.25 | | 0.28 | | 0.33 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

**Table 2-96 • A3PE1500 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | –2 | | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.07 | 1.29 | 1.22 | 1.47 | 1.43 | 1.72 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.06 | 1.32 | 1.21 | 1.50 | 1.42 | 1.76 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.75 | | 0.85 | | 1.00 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | | 0.96 | | 1.13 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.26 | | 0.29 | | 0.34 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

**Table 2-97 • A3PE3000 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | –2 | | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.41 | 1.62 | 1.60 | 1.85 | 1.88 | 2.17 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.40 | 1.66 | 1.59 | 1.89 | 1.87 | 2.22 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.75 | | 0.85 | | 1.00 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | | 0.96 | | 1.13 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.26 | | 0.29 | | 0.35 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

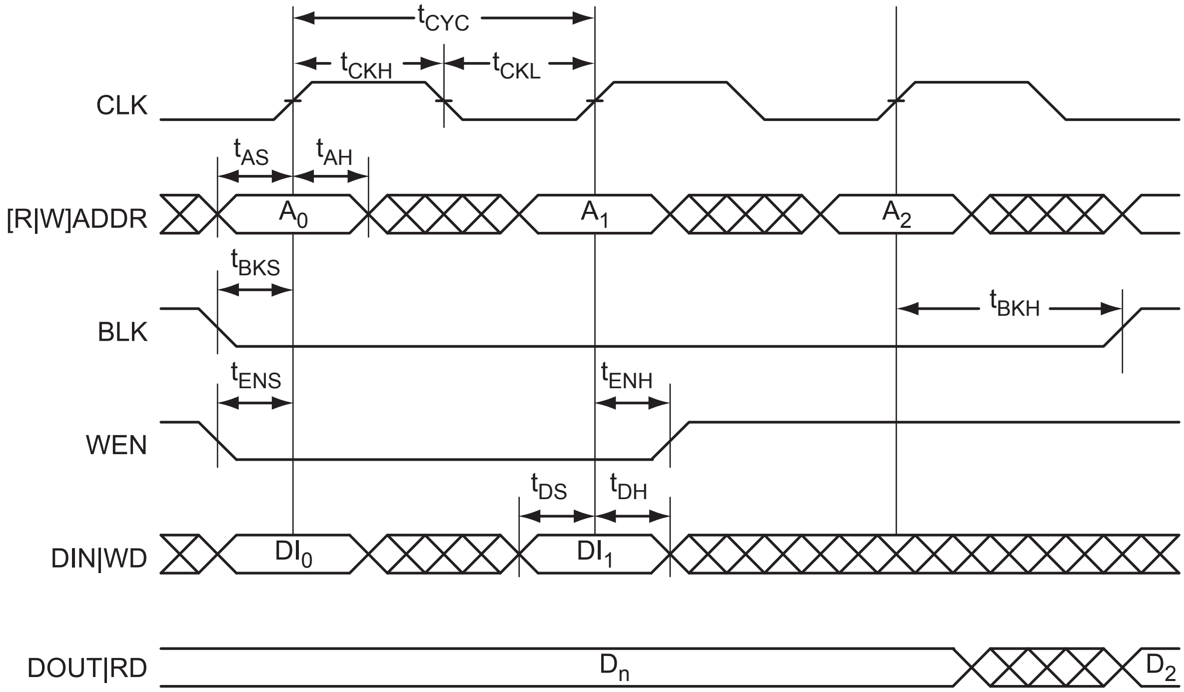


*Figure 2-43* • **RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.**

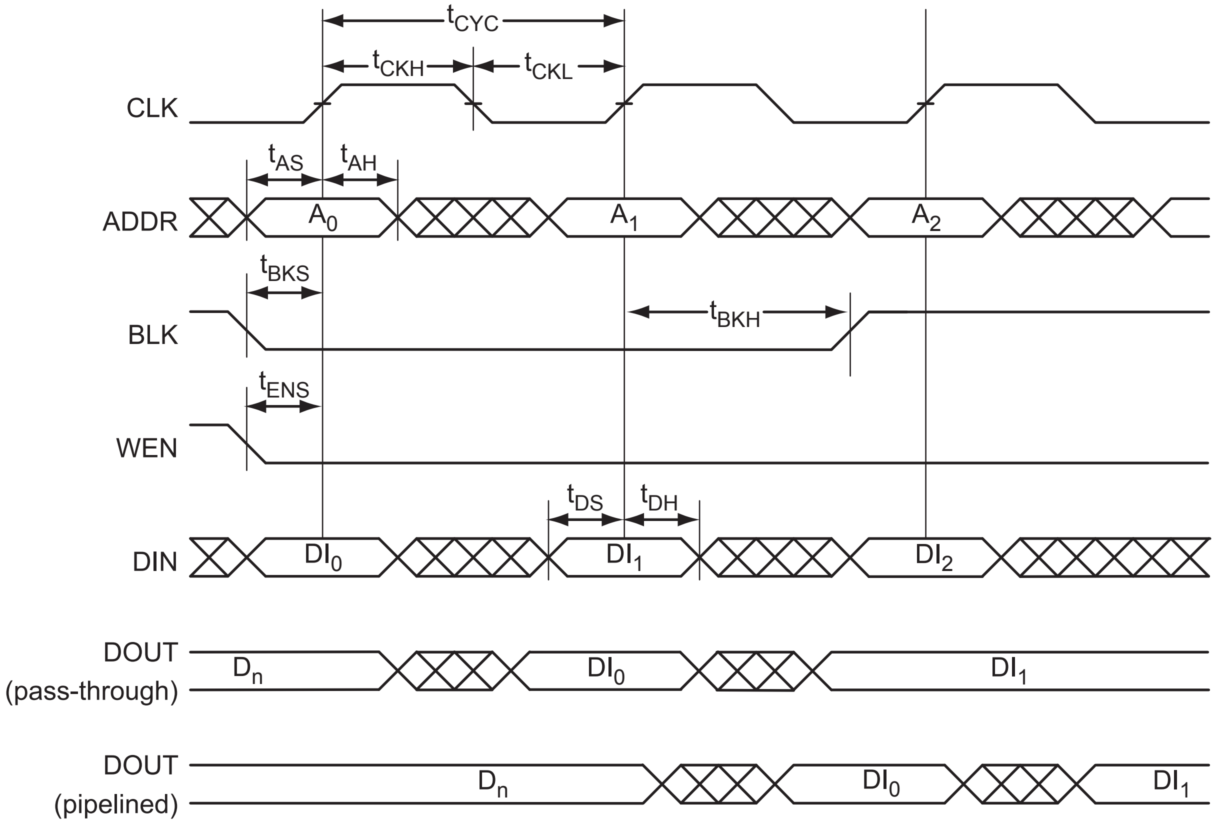


*Figure 2-44* • **RAM Write, Output as Write Data. Applicable to RAM4K9 Only.**

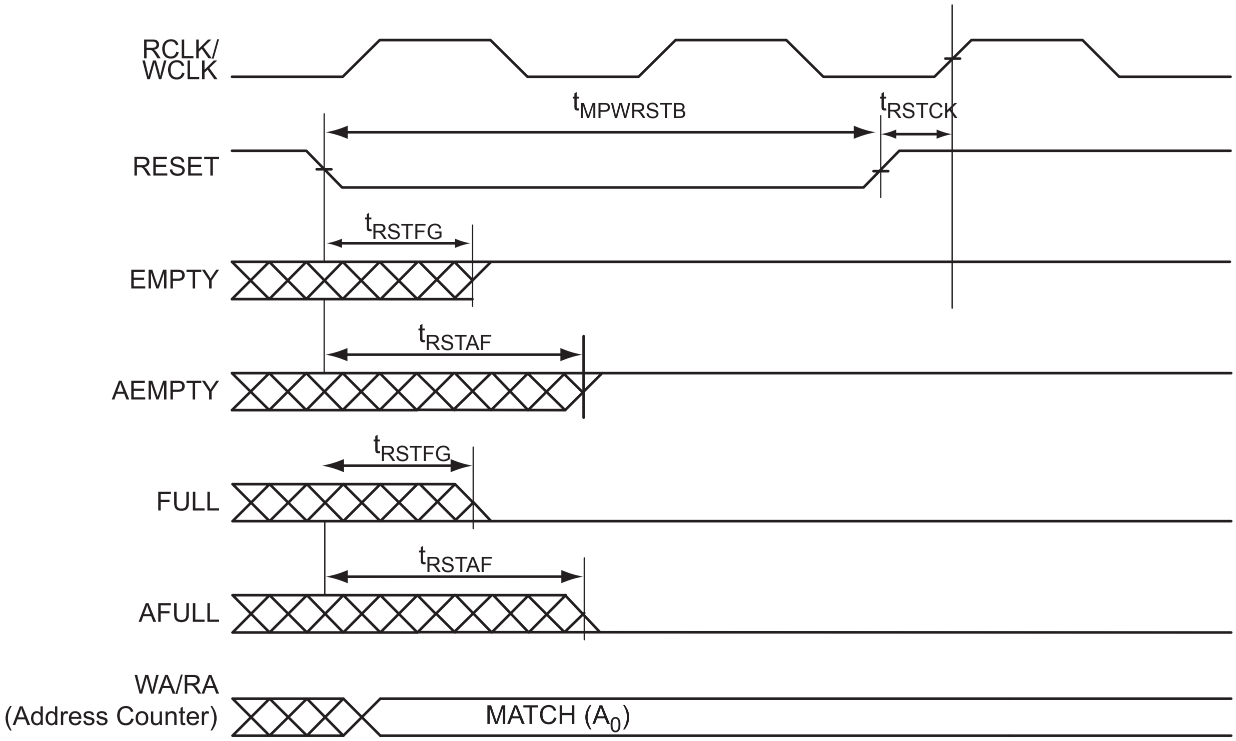


*Figure 2-49* • **FIFO Reset**

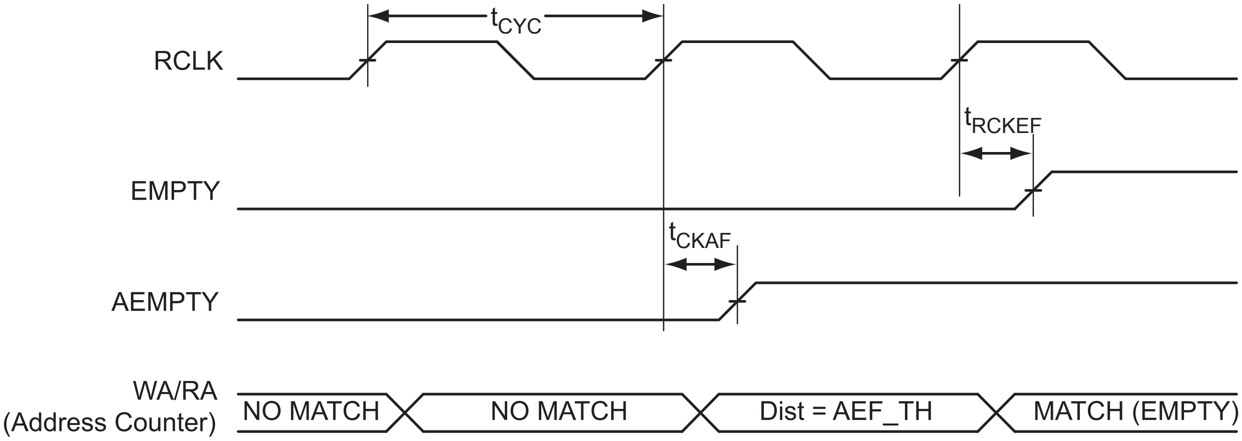


*Figure 2-50* • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

### VJTAG JTAG Supply Voltage

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

### VPUMP Programming Supply Voltage

For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

## User-Defined Supply Pins

### VREF I/O Voltage Reference

Reference voltage for I/O minibanks. VREF pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, can be designated the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One VREF pin can support the number of I/Os available in its minibank.

## User Pins

### I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

### GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *ProASIC3E FPGA Fabric User's Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

# 4 – Package Pin Assignments

## PQ208

*Note: This is the top view of the package.*

### *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/products/fpga-soc/solutions*.

| PQ208 | |
|---|---|
| Pin Number | A3PE600 Function |
| 1 | GND |
| 2 | GNDQ |
| 3 | VMV7 |
| 4 | GAB2/IO133PSB7V1 |
| 5 | GAA2/IO134PDB7V1 |
| 6 | IO134NDB7V1 |
| 7 | GAC2/IO132PDB7V1 |
| 8 | IO132NDB7V1 |
| 9 | IO130PDB7V1 |
| 10 | IO130NDB7V1 |
| 11 | IO127PDB7V1 |
| 12 | IO127NDB7V1 |
| 13 | IO126PDB7V0 |
| 14 | IO126NDB7V0 |
| 15 | IO124PSB7V0 |
| 16 | VCC |
| 17 | GND |
| 18 | VCCIB7 |
| 19 | IO122PPB7V0 |
| 20 | IO121PSB7V0 |
| 21 | IO122NPB7V0 |
| 22 | GFC1/IO120PSB7V0 |
| 23 | GFB1/IO119PDB7V0 |
| 24 | GFB0/IO119NDB7V0 |
| 25 | VCOMPLF |
| 26 | GFA0/IO118NPB6V1 |
| 27 | VCCPLF |
| 28 | GFA1/IO118PPB6V1 |
| 29 | GND |
| 30 | GFA2/IO117PDB6V1 |
| 31 | IO117NDB6V1 |
| 32 | GFB2/IO116PPB6V1 |
| 33 | GFC2/IO115PPB6V1 |
| 34 | IO116NPB6V1 |
| 35 | IO115NPB6V1 |
| 36 | VCC |
| 37 | IO112PDB6V1 |
| 38 | IO112NDB6V1 |
| 39 | IO108PSB6V0 |
| 40 | VCCIB6 |
| 41 | GND |
| 42 | IO106PDB6V0 |
| 43 | IO106NDB6V0 |
| 44 | GEC1/IO104PDB6V0 |
| 45 | GEC0/IO104NDB6V0 |
| 46 | GEB1/IO103PPB6V0 |
| 47 | GEA1/IO102PPB6V0 |
| 48 | GEB0/IO103NPB6V0 |
| 49 | GEA0/IO102NPB6V0 |
| 50 | VMV6 |
| 51 | GNDQ |
| 52 | GND |
| 53 | VMV5 |
| 54 | GNDQ |
| 55 | IO101NDB5V2 |
| 56 | GEA2/IO101PDB5V2 |
| 57 | IO100NDB5V2 |
| 58 | GEB2/IO100PDB5V2 |
| 59 | IO99NDB5V2 |
| 60 | GEC2/IO99PDB5V2 |
| 61 | IO98PSB5V2 |
| 62 | VCCIB5 |
| 63 | IO96PSB5V2 |
| 64 | IO94NDB5V1 |
| 65 | GND |
| 66 | IO94PDB5V1 |
| 67 | IO92NDB5V1 |
| 68 | IO92PDB5V1 |
| 69 | IO88NDB5V0 |
| 70 | IO88PDB5V0 |
| 71 | VCC |
| 72 | VCCIB5 |
| 73 | IO85NPB5V0 |
| 74 | IO84NPB5V0 |
| 75 | IO85PPB5V0 |
| 76 | IO84PPB5V0 |
| 77 | IO83NPB5V0 |
| 78 | IO82NPB5V0 |
| 79 | IO83PPB5V0 |
| 80 | IO82PPB5V0 |
| 81 | GND |
| 82 | IO80NDB4V1 |
| 83 | IO80PDB4V1 |
| 84 | IO79NPB4V1 |
| 85 | IO78NPB4V1 |
| 86 | IO79PPB4V1 |
| 87 | IO78PPB4V1 |
| 88 | VCC |
| 89 | VCCIB4 |
| 90 | IO76NDB4V1 |
| 91 | IO76PDB4V1 |
| 92 | IO72NDB4V0 |
| 93 | IO72PDB4V0 |
| 94 | IO70NDB4V0 |
| 95 | GDC2/IO70PDB4V0 |
| 96 | IO68NDB4V0 |
| 97 | GND |
| 98 | GDA2/IO68PDB4V0 |
| 99 | GDB2/IO69PSB4V0 |
| 100 | GNDQ |
| 101 | TCK |
| 102 | TDI |
| 103 | TMS |
| 104 | VMV4 |
| 105 | GND |
| 106 | VPUMP |
| 107 | GNDQ |

| PQ208 | |
|---|---|
| **Pin Number** | **A3PE3000 Function** |
| 118 | IO134NDB3V2 |
| 119 | IO134PDB3V2 |
| 120 | IO132NDB3V2 |
| 121 | IO132PDB3V2 |
| 122 | GND |
| 123 | VCCIB3 |
| 124 | GCC2/IO117PSB3V0 |
| 125 | GCB2/IO116PSB3V0 |
| 126 | NC |
| 127 | IO115NDB3V0 |
| 128 | GCA2/IO115PDB3V0 |
| 129 | GCA1/IO114PPB3V0 |
| 130 | GND |
| 131 | VCCPLC |
| 132 | GCA0/IO114NPB3V0 |
| 133 | VCOMPLC |
| 134 | GCB0/IO113NDB2V3 |
| 135 | GCB1/IO113PDB2V3 |
| 136 | GCC1/IO112PSB2V3 |
| 137 | IO110NDB2V3 |
| 138 | IO110PDB2V3 |
| 139 | IO106PSB2V3 |
| 140 | VCCIB2 |
| 141 | GND |
| 142 | VCC |
| 143 | IO99NDB2V2 |
| 144 | IO99PDB2V2 |
| 145 | IO96NDB2V1 |
| 146 | IO96PDB2V1 |
| 147 | IO91NDB2V1 |
| 148 | IO91PDB2V1 |
| 149 | IO88NDB2V0 |
| 150 | IO88PDB2V0 |
| 151 | GBC2/IO84PSB2V0 |
| 152 | GBA2/IO82PSB2V0 |
| 153 | GBB2/IO83PSB2V0 |
| 154 | VMV2 |
| 155 | GNDQ |
| 156 | GND |
| 157 | VMV1 |
| 158 | GNDQ |
| 159 | GBA1/IO81PDB1V4 |
| 160 | GBA0/IO81NDB1V4 |
| 161 | GBB1/IO80PDB1V4 |
| 162 | GND |
| 163 | GBB0/IO80NDB1V4 |
| 164 | GBC1/IO79PDB1V4 |
| 165 | GBC0/IO79NDB1V4 |
| 166 | IO74PDB1V4 |
| 167 | IO74NDB1V4 |
| 168 | IO70PDB1V3 |
| 169 | IO70NDB1V3 |
| 170 | VCCIB1 |
| 171 | VCC |
| 172 | IO56PSB1V1 |
| 173 | IO55PDB1V1 |
| 174 | IO55NDB1V1 |
| 175 | IO54PDB1V1 |
| 176 | IO54NDB1V1 |
| 177 | IO40PDB0V4 |
| 178 | GND |
| 179 | IO40NDB0V4 |
| 180 | IO37PDB0V4 |
| 181 | IO37NDB0V4 |
| 182 | IO35PDB0V4 |
| 183 | IO35NDB0V4 |
| 184 | IO32PDB0V3 |
| 185 | IO32NDB0V3 |
| 186 | VCCIB0 |
| 187 | VCC |
| 188 | IO28PDB0V3 |
| 189 | IO28NDB0V3 |
| 190 | IO24PDB0V2 |
| 191 | IO24NDB0V2 |
| 192 | IO21PSB0V2 |
| 193 | IO16PDB0V1 |
| 194 | IO16NDB0V1 |
| 195 | GND |
| 196 | IO11PDB0V1 |
| 197 | IO11NDB0V1 |
| 198 | IO08PDB0V0 |
| 199 | IO08NDB0V0 |
| 200 | VCCIB0 |
| 201 | GAC1/IO02PDB0V0 |
| 202 | GAC0/IO02NDB0V0 |
| 203 | GAB1/IO01PDB0V0 |
| 204 | GAB0/IO01NDB0V0 |
| 205 | GAA1/IO00PDB0V0 |
| 206 | GAA0/IO00NDB0V0 |
| 207 | GNDQ |
| 208 | VMV0 |

| FG324 | |
|---|---|
| **Pin Number** | **A3PE3000 FBGA** |
| G1 | GND |
| G2 | IO287PDB7V1 |
| G3 | IO287NDB7V1 |
| G4 | IO283PPB7V1 |
| G5 | VCCIB7 |
| G6 | IO279PDB7V0 |
| G7 | IO291NPB7V2 |
| G8 | VCC |
| G9 | IO26NDB0V3 |
| G10 | IO34NDB0V4 |
| G11 | VCC |
| G12 | IO94NPB2V1 |
| G13 | IO98PDB2V2 |
| G14 | VCCIB2 |
| G15 | GCC0/IO112NPB2V3 |
| G16 | IO104PDB2V2 |
| G17 | IO104NDB2V2 |
| G18 | GND |
| H1 | IO267PDB6V4 |
| H2 | VCCIB7 |
| H3 | IO283NPB7V1 |
| H4 | GFB1/IO274PPB7V0 |
| H5 | GND |
| H6 | IO279NDB7V0 |
| H7 | VCC |
| H8 | VCC |
| H9 | GND |
| H10 | GND |
| H11 | VCC |
| H12 | VCC |
| H13 | IO98NDB2V2 |
| H14 | GND |
| H15 | GCB1/IO113PDB2V3 |
| H16 | GCC1/IO112PPB2V3 |
| H17 | VCCIB2 |
| H18 | IO108PDB2V3 |

| FG324 | |
|---|---|
| **Pin Number** | **A3PE3000 FBGA** |
| J1 | IO267NDB6V4 |
| J2 | GFA0/IO273NDB6V4 |
| J3 | VCOMPLF |
| J4 | GFA2/IO272PDB6V4 |
| J5 | GFB0/IO274NPB7V0 |
| J6 | GFC0/IO275NDB7V0 |
| J7 | GFC1/IO275PDB7V0 |
| J8 | GND |
| J9 | GND |
| J10 | GND |
| J11 | GND |
| J12 | GCA2/IO115PDB3V0 |
| J13 | GCA1/IO114PDB3V0 |
| J14 | GCA0/IO114NDB3V0 |
| J15 | GCB0/IO113NDB2V3 |
| J16 | VCOMPLC |
| J17 | IO120NPB3V0 |
| J18 | IO108NDB2V3 |
| K1 | IO263PDB6V3 |
| K2 | GFA1/IO273PDB6V4 |
| K3 | VCCPLF |
| K4 | IO272NDB6V4 |
| K5 | GFC2/IO270PPB6V4 |
| K6 | GFB2/IO271PDB6V4 |
| K7 | IO271NDB6V4 |
| K8 | GND |
| K9 | GND |
| K10 | GND |
| K11 | GND |
| K12 | IO115NDB3V0 |
| K13 | GCB2/IO116PDB3V0 |
| K14 | IO116NDB3V0 |
| K15 | GCC2/IO117PDB3V0 |
| K16 | VCCPLC |
| K17 | IO124NPB3V1 |
| K18 | IO120PPB3V0 |

| FG324 | |
|---|---|
| **Pin Number** | **A3PE3000 FBGA** |
| L1 | IO263NDB6V3 |
| L2 | VCCIB6 |
| L3 | IO259PDB6V3 |
| L4 | IO259NDB6V3 |
| L5 | GND |
| L6 | IO270NPB6V4 |
| L7 | VCC |
| L8 | VCC |
| L9 | GND |
| L10 | GND |
| L11 | VCC |
| L12 | VCC |
| L13 | IO132PDB3V2 |
| L14 | GND |
| L15 | IO117NDB3V0 |
| L16 | IO128NPB3V1 |
| L17 | VCCIB3 |
| L18 | IO124PPB3V1 |
| M1 | GND |
| M2 | IO255PDB6V2 |
| M3 | IO255NDB6V2 |
| M4 | IO251PPB6V2 |
| M5 | VCCIB6 |
| M6 | GEB0/IO235NDB6V0 |
| M7 | GEB1/IO235PDB6V0 |
| M8 | VCC |
| M9 | IO192PPB4V4 |
| M10 | IO154NPB4V0 |
| M11 | VCC |
| M12 | GDA0/IO153NPB3V4 |
| M13 | IO132NDB3V2 |
| M14 | VCCIB3 |
| M15 | IO134NDB3V2 |
| M16 | IO134PDB3V2 |
| M17 | IO128PPB3V1 |
| M18 | GND |

| FG484 | |
|---|---|
| **Pin Number** | **A3PE3000 Function** |
| A1 | GND |
| A2 | GND |
| A3 | VCCIB0 |
| A4 | IO10NDB0V1 |
| A5 | IO10PDB0V1 |
| A6 | IO16NDB0V1 |
| A7 | IO16PDB0V1 |
| A8 | IO18PDB0V2 |
| A9 | IO24PDB0V2 |
| A10 | IO28NDB0V3 |
| A11 | IO28PDB0V3 |
| A12 | IO46PDB1V0 |
| A13 | IO54PDB1V1 |
| A14 | IO56NDB1V1 |
| A15 | IO56PDB1V1 |
| A16 | IO64NDB1V2 |
| A17 | IO64PDB1V2 |
| A18 | IO72NDB1V3 |
| A19 | IO74NDB1V4 |
| A20 | VCCIB1 |
| A21 | GND |
| A22 | GND |
| AA1 | GND |
| AA2 | VCCIB6 |
| AA3 | IO228PDB5V4 |
| AA4 | IO224PDB5V3 |
| AA5 | IO218NDB5V3 |
| AA6 | IO218PDB5V3 |
| AA7 | IO212NDB5V2 |
| AA8 | IO212PDB5V2 |
| AA9 | IO198PDB5V0 |
| AA10 | IO198NDB5V0 |
| AA11 | IO188PPB4V4 |
| AA12 | IO180NDB4V3 |
| AA13 | IO180PDB4V3 |
| AA14 | IO170NDB4V2 |
| AA15 | IO170PDB4V2 |
| AA16 | IO166NDB4V1 |
| AA17 | IO166PDB4V1 |
| AA18 | IO160NDB4V0 |
| AA19 | IO160PDB4V0 |
| AA20 | IO158NPB4V0 |
| AA21 | VCCIB3 |
| AA22 | GND |
| AB1 | GND |
| AB2 | GND |
| AB3 | VCCIB5 |
| AB4 | IO216NDB5V2 |
| AB5 | IO216PDB5V2 |
| AB6 | IO210NDB5V2 |
| AB7 | IO210PDB5V2 |
| AB8 | IO208NDB5V1 |
| AB9 | IO208PDB5V1 |
| AB10 | IO197NDB5V0 |
| AB11 | IO197PDB5V0 |
| AB12 | IO174NDB4V2 |
| AB13 | IO174PDB4V2 |
| AB14 | IO172NDB4V2 |
| AB15 | IO172PDB4V2 |
| AB16 | IO168NDB4V1 |
| AB17 | IO168PDB4V1 |
| AB18 | IO162NDB4V1 |
| AB19 | IO162PDB4V1 |
| AB20 | VCCIB4 |
| AB21 | GND |
| AB22 | GND |
| B1 | GND |
| B2 | VCCIB7 |
| B3 | IO06PPB0V0 |
| B4 | IO08NDB0V0 |
| B5 | IO08PDB0V0 |
| B6 | IO14NDB0V1 |
| B7 | IO14PDB0V1 |
| B8 | IO18NDB0V2 |
| B9 | IO24NDB0V2 |
| B10 | IO34PDB0V4 |
| B11 | IO40PDB0V4 |
| B12 | IO46NDB1V0 |
| B13 | IO54NDB1V1 |
| B14 | IO62NDB1V2 |
| B15 | IO62PDB1V2 |
| B16 | IO68NDB1V3 |
| B17 | IO68PDB1V3 |
| B18 | IO72PDB1V3 |
| B19 | IO74PDB1V4 |
| B20 | IO76NPB1V4 |
| B21 | VCCIB2 |
| B22 | GND |
| C1 | VCCIB7 |
| C2 | IO303PDB7V3 |
| C3 | IO305PDB7V3 |
| C4 | IO06NPB0V0 |
| C5 | GND |
| C6 | IO12NDB0V1 |
| C7 | IO12PDB0V1 |
| C8 | VCC |
| C9 | VCC |
| C10 | IO34NDB0V4 |
| C11 | IO40NDB0V4 |
| C12 | IO48NDB1V0 |
| C13 | IO48PDB1V0 |
| C14 | VCC |
| C15 | VCC |
| C16 | IO70NDB1V3 |
| C17 | IO70PDB1V3 |
| C18 | GND |
| C19 | IO76PPB1V4 |
| C20 | IO88NDB2V0 |

| Revision | Changes | Page |
|---|---|---|
| Advance v0.5 (continued) | The "RESET" section was updated. | 2-25 |
| | The "RESET" section was updated. | 2-27 |
| | The "Introduction" of the "Introduction" section was updated. | 2-28 |
| | PCI-X 3.3 V was added to the Compatible Standards for 3.3 V in Table 2-11 • VCCI Voltages and Compatible Standards | 2-29 |
| | Table 2-35 • ProASIC3E I/O Features was updated. | 2-54 |
| | The "Double Data Rate (DDR) Support" section was updated to include information concerning implementation of the feature. | 2-32 |
| | The "Electrostatic Discharge (ESD) Protection" section was updated to include testing information. | 2-35 |
| | Level 3 and 4 descriptions were updated in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices. | 2-64 |
| | The notes in Table 2-45 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3E Devices were updated. | 2-64 |
| | The "Simultaneous Switching Outputs (SSOs) and Printed Circuit Board Layout" section is new. | 2-41 |
| | A footnote was added to Table 2-37 • Maximum I/O Frequency for Single-Ended and Differential I/Os in All Banks in ProASIC3E Devices (maximum drive strength and high slew selected). | 2-55 |
| | Table 2-48 • ProASIC3E I/O Attributes vs. I/O Standard Applications | 2-81 |
| | Table 2-55 • ProASIC3 I/O Standards—SLEW and Output Drive (OUT_DRIVE) Settings | 2-85 |
| | The "x" was updated in the "Pin Descriptions" section. | 2-50 |
| | The "VCC Core Supply Voltage" pin description was updated. | 2-50 |
| | The "VMVx I/O Supply Voltage (quiet)" pin description was updated to include information concerning leaving the pin unconnected. | 2-50 |
| | EXTFB was removed from Figure 2-24 • ProASIC3E CCC Options. | 2-24 |
| | The CCC Output Peak-to-Peak Period Jitter $F_{CCC\_OUT}$ was updated in Table 2-13 • ProASIC3E CCC/PLL Specification. | 2-30 |
| | EXTFB was removed from Figure 2-27 • CCC/PLL Macro. | 2-28 |
| | The LVPECL specification in Table 2-45 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3E Devices was updated. | 2-64 |
| | Table 2-15 • Levels of Hot-Swap Support was updated. | 2-34 |
| | The "Cold-Sparing Support" section was updated. | 2-34 |
| | "Electrostatic Discharge (ESD) Protection" section was updated. | 2-35 |
| | The VJTAG and I/O pin descriptions were updated in the "Pin Descriptions" section. | 2-50 |
| | The "VJTAG JTAG Supply Voltage" pin description was updated. | 2-50 |
| | The "VPUMP Programming Supply Voltage" pin description was updated to include information on what happens when the pin is tied to ground. | 2-50 |

| Revision | Changes | Page |
|---|---|---|
| Advance v0.3 (continued) | The "Methodology" section was updated. | 3-9 |
|  | The A3PE3000 "208-Pin PQFP" pin table was updated. | 4-6 |