Microchip Technology - M1A3PE1500-2PQG208 Datasheet

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	147
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3pe1500-2pqg208

Temperature Grade Offerings

Package	**A3PE600**	**A3PE1500**	**A3PE3000**
Cortex-M1 Devices		**M1A3PE1500**	**M1A3PE3000**
PQ208	C, I	C, I	C, I
FG256	C, I	–	–
FG324	–	–	C, I
FG484	C, I	C, I	C, I
FG676	–	C, I	–
FG896	–	–	C, I

Note: C = Commercial temperature range: 0°C to 70°C ambient temperature
I = Industrial temperature range: –40°C to 85°C ambient temperature

Speed Grade and Temperature Grade Matrix

Temperature Grade	**Std.**	**–1**	**–2**
C [1]	✓	✓	✓
I [2]	✓	✓	✓

Notes:

1. *C = Commercial temperature range: 0°C to 70°C ambient temperature*
2. *I = Industrial temperature range: –40°C to 85°C ambient temperature*

References made to ProASIC3E devices also apply to ARM-enabled ProASIC3E devices. The ARM-enabled part numbers start with M1 (Cortex-M1).

Contact your local Microsemi SoC Products Group representative for device availability: *www.microsemi.com/index.php?option=com_content&id=135&lang=en&view=article*.

Table of Contents

ProASIC3E Device Family Overview

ProASIC3E DC and Switching Characteristics

Pin Descriptions and Packaging

Package Pin Assignments

Datasheet Information

Advanced Architecture

The proprietary ProASIC3E architecture provides granularity comparable to standard-cell ASICs. The ProASIC3E device consists of five distinct and programmable architectural features (Figure 1-1 on page 3):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- Pro I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the ProASIC3E core tile as either a three-input lookup table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC family of third-generation architecture Flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

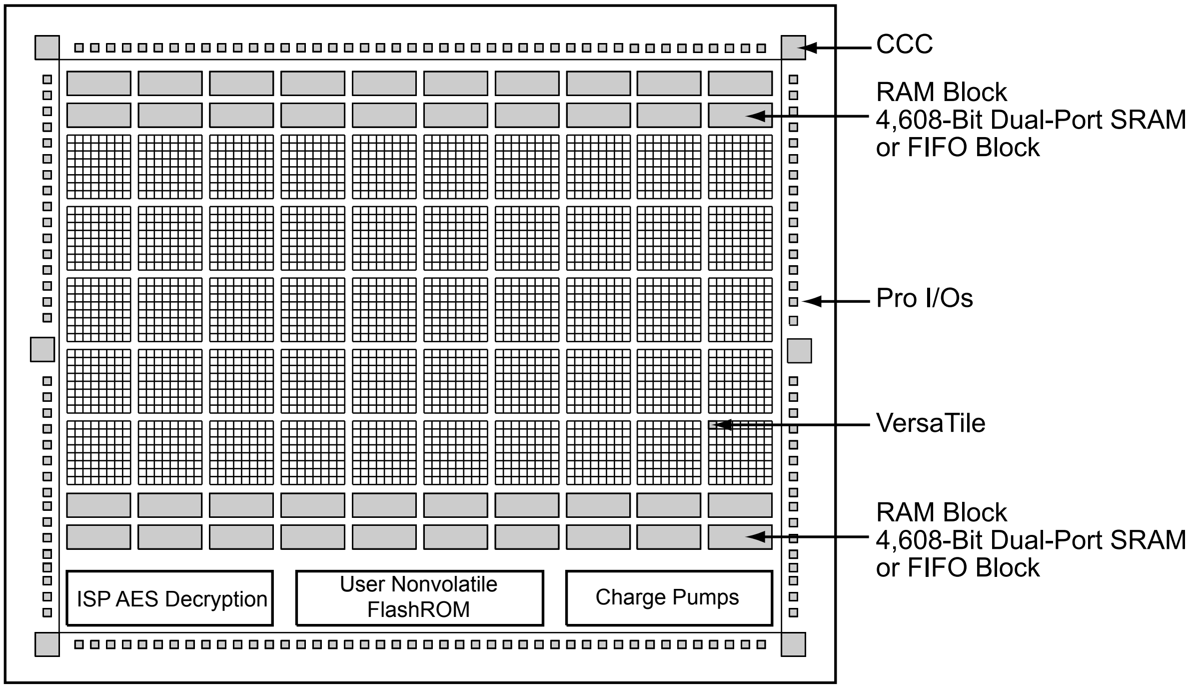

Figure 1-1 • **ProASIC3E Device Architecture Overview**

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLXL exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-1 on page 2-4 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *ProASIC3E FPGA Fabric User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

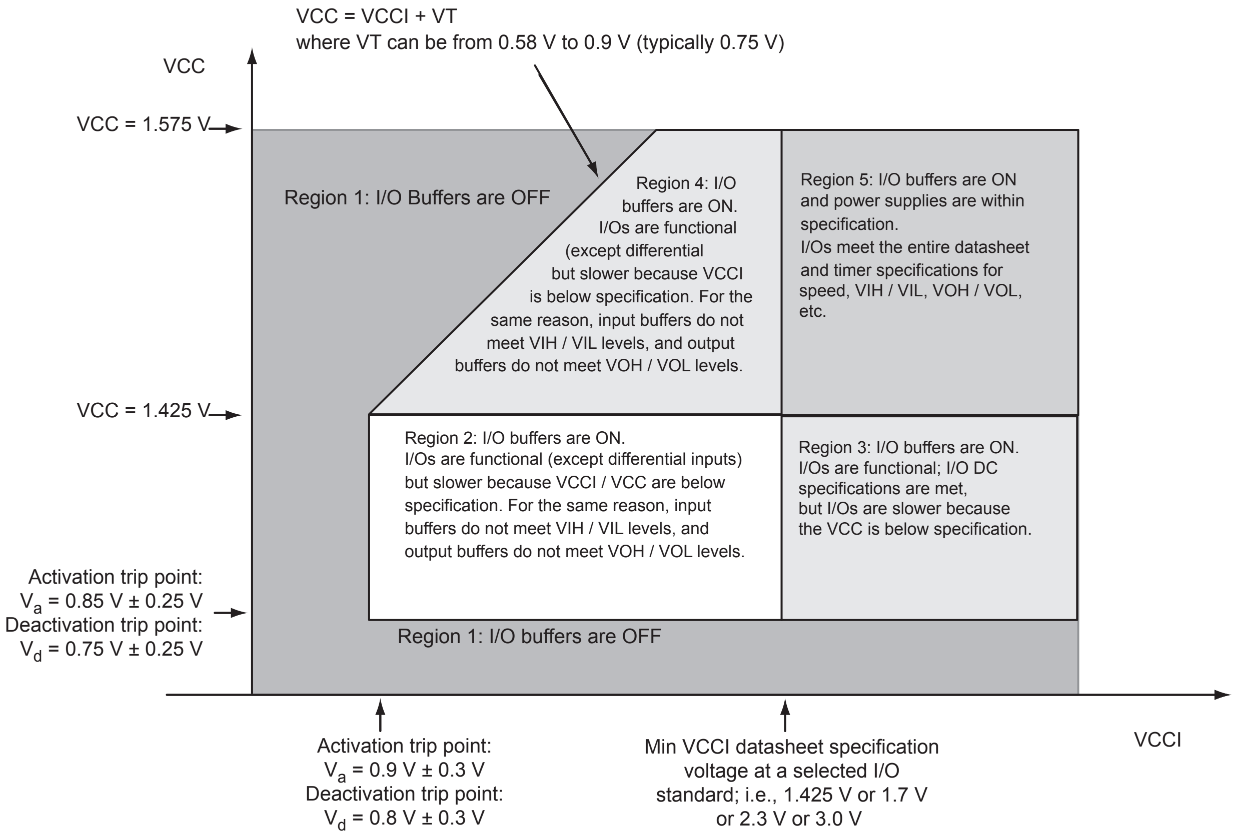

Figure 2-1 • **I/O State as a Function of VCCI and VCC Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 1

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 110°C. EQ 2 shows a sample calculation of the absolute maximum power dissipation allowed for an 896-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}\text{(°C/W)}} = \frac{110°\text{C} - 70°\text{C}}{13.6°\text{C/W}} = 5.88\text{ W}$$

EQ 2

Table 2-5 • **Package Thermal Resistivities**

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 200 ft./min.	θ_{ja} 500 ft./min.	Units
Plastic Quad Flat Package (PQFP)	208	8.0	26.1	22.5	20.8	C/W
Plastic Quad Flat Package (PQFP) with embedded heat spreader in A3PE3000	208	3.8	16.2	13.3	11.9	C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.9	22.8	21.5	C/W
	484	3.2	20.5	17.0	15.9	C/W
	676	3.2	16.4	13.0	12.0	C/W
	896	2.4	13.6	10.4	9.4	C/W

Temperature and Voltage Derating Factors

Table 2-6 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, VCC = 1.425 V)**

Array Voltage VCC (V)	Junction Temperature (°C) –40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.87	0.92	0.95	1.00	1.02	1.04
1.500	0.83	0.88	0.90	0.95	0.97	0.98
1.575	0.80	0.85	0.87	0.92	0.93	0.95

Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-11 on page 2-11.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-11 on page 2-11.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-11 on page 2-11.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-11 on page 2-11.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-12 on page 2-11.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = PAC11 * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in Table 2-12 on page 2-11.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-12 on page 2-11.

PLL Contribution—P_{PLL}

$P_{PLL} = PAC13 + PAC14 * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.[1]

---

[1] *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution (PAC14 * F_{CLKOUT} product) to the total PLL contribution.*

User I/O Characteristics

Timing Model

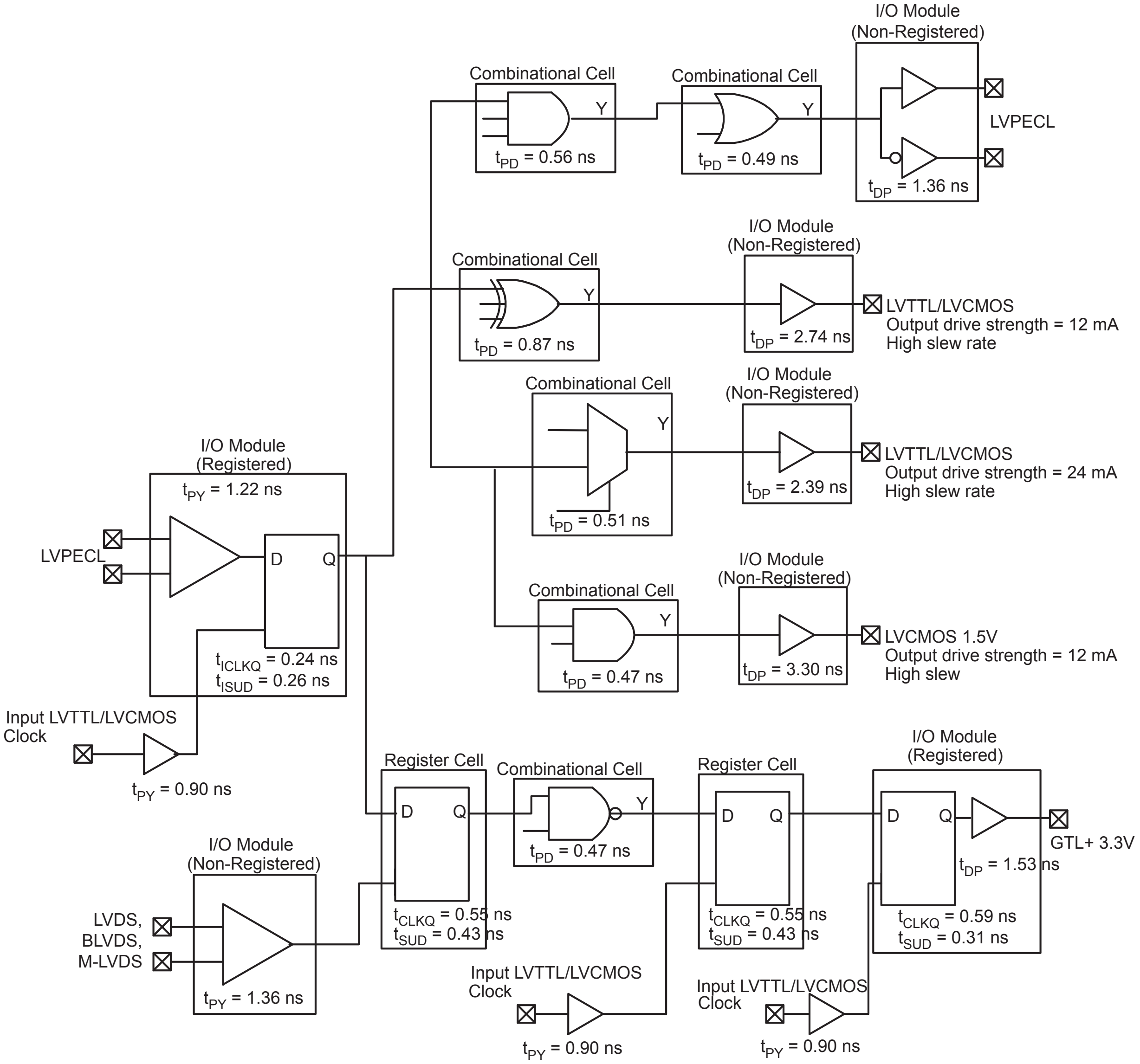

Figure 2-2 • **Timing Model**
Operating Conditions: –2 Speed, Commercial Temperature Range (T_J = 70°C), Worst-Case VCC = 1.425 V

Table 2-17 • **Summary of I/O Timing Characteristics—Software Default Settings**
–2 Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option)[1]	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)
3.3 V LVTTL / 3.3 V LVCMOS	12	12	High	35	–	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81
3.3 V LVCMOS Wide Range[2]	100 µA	12	High	35	–	0.49	4.24	0.03	1.36	1.78	0.32	4.24	3.25	3.78	4.17	6.77	5.79
2.5 V LVCMOS	12	12	High	35	–	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28
1.8 V LVCMOS	12	12	High	35	–	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98
1.5 V LVCMOS	12	12	High	35	–	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37
3.3 V PCI	Per PCI spec	–	High	10	25[3]	0.49	2.09	0.03	0.78	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16
3.3 V PCI-X	Per PCI-X spec	–	High	10	25[3]	0.49	2.09	0.03	0.78	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16
3.3 V GTL	20[4]	–	High	10	25	0.45	1.55	0.03	2.19	–	0.32	1.52	1.55	–	–	3.19	3.22
2.5 V GTL	20[4]	–	High	10	25	0.45	1.59	0.03	1.83	–	0.32	1.61	1.59	–	–	3.28	3.26
3.3 V GTL+	35	–	High	10	25	0.45	1.53	0.03	1.19	–	0.32	1.56	1.53	–	–	3.23	3.20
2.5 V GTL+	33	–	High	10	25	0.45	1.65	0.03	1.13	–	0.32	1.68	1.57	–	–	3.35	3.24
HSTL (I)	8	–	High	20	50	0.49	2.37	0.03	1.59	–	0.32	2.42	2.35	–	–	4.09	4.02
HSTL (II)	15[4]	–	High	20	25	0.49	2.26	0.03	1.59	–	0.32	2.30	2.03	–	–	3.97	3.70
SSTL2 (I)	15	–	High	30	50	0.49	1.59	0.03	1.00	–	0.32	1.62	1.38	–	–	3.29	3.05
SSTL2 (II)	18	–	High	30	25	0.49	1.62	0.03	1.00	–	0.32	1.65	1.32	–	–	3.32	2.99
SSTL3 (I)	14	–	High	30	50	0.49	1.72	0.03	0.93	–	0.32	1.75	1.37	–	–	3.42	3.04
SSTL3 (II)	21	–	High	30	25	0.49	1.54	0.03	0.93	–	0.32	1.57	1.25	–	–	3.24	2.92
LVDS/B-LVDS/ M-LVDS	24	–	High	–	–	0.49	1.40	0.03	1.36	–	–	–	–	–	–	–	–
LVPECL	24	–	High	–	–	0.49	1.36	0.03	1.22	–	–	–	–	–	–	–	–

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3V wide range as specified in the JESD8b specification.*
3. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-38 for connectivity. This resistor is not required during normal operation.*
4. *Output drive strength is below JEDEC specification.*
5. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5.*

***Table 2-28* • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
12 mA	Std.	0.66	6.03	0.04	1.20	1.57	0.43	6.14	5.02	3.28	3.47	8.37	7.26	ns
	–1	0.56	5.13	0.04	1.02	1.33	0.36	5.22	4.27	2.79	2.95	7.12	6.17	ns
	–2	0.49	4.50	0.03	0.90	1.17	0.32	4.58	3.75	2.45	2.59	6.25	5.42	ns
16 mA	Std.	0.66	5.62	0.04	1.20	1.57	0.43	5.72	4.72	3.32	3.58	7.96	6.96	ns
	–1	0.56	4.78	0.04	1.02	1.33	0.36	4.87	4.02	2.83	3.04	6.77	5.92	ns
	–2	0.49	4.20	0.03	0.90	1.17	0.32	4.27	3.53	2.48	2.67	5.94	5.20	ns
24 mA	Std.	0.66	5.24	0.04	1.20	1.57	0.43	5.34	4.69	3.39	3.96	7.58	6.93	ns
	–1	0.56	4.46	0.04	1.02	1.33	0.36	4.54	3.99	2.88	3.37	6.44	5.89	ns
	–2	0.49	3.92	0.03	0.90	1.17	0.32	3.99	3.50	2.53	2.96	5.66	5.17	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

***Table 2-40* • 1.8 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	15.84	0.04	1.45	1.91	0.43	15.65	15.84	2.78	1.58	17.89	18.07	ns
	–1	0.56	13.47	0.04	1.23	1.62	0.36	13.31	13.47	2.37	1.35	15.22	15.37	ns
	–2	0.49	11.83	0.03	1.08	1.42	0.32	11.69	11.83	2.08	1.18	13.36	13.50	ns
4 mA	Std.	0.66	11.39	0.04	1.45	1.91	0.43	11.60	10.76	3.26	2.77	13.84	12.99	ns
	–1	0.56	9.69	0.04	1.23	1.62	0.36	9.87	9.15	2.77	2.36	11.77	11.05	ns
	–2	0.49	8.51	0.03	1.08	1.42	0.32	8.66	8.03	2.43	2.07	10.33	9.70	ns
6 mA	Std.	0.66	8.97	0.04	1.45	1.91	0.43	9.14	8.10	3.57	3.36	11.37	10.33	ns
	–1	0.56	7.63	0.04	1.23	1.62	0.36	7.77	6.89	3.04	2.86	9.67	8.79	ns
	–2	0.49	6.70	0.03	1.08	1.42	0.32	6.82	6.05	2.66	2.51	8.49	7.72	ns
8 mA	Std.	0.66	8.35	0.04	1.45	1.91	0.43	8.50	7.59	3.64	3.52	10.74	9.82	ns
	–1	0.56	7.10	0.04	1.23	1.62	0.36	7.23	6.45	3.10	3.00	9.14	8.35	ns
	–2	0.49	6.24	0.03	1.08	1.42	0.32	6.35	5.66	2.72	2.63	8.02	7.33	ns
12 mA	Std.	0.66	7.94	0.04	1.45	1.91	0.43	8.09	7.56	3.74	4.11	10.32	9.80	ns
	–1	0.56	6.75	0.04	1.23	1.62	0.36	6.88	6.43	3.18	3.49	8.78	8.33	ns
	–2	0.49	5.93	0.03	1.08	1.42	0.32	6.04	5.65	2.79	3.07	7.71	7.32	ns
16 mA	Std.	0.66	7.94	0.04	1.45	1.91	0.43	8.09	7.56	3.74	4.11	10.32	9.80	ns
	–1	0.56	6.75	0.04	1.23	1.62	0.36	6.88	6.43	3.18	3.49	8.78	8.33	ns
	–2	0.49	5.93	0.03	1.08	1.42	0.32	6.04	5.65	2.79	3.07	7.71	7.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

***Table 2-54* • Minimum and Maximum DC Input and Output Levels**

3.3 V GTL+	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	μA[2]	μA[2]
35 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35	181	268	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

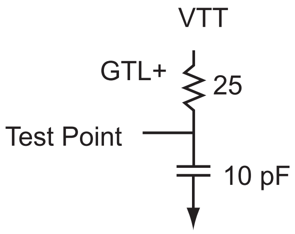

***Figure 2-14* • AC Loading**

***Table 2-55* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

***Table 2-56* • 3.3 V GTL+**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.60	2.06	0.04	1.59	0.43	2.09	2.06			4.33	4.29	ns
–1	0.51	1.75	0.04	1.35	0.36	1.78	1.75			3.68	3.65	ns
–2	0.45	1.53	0.03	1.19	0.32	1.56	1.53			3.23	3.20	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

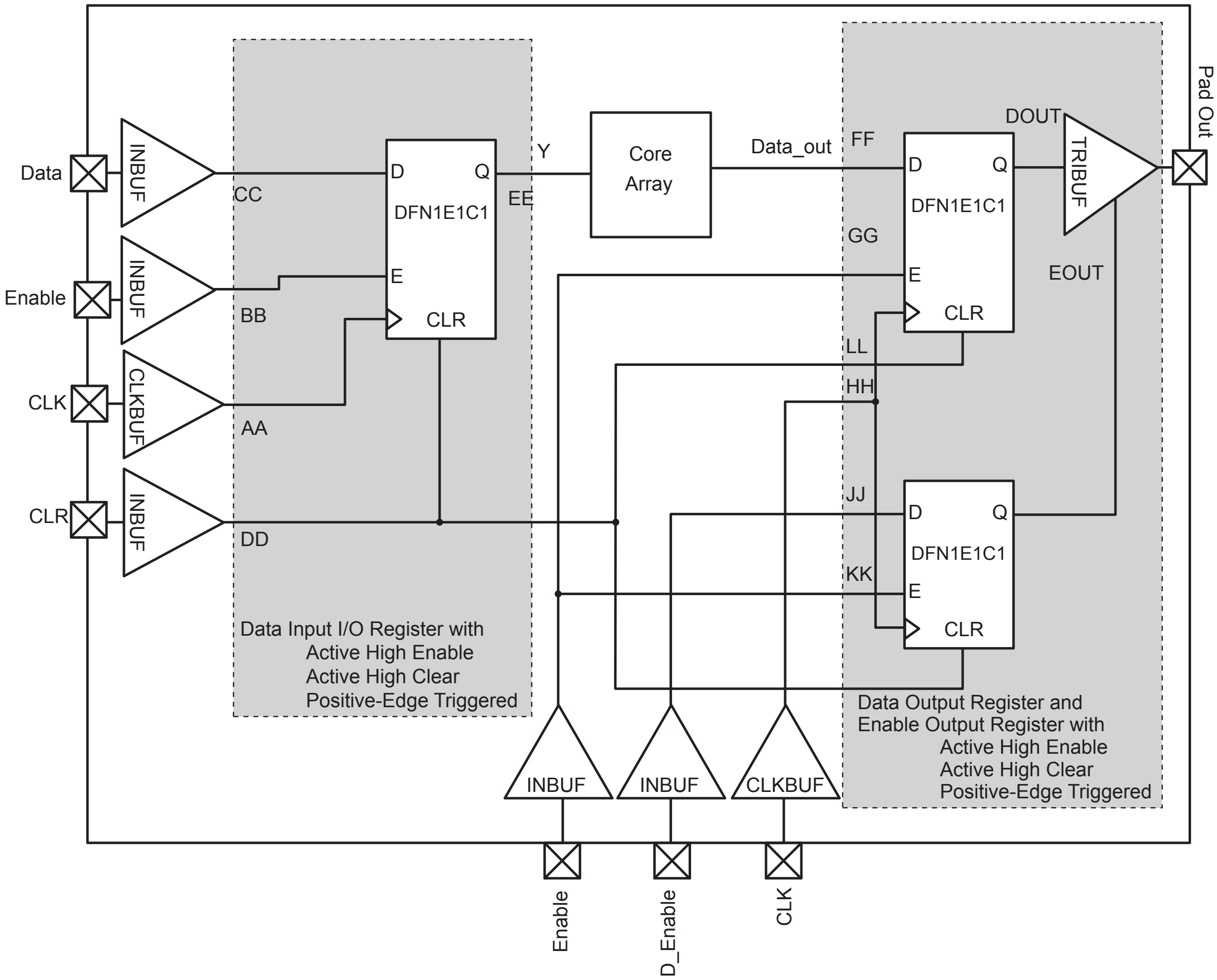

***Figure 2-26* • Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

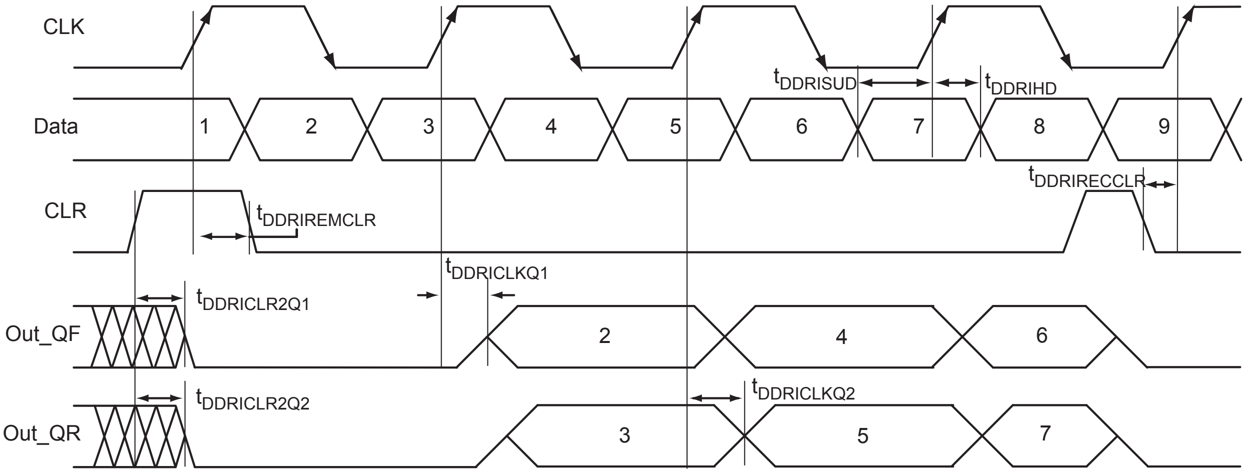

***Figure 2-31* • Input DDR Timing Diagram**

Timing Characteristics

***Table 2-90* • Input DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.39	0.44	0.52	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.27	0.31	0.37	ns
$t_{DDRISUD}$	Data Setup for Input DDR	0.28	0.32	0.38	ns
t_{DDRIHD}	Data Hold for Input DDR	0.00	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear to Out Out_QR for Input DDR	0.57	0.65	0.76	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.46	0.53	0.62	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.22	0.25	0.30	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.22	0.25	0.30	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.36	0.41	0.48	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.32	0.37	0.43	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	1404	1232	1048	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

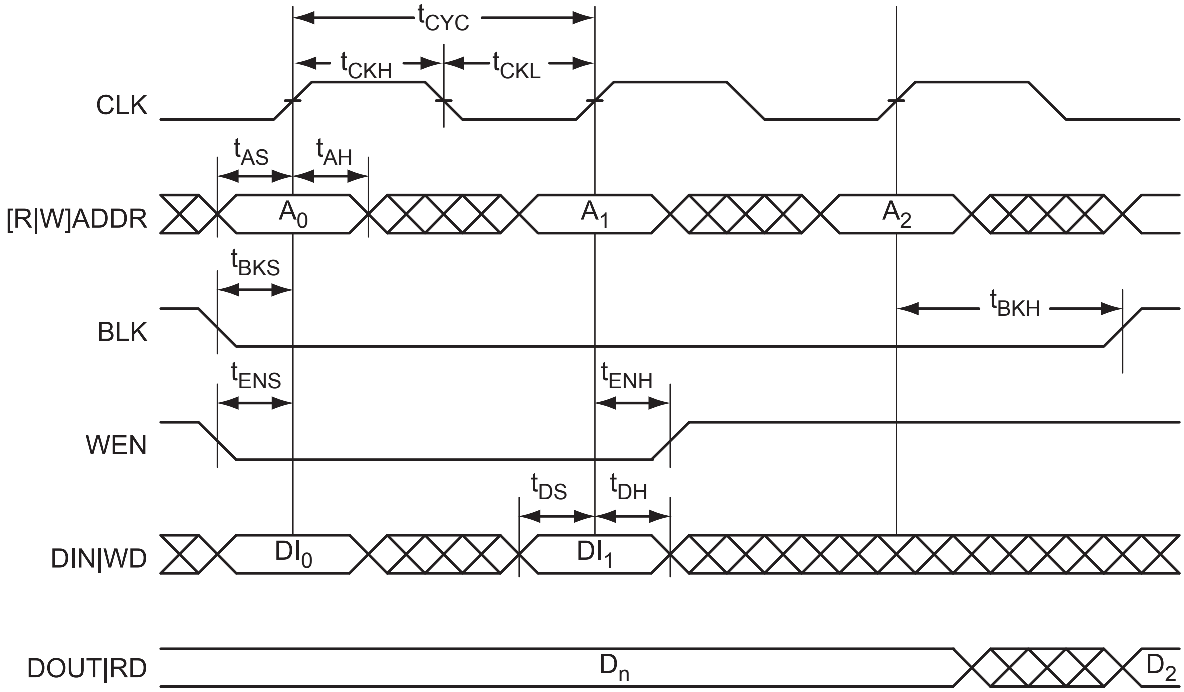

***Figure 2-43* • RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.**

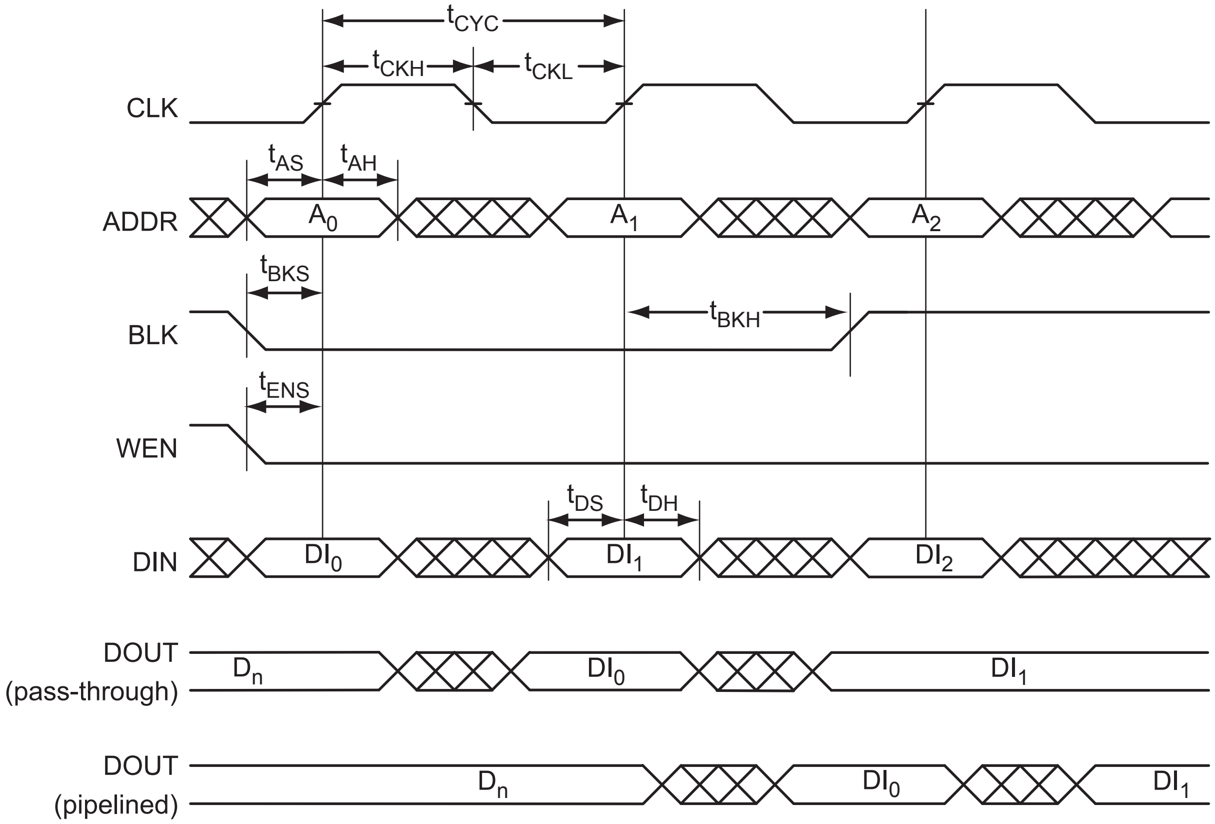

***Figure 2-44* • RAM Write, Output as Write Data. Applicable to RAM4K9 Only.**

Table 2-100 • RAM512X18
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.28	0.33	ns
t_{AH}	Address hold time	0.00	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.18	0.20	0.24	ns
t_{ENH}	REN, WEN hold time	0.06	0.07	0.08	ns
t_{DS}	Input data (WD) setup time	0.18	0.21	0.25	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	2.16	2.46	2.89	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	0.90	1.02	1.20	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.50	0.43	0.38	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge	0.59	0.50	0.44	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to data out Low on RD (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.21	0.24	0.29	ns
t_{CYC}	Clock cycle time	3.23	3.68	4.32	ns
F_{MAX}	Maximum frequency	310	272	231	MHz

Notes:

1. *For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

FIFO

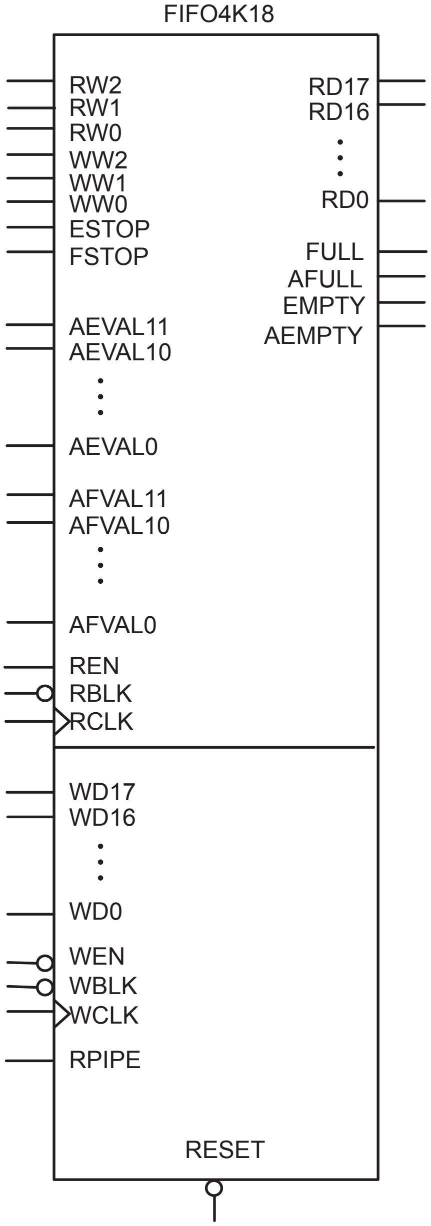

***Figure 2-46* • FIFO Model**

3 – Pin Descriptions and Packaging

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

VCCIBx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. In general, unused I/O banks should have their corresponding VCCIX pins tied to GND. If an output pad is terminated to ground through any resistor and if the corresponding VCCIX is left floating, then the leakage current to ground is ~ 0uA. However, if an output pad is terminated to ground through any resistor and the corresponding VCCIX grounded, then the leakage current to ground is ~ 3 uA. For unused banks the aforementioned behavior is to be taken into account while deciding if it’s better to float VCCIX of unused bank or tie it to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V.

When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *ProASIC3E FPGA Fabric User’s Guide* for a complete board solution for the PLL analog power supply and ground.

There are six VCCPLX pins on ProASIC3E devices.

VCOMPLA/B/C/D/E/F **PLL Ground**

Ground to analog PLL power supplies. When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There are six VCOMPL pins (PLL ground) on ProASIC3E devices.

FG484	
Pin Number	**A3PE1500 Function**
V15	IO112NDB4V0
V16	GDB2/IO112PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO105NDB3V2
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO165NDB5V3
W6	GEB2/IO165PDB5V3
W7	IO164NDB5V3
W8	IO153NDB5V2
W9	IO153PDB5V2
W10	IO147NDB5V1
W11	IO133NDB4V2
W12	IO130NDB4V2
W13	IO130PDB4V2
W14	IO113NDB4V0
W15	GDC2/IO113PDB4V0
W16	IO111NDB4V0
W17	GDA2/IO111PDB4V0
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB6
Y2	NC
Y3	NC
Y4	IO161NDB5V3
Y5	GND
Y6	IO163NDB5V3

FG484	
Pin Number	**A3PE1500 Function**
Y7	IO163PDB5V3
Y8	VCC
Y9	VCC
Y10	IO147PDB5V1
Y11	IO133PDB4V2
Y12	IO131NPB4V2
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB3

FG484	
Pin Number	**A3PE3000 Function**
C21	IO94PPB2V1
C22	VCCIB2
D1	IO293PDB7V2
D2	IO303NDB7V3
D3	IO305NDB7V3
D4	GND
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0
D7	GAB0/IO01NDB0V0
D8	IO20PDB0V2
D9	IO22PDB0V2
D10	IO30PDB0V3
D11	IO38NDB0V4
D12	IO52NDB1V1
D13	IO52PDB1V1
D14	IO66NDB1V3
D15	IO66PDB1V3
D16	GBB1/IO80PDB1V4
D17	GBA0/IO81NDB1V4
D18	GBA1/IO81PDB1V4
D19	GND
D20	IO88PDB2V0
D21	IO90PDB2V1
D22	IO94NPB2V1
E1	IO293NDB7V2
E2	IO299PPB7V3
E3	GND
E4	GAB2/IO308PDB7V4
E5	GAA2/IO309PDB7V4
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO20NDB0V2
E9	IO22NDB0V2
E10	IO30NDB0V3
E11	IO38PDB0V4
E12	IO44NDB1V0
E13	IO58NDB1V2
E14	IO58PDB1V2
E15	GBC1/IO79PDB1V4
E16	GBB0/IO80NDB1V4
E17	GNDQ
E18	GBA2/IO82PDB2V0
E19	IO86NDB2V0
E20	GND
E21	IO90NDB2V1
E22	IO98PDB2V2
F1	IO299NPB7V3
F2	IO301NDB7V3
F3	IO301PDB7V3
F4	IO308NDB7V4
F5	IO309NDB7V4
F6	VMV7
F7	VCCPLA
F8	GAC0/IO02NDB0V0
F9	GAC1/IO02PDB0V0
F10	IO32NDB0V3
F11	IO32PDB0V3
F12	IO44PDB1V0
F13	IO50NDB1V1
F14	IO60PDB1V2
F15	GBC0/IO79NDB1V4
F16	VCCPLB
F17	VMV2
F18	IO82NDB2V0
F19	IO86PDB2V0
F20	IO96PDB2V1
F21	IO96NDB2V1
F22	IO98NDB2V2
G1	IO289NDB7V1
G2	IO289PDB7V1
G3	IO291PPB7V2
G4	IO295PDB7V2
G5	IO297PDB7V2
G6	GAC2/IO307PDB7V4
G7	VCOMPLA
G8	GNDQ
G9	IO26NDB0V3
G10	IO26PDB0V3
G11	IO36PDB0V4
G12	IO42PDB1V0
G13	IO50PDB1V1
G14	IO60NDB1V2
G15	GNDQ
G16	VCOMPLB
G17	GBB2/IO83PDB2V0
G18	IO92PDB2V1
G19	IO92NDB2V1
G20	IO102PDB2V2
G21	IO102NDB2V2
G22	IO105NDB2V2
H1	IO286PSB7V1
H2	IO291NPB7V2
H3	VCC
H4	IO295NDB7V2
H5	IO297NDB7V2
H6	IO307NDB7V4
H7	IO287PDB7V1
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO36NDB0V4
H12	IO42NDB1V0
H13	VCCIB1
H14	VCCIB1
H15	VMV1
H16	GBC2/IO84PDB2V0
H17	IO83NDB2V0
H18	IO100NDB2V2

Revision	Changes	Page
Revision 3 (Apr 2008) Packaging v1.2	The following pins had duplicates and the extra pins were deleted from the "PQ208" A3PE3000 table: 36, 62, 171 Note: There were no pin function changes in this update.	4-2
	The following pins had duplicates and the extra pins were deleted from the "FG324" table: E2, E3, E16, E17, P2, P3, T16, U17 Note: There were no pin function changes in this update.	4-12
	The "FG256" pin table was updated for the A3PE600 device because the old PAT were based on the IFX die, and this is the final UMC die version.	4-9
	The "FG484" was updated for the A3PE600 device because the old PAT were based on the IFX die, and this is the final UMC die version.	4-22
	The following pins had duplicates and the extra pins were deleted from the "FG896" table: AD6, AE5, AE28, AF29, F5, F26, G6, G25 Note: There were no pin function changes in this update.	4-41
Revision 2 (Mar 2008) Product Brief rev. 1	The FG324 package was added to the "ProASIC3E Product Family" table, the "I/Os Per Package1" table, and the "Temperature Grade Offerings" table for A3PE3000.	I, II, IV
Revision 1 (Feb 2008) DC and Switching Characteristics v1.1	In Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature 1, Maximum Operating Junction Temperature was changed from 110°C to 100°C for both commercial and industrial grades.	2
	The "PLL Behavior at Brownout Condition" section is new.	2-4
	In the "PLL Contribution—PPLL" section, the following was deleted: FCLKIN is the input clock frequency.	2-10
	In Table 2-14 • Summary of Maximum and Minimum DC Input Levels, the note was incorrect. It previously said T_J and it was corrected and changed to T_A.	2-17
	In Table 2-98 • ProASIC3E CCC/PLL Specification, the SCLK parameter and note 1 are new.	2-70
	Table 2-103 • JTAG 1532 was populated with the parameter data, which was not in the previous version of the document.	2-83
Revision 1 (cont'd) Packaging v1.1	The "PQ208" pin table for A3PE3000 was updated.	4-2
	The "FG324" pin table for A3PE3000 is new.	4-13
	The "FG484" pin table for A3PE3000 is new.	4-17
	The "FG896" pin table for A3PE3000 is new.	4-41
Revision 0 (Jan 2008)	This document was previously in datasheet v2.1. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is 51700098-001-0.	N/A
v2.1 (July 2007)	CoreMP7 information was removed from the "Features and Benefits" section.	1-I
	The M1 device part numbers have been updated in ProASIC3E Product Family, "Packaging Tables", "Temperature Grade Offerings", "Speed Grade and Temperature Grade Matrix", and "Speed Grade and Temperature Grade Matrix".	1-I