



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	147
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3pe1500-2pqg208i

I/Os Per Package¹

ProASIC3E Devices	A3PE600		A3PE1500 ³		A3PE3000 ³	
Cortex-M1 Devices ²			M1A3PE1500		M1A3PE3000	
	I/O Types					
	Single-Ended I/O ¹	Differential I/O Pairs	Single-Ended I/O ¹	Differential I/O Pairs	Single-Ended I/O ¹	Differential I/O Pairs
Package						
PQ208	147	65	147	65	147	65
FG256	165	79	–	–	–	–
FG324	–	–	–	–	221	110
FG484	270	135	280	139	341	168
FG676	–	–	444	222	–	–
FG896	–	–	–	–	620	310

Notes:

- When considering migrating your design to a lower- or higher-density device, refer to the [ProASIC3E FPGA Fabric User's Guide](#) to ensure compliance with design and board migration requirements.
- Each used differential I/O pair reduces the number of single-ended I/Os available by two.
- For A3PE1500 and A3PE3000 devices, the usage of certain I/O standards is limited as follows:
 - SSTL3(I) and (II): up to 40 I/Os per north or south bank
 - LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank
 - SSTL2(I) and (II) / GTL+ 2.5 V / GTL 2.5 V: up to 72 I/Os per north or south bank
- FG256 and FG484 are footprint-compatible packages.
- When using voltage-referenced I/O standards, one I/O pin should be assigned as a voltage-referenced pin (VREF) per minibank (group of I/Os).
- "G" indicates RoHS-compliant packages. Refer to the ["ProASIC3E Ordering Information"](#) on page III for the location of the "G" in the part number.

Table 1-2 • ProASIC3E FPGAs Package Sizes Dimensions

Package	PQ208	FG256	FG324	FG484	FG676	FG896
Length × Width (mm\mm)	28 × 28	17 × 17	19 × 19	23 × 23	27 × 27	31 × 31
Nominal Area (mm ²)	784	289	361	529	729	961
Pitch (mm)	0.5	1.0	1.0	1.0	1.0	1.0
Height (mm)	3.40	1.60	1.63	2.23	2.23	2.23

ProASIC3E Device Status

ProASIC3E Devices	Status	M1 ProASIC3E Devices	Status
A3PE600	Production		
A3PE1500	Production	M1A3PE1500	Production
A3PE3000	Production	M1A3PE3000	Production

Calculating Power Dissipation

Quiescent Supply Current

Table 2-7 • Quiescent Supply Current Characteristics

	A3PE600	A3PE1500	A3PE3000
Typical (25°C)	5 mA	12 mA	25 mA
Maximum (Commercial)	30 mA	70 mA	150 mA
Maximum (Industrial)	45 mA	105 mA	225 mA

Notes:

1. *IDD* Includes *VCC*, *VPUMP*, *VCCI*, and *VMV* currents. Values do not include I/O static contribution, which is shown in [Table 2-8](#) and [Table 2-9](#) on [page 2-7](#).
2. *-F* speed grade devices may experience higher standby *IDD* of up to five times the standard *IDD* and higher I/O leakage.

Power per I/O Pin

Table 2-8 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings

	VMV (V)	Static Power PDC2 (mW) ¹	Dynamic Power PAC9 (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL/LVCMOS	3.3	–	17.39
3.3 V LVTTTL/LVCMOS – Schmitt trigger	3.3	–	25.51
3.3 V LVTTTL/LVCMOS Wide Range ³	3.3	–	16.34
3.3 V LVTTTL/LVCMOS Wide Range – Schmitt trigger ³	3.3	–	24.49
2.5 V LVCMOS	2.5	–	5.76
2.5 V LVCMOS – Schmitt trigger	2.5	–	7.16
1.8 V LVCMOS	1.8	–	2.72
1.8 V LVCMOS – Schmitt trigger	1.8	–	2.80
1.5 V LVCMOS (JESD8-11)	1.5	–	2.08
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	2.00
3.3 V PCI	3.3	–	18.82
3.3 V PCI – Schmitt trigger	3.3	–	20.12
3.3 V PCI-X	3.3	–	18.82
3.3 V PCI-X – Schmitt trigger	3.3	–	20.12
Voltage-Referenced			
3.3 V GTL	3.3	2.90	8.23
2.5 V GTL	2.5	2.13	4.78
3.3 V GTL+	3.3	2.81	4.14
2.5 V GTL+	2.5	2.57	3.71

Notes:

1. *PDC2* is the static power (where applicable) measured on *VMV*.
2. *PAC9* is the total dynamic power measured on *VCC* and *VMV*.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.

Combinatorial Cells Contribution— P_{C-CELL}

$$P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-11 on page 2-11](#).

F_{CLK} is the global clock signal frequency.

Routing Net Contribution— P_{NET}

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-11 on page 2-11](#).

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution— P_{INPUTS}

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-11 on page 2-11](#).

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution— $P_{OUTPUTS}$

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-11 on page 2-11](#).

β_1 is the I/O buffer enable rate—guidelines are provided in [Table 2-12 on page 2-11](#).

F_{CLK} is the global clock signal frequency.

RAM Contribution— P_{MEMORY}

$$P_{MEMORY} = PAC11 * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in [Table 2-12 on page 2-11](#).

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in [Table 2-12 on page 2-11](#).

PLL Contribution— P_{PLL}

$$P_{PLL} = PAC13 + PAC14 * F_{CLKOUT}$$

F_{CLKOUT} is the output clock frequency.¹

1. The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($PAC14 * F_{CLKOUT}$ product) to the total PLL contribution.

Single-Ended I/O Characteristics

3.3 V LVTTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTTL support.

Table 2-25 • Minimum and Maximum DC Input and Output Levels

3.3 V LVTTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min., V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	−0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	−0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	−0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

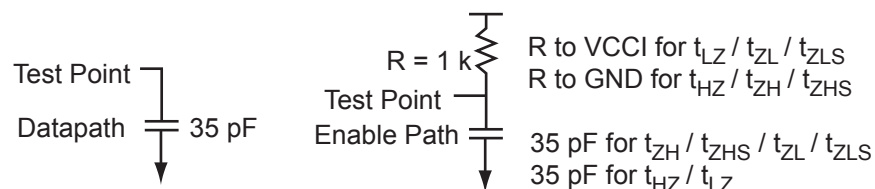


Figure 2-6 • AC Loading

Table 2-26 • 3.3 V LVTTTL / 3.3 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	3.3	1.4	–	35

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-60 • Minimum and Maximum DC Input and Output Levels

HSTL Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
8 mA	−0.3	VREF − 0.1	VREF + 0.1	3.6	0.4	VCCI − 0.4	8	8	39	32	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.

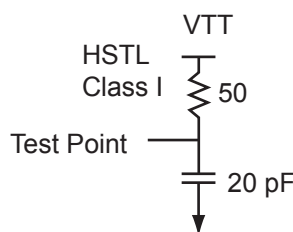


Figure 2-16 • AC Loading

Table 2-61 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF − 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-62 • HSTL Class I

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = .4 V, VREF = 0.75 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.66	3.18	0.04	2.12	0.43	3.24	3.14			5.47	5.38	ns
−1	0.56	2.70	0.04	1.81	0.36	2.75	2.67			4.66	4.58	ns
−2	0.49	2.37	0.03	1.59	0.32	2.42	2.35			4.09	4.02	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Table 2-84 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{iCLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{iSUD}	Data Setup Time for the Input Data Register	C, A
t_{iHD}	Data Hold Time for the Input Data Register	C, A
t_{iSUE}	Enable Setup Time for the Input Data Register	B, A
t_{iHE}	Enable Hold Time for the Input Data Register	B, A
t_{iPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{iREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{iRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: *See Figure 2-25 on page 2-53 for more information.

Input Register

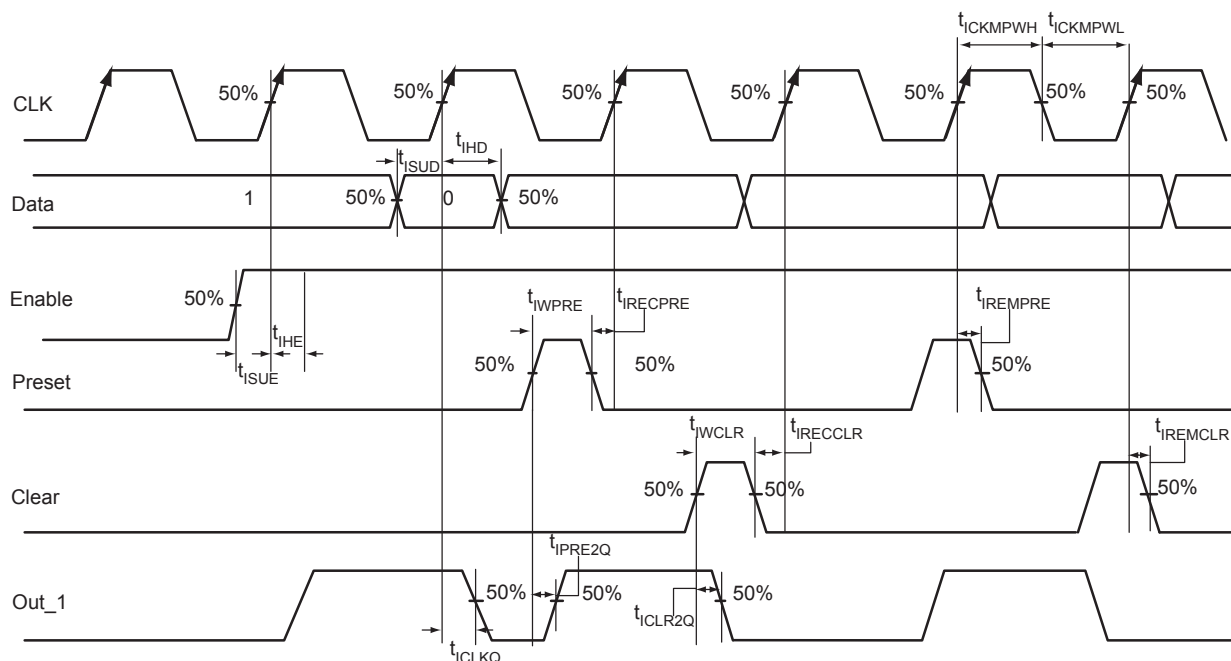


Figure 2-27 • Input Register Timing Diagram

Timing Characteristics

Table 2-86 • Input Data Register Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.27	0.32	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.26	0.30	0.35	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.37	0.42	0.50	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.45	0.52	0.61	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.45	0.52	0.61	ns
t_{IEMCLR}	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	0.00	ns
t_{IRECCLR}	Asynchronous Clear Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
t_{IREMPRE}	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	0.00	ns
t_{IRECPRE}	Asynchronous Preset Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
t_{ICKMPWH}	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.41	0.48	ns
t_{ICKMPWL}	Clock Minimum Pulse Width Low for the Input Data Register	0.32	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

DDR Module Specifications

Input DDR Module

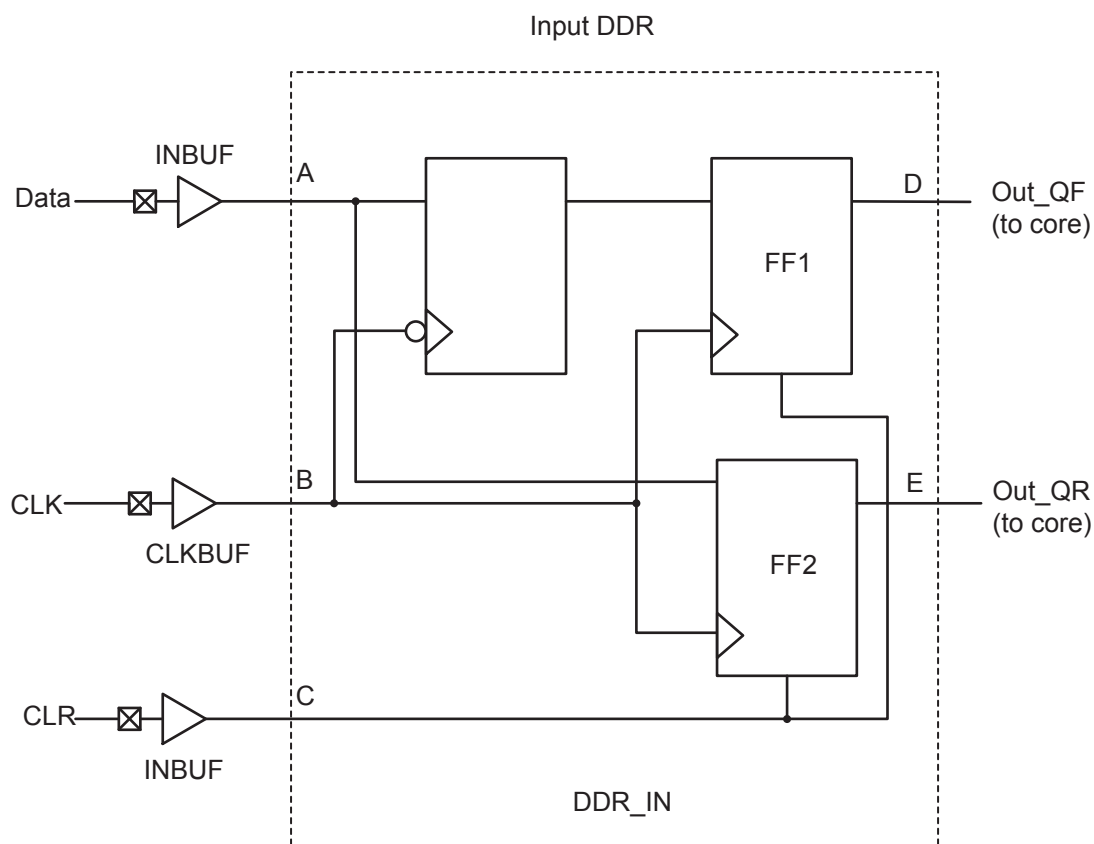


Figure 2-30 • Input DDR Timing Model

Table 2-89 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

Timing Characteristics

Table 2-95 • A3PE600 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2		-1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	0.83	1.04	0.94	1.18	1.11	1.39	ns
t_{RCKH}	Input High Delay for Global Clock	0.81	1.06	0.93	1.21	1.09	1.42	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.25		0.28		0.33	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

Table 2-96 • A3PE1500 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2		-1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.07	1.29	1.22	1.47	1.43	1.72	ns
t_{RCKH}	Input High Delay for Global Clock	1.06	1.32	1.21	1.50	1.42	1.76	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

Table 2-97 • A3PE3000 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2		-1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.41	1.62	1.60	1.85	1.88	2.17	ns
t_{RCKH}	Input High Delay for Global Clock	1.40	1.66	1.59	1.89	1.87	2.22	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.35	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-98 • ProASIC3E CCC/PLL Specification

Parameter	Minimum	Typical	Maximum	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		350	MHz
Delay Increments in Programmable Delay Blocks ^{1, 2}		160 ³		ps
Serial Clock (SCLK) for Dynamic PLL ⁴			125	MHz
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Max Peak-to-Peak Period Jitter			
	1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%		0.70%	
24 MHz to 100 MHz	1.00%		1.20%	
100 MHz to 250 MHz	1.75%		2.00%	
250 MHz to 350 MHz	2.50%		5.60%	
Acquisition Time	LockControl = 0		300	μs
	LockControl = 1		6.0	ms
Tracking Jitter ⁵	LockControl = 0		1.6	ns
	LockControl = 1		0.8	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 ^{1, 2}	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2 ^{1, 2}	0.025		5.56	ns
Delay Range in Block: Fixed Delay ^{1, 4}		2.2		ns

Notes:

1. This delay is a function of voltage and temperature. See [Table 2-6 on page 2-5](#) for deratings
2. $T_J = 25^\circ\text{C}$, $V_{CC} = 1.5\text{ V}$.
3. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help for more information.
4. Maximum value obtained for a –2 speed-grade device in worst-case commercial conditions. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.
5. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.

Timing Characteristics

Table 2-99 • RAM4K9

Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	Units
t_{AS}	Address setup time	0.25	0.28	0.33	ns
t_{AH}	Address hold time	0.00	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.14	0.16	0.19	ns
t_{ENH}	REN, WEN hold time	0.10	0.11	0.13	ns
t_{BKS}	BLK setup time	0.23	0.27	0.31	ns
t_{BKH}	BLK hold time	0.02	0.02	0.02	ns
t_{DS}	Input data (DIN) setup time	0.18	0.21	0.25	ns
t_{DH}	Input data (DIN) hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	1.79	2.03	2.39	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.36	2.68	3.15	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	0.89	1.02	1.20	ns
t_{C2CWWL}^1	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Closing Edge	0.33	0.28	0.25	ns
t_{C2CWWH}^1	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge	0.30	0.26	0.23	ns
t_{C2CRWH}^1	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.45	0.38	0.34	ns
t_{C2CWRH}^1	Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge	0.49	0.42	0.37	ns
t_{RSTBQ}	RESET Low to data out Low on DO (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on DO (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.21	0.24	0.29	ns
t_{CYC}	Clock cycle time	3.23	3.68	4.32	ns
F_{MAX}	Maximum frequency	310	272	231	MHz

Notes:

1. For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

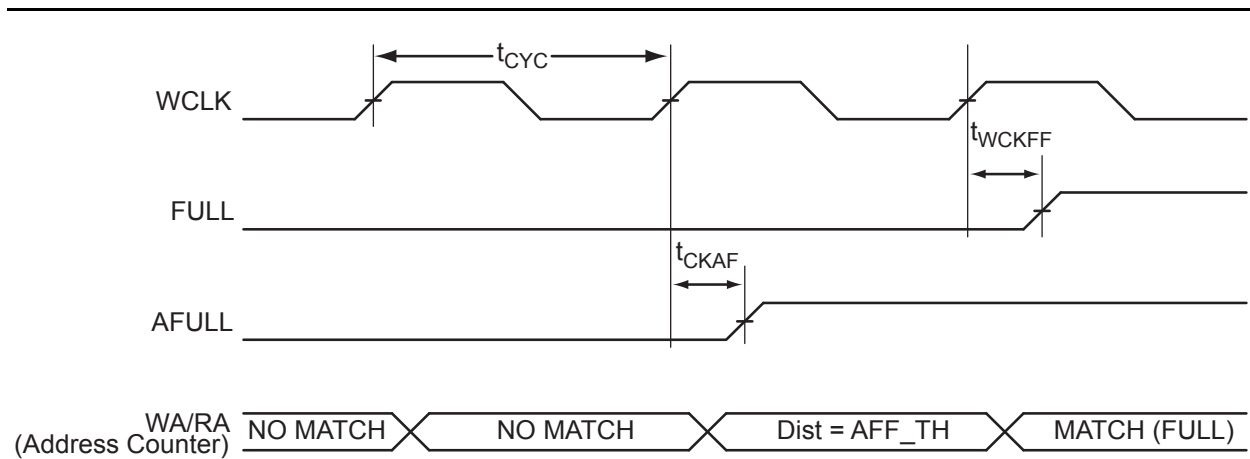


Figure 2-51 • FIFO FULL Flag and AFULL Flag Assertion

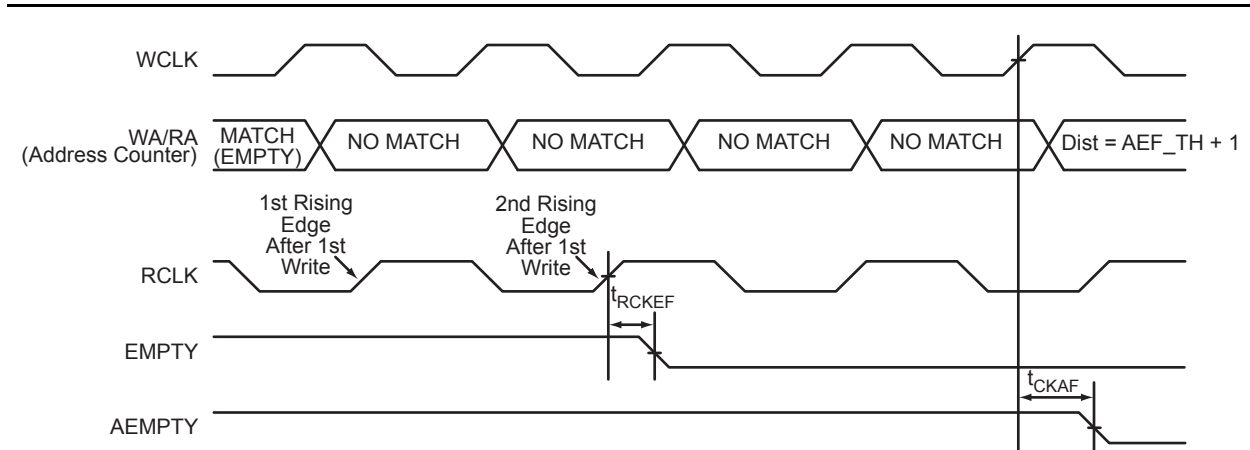


Figure 2-52 • FIFO EMPTY Flag and AEMPTY Flag Deassertion

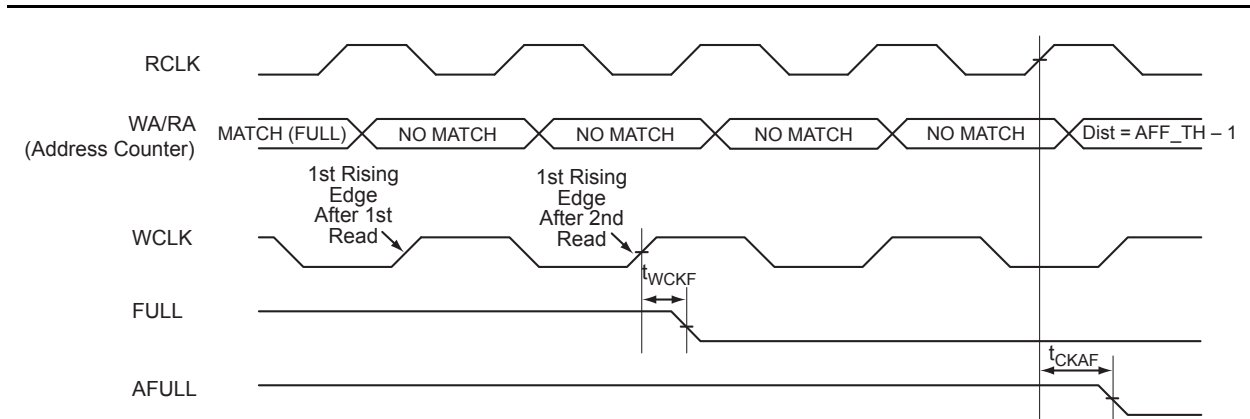


Figure 2-53 • FIFO FULL Flag and AFULL Flag Deassertion

Timing Characteristics

Table 2-101 • FIFO
Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–2	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.38	1.57	1.84	ns
t_{ENH}	REN, WEN Hold Time	0.02	0.02	0.02	ns
t_{BKS}	BLK Setup Time	0.19	0.22	0.26	ns
t_{BKH}	BLK Hold Time	0.00	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (pass-through)	2.36	2.68	3.15	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.89	1.02	1.20	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (pass-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on RD (pipelined)	0.92	1.05	1.23	ns
t_{REMRSTB}	RESET Removal	0.29	0.33	0.38	ns
t_{RECRSTB}	RESET Recovery	1.50	1.71	2.01	ns
t_{MPWRSTB}	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency	310	272	231	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

Special Function Pins

NC

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

No Connect

DC

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Do Not Connect

Packaging

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

Microsemi consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Microsemi IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Microsemi offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

Related Documents

User's Guides

ProASIC3E FPGA Fabric User's Guide

http://www.microsemi.com/document-portal/doc_download/130883-proasic3e-fpga-fabric-user-s-guide

Packaging

The following documents provide packaging information and device selection for low power flash devices.

Product Catalog

http://www.microsemi.com/soc/documents/ProdCat_PIB.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

Package Mechanical Drawings

http://www.microsemi.com/document-portal/doc_download/131095-package-mechanical-drawings

This document contains the package mechanical drawings for all packages currently or previously supplied by Microsemi. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials: <http://www.microsemi.com/products/fpga-soc/solutions>.

PQ208	
Pin Number	A3PE600 Function
108	TDO
109	TRST
110	VJTAG
111	VMV3
112	GDA0/IO67NPB3V1
113	GDB0/IO66NPB3V1
114	GDA1/IO67PPB3V1
115	GDB1/IO66PPB3V1
116	GDC0/IO65NDB3V1
117	GDC1/IO65PDB3V1
118	IO62NDB3V1
119	IO62PDB3V1
120	IO58NDB3V0
121	IO58PDB3V0
122	GND
123	VCCIB3
124	GCC2/IO55PSB3V0
125	GCB2/IO54PSB3V0
126	NC
127	IO53NDB3V0
128	GCA2/IO53PDB3V0
129	GCA1/IO52PPB3V0
130	GND
131	VCCPLC
132	GCA0/IO52NPB3V0
133	VCOMPLC
134	GCB0/IO51NDB2V1
135	GCB1/IO51PDB2V1
136	GCC1/IO50PSB2V1
137	IO49NDB2V1
138	IO49PDB2V1
139	IO48PSB2V1
140	VCCIB2
141	GND
142	VCC
143	IO47NDB2V1

PQ208	
Pin Number	A3PE600 Function
144	IO47PDB2V1
145	IO44NDB2V1
146	IO44PDB2V1
147	IO43NDB2V0
148	IO43PDB2V0
149	IO40NDB2V0
150	IO40PDB2V0
151	GBC2/IO38PSB2V0
152	GBA2/IO36PSB2V0
153	GBB2/IO37PSB2V0
154	VMV2
155	GNDQ
156	GND
157	VMV1
158	GNDQ
159	GBA1/IO35PDB1V1
160	GBA0/IO35NDB1V1
161	GBB1/IO34PDB1V1
162	GND
163	GBB0/IO34NDB1V1
164	GBC1/IO33PDB1V1
165	GBC0/IO33NDB1V1
166	IO31PDB1V1
167	IO31NDB1V1
168	IO27PDB1V0
169	IO27NDB1V0
170	VCCIB1
171	VCC
172	IO23PPB1V0
173	IO22PSB1V0
174	IO23NPB1V0
175	IO21PDB1V0
176	IO21NDB1V0
177	IO19PPB0V2
178	GND
179	IO18PPB0V2

PQ208	
Pin Number	A3PE600 Function
180	IO19NPB0V2
181	IO18NPB0V2
182	IO17PPB0V2
183	IO16PPB0V2
184	IO17NPB0V2
185	IO16NPB0V2
186	VCCIB0
187	VCC
188	IO15PDB0V2
189	IO15NDB0V2
190	IO13PDB0V2
191	IO13NDB0V2
192	IO11PSB0V1
193	IO09PDB0V1
194	IO09NDB0V1
195	GND
196	IO07PDB0V1
197	IO07NDB0V1
198	IO05PDB0V0
199	IO05NDB0V0
200	VCCIB0
201	GAC1/IO02PDB0V0
202	GAC0/IO02NDB0V0
203	GAB1/IO01PDB0V0
204	GAB0/IO01NDB0V0
205	GAA1/IO00PDB0V0
206	GAA0/IO00NDB0V0
207	GNDQ
208	VMV0

FG484	
Pin Number	A3PE1500 Function
V15	IO112NDB4V0
V16	GDB2/IO112PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO105NDB3V2
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO165NDB5V3
W6	GEB2/IO165PDB5V3
W7	IO164NDB5V3
W8	IO153NDB5V2
W9	IO153PDB5V2
W10	IO147NDB5V1
W11	IO133NDB4V2
W12	IO130NDB4V2
W13	IO130PDB4V2
W14	IO113NDB4V0
W15	GDC2/IO113PDB4V0
W16	IO111NDB4V0
W17	GDA2/IO111PDB4V0
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB6
Y2	NC
Y3	NC
Y4	IO161NDB5V3
Y5	GND
Y6	IO163NDB5V3

FG484	
Pin Number	A3PE1500 Function
Y7	IO163PDB5V3
Y8	VCC
Y9	VCC
Y10	IO147PDB5V1
Y11	IO133PDB4V2
Y12	IO131NPB4V2
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB3

FG676	
Pin Number	A3PE1500 Function
G13	IO21NDB0V2
G14	IO27PDB0V3
G15	IO35NDB1V0
G16	IO39PDB1V0
G17	IO51NDB1V2
G18	IO53NDB1V2
G19	VCCIB1
G20	GBA2/IO58PPB2V0
G21	GNDQ
G22	IO64NDB2V1
G23	IO64PDB2V1
G24	IO72PDB2V2
G25	IO72NDB2V2
G26	IO78PDB2V2
H1	IO208NDB7V2
H2	IO208PDB7V2
H3	IO209NDB7V2
H4	IO209PDB7V2
H5	IO219NDB7V3
H6	GAC2/IO219PDB7V3
H7	VCCIB7
H8	VCC
H9	VCCIB0
H10	VCCIB0
H11	VCCIB0
H12	VCCIB0
H13	VCCIB0
H14	VCCIB1
H15	VCCIB1
H16	VCCIB1
H17	VCCIB1
H18	VCCIB1
H19	VCC
H20	VCC
H21	IO58NPB2V0
H22	IO70PDB2V1

FG676	
Pin Number	A3PE1500 Function
H23	IO69PDB2V1
H24	IO76PDB2V2
H25	IO76NDB2V2
H26	IO78NDB2V2
J1	IO197NDB7V0
J2	IO197PDB7V0
J3	VMV7
J4	IO215NDB7V3
J5	IO215PDB7V3
J6	IO214PDB7V3
J7	IO214NDB7V3
J8	VCCIB7
J9	VCC
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	VCC
J15	VCC
J16	VCC
J17	VCC
J18	VCC
J19	VCCIB2
J20	IO62PDB2V0
J21	IO62NDB2V0
J22	IO70NDB2V1
J23	IO69NDB2V1
J24	VMV2
J25	IO80PDB2V3
J26	IO80NDB2V3
K1	IO195PDB7V0
K2	IO199NDB7V1
K3	IO199PDB7V1
K4	IO205NDB7V1
K5	IO205PDB7V1
K6	IO217PDB7V3

FG676	
Pin Number	A3PE1500 Function
K7	IO217NDB7V3
K8	VCCIB7
K9	VCC
K10	GND
K11	GND
K12	GND
K13	GND
K14	GND
K15	GND
K16	GND
K17	GND
K18	VCC
K19	VCCIB2
K20	IO65PDB2V1
K21	IO65NDB2V1
K22	IO74PDB2V2
K23	IO74NDB2V2
K24	IO75PDB2V2
K25	IO75NDB2V2
K26	IO84PDB2V3
L1	IO195NDB7V0
L2	IO198PPB7V0
L3	GNDQ
L4	IO201PDB7V1
L5	IO201NDB7V1
L6	IO210NDB7V2
L7	IO210PDB7V2
L8	VCCIB7
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	GND
L15	GND
L16	GND

FG896		FG896		FG896	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
A2	GND	AA9	GEB1/IO235PPB6V0	AB15	IO198PDB5V0
A3	GND	AA10	VCC	AB16	IO192NDB4V4
A4	IO14NPB0V1	AA11	IO226PPB5V4	AB17	IO192PDB4V4
A5	GND	AA12	VCCIB5	AB18	IO178NDB4V3
A6	IO07NPB0V0	AA13	VCCIB5	AB19	IO178PDB4V3
A7	GND	AA14	VCCIB5	AB20	IO174NDB4V2
A8	IO09NDB0V1	AA15	VCCIB5	AB21	IO162NPB4V1
A9	IO17NDB0V2	AA16	VCCIB4	AB22	VCC
A10	IO17PDB0V2	AA17	VCCIB4	AB23	VCCPLD
A11	IO21NDB0V2	AA18	VCCIB4	AB24	VCCIB3
A12	IO21PDB0V2	AA19	VCCIB4	AB25	IO150PDB3V4
A13	IO33NDB0V4	AA20	IO174PDB4V2	AB26	IO148PDB3V4
A14	IO33PDB0V4	AA21	VCC	AB27	IO147NDB3V4
A15	IO35NDB0V4	AA22	IO142NPB3V3	AB28	IO145PDB3V3
A16	IO35PDB0V4	AA23	IO144NDB3V3	AB29	IO143PDB3V3
A17	IO41NDB1V0	AA24	IO144PDB3V3	AB30	IO137PDB3V2
A18	IO43NDB1V0	AA25	IO146NDB3V4	AC1	IO254PDB6V2
A19	IO43PDB1V0	AA26	IO146PDB3V4	AC2	IO254NDB6V2
A20	IO45NDB1V0	AA27	IO147PDB3V4	AC3	IO240PDB6V0
A21	IO45PDB1V0	AA28	IO139NDB3V3	AC4	GEC1/IO236PDB6V0
A22	IO57NDB1V2	AA29	IO139PDB3V3	AC5	IO237PDB6V0
A23	IO57PDB1V2	AA30	IO133NDB3V2	AC6	IO237NDB6V0
A24	GND	AB1	IO256NDB6V2	AC7	VCOMPLE
A25	IO69PPB1V3	AB2	IO244PDB6V1	AC8	GND
A26	GND	AB3	IO244NDB6V1	AC9	IO226NPB5V4
A27	GBC1/IO79PPB1V4	AB4	IO241PDB6V0	AC10	IO222NDB5V3
A28	GND	AB5	IO241NDB6V0	AC11	IO216NPB5V2
A29	GND	AB6	IO243NPB6V1	AC12	IO210NPB5V2
AA1	IO256PDB6V2	AB7	VCCIB6	AC13	IO204NDB5V1
AA2	IO248PDB6V1	AB8	VCCPLE	AC14	IO204PDB5V1
AA3	IO248NDB6V1	AB9	VCC	AC15	IO194NDB5V0
AA4	IO246NDB6V1	AB10	IO222PDB5V3	AC16	IO188NDB4V4
AA5	GEA1/IO234PDB6V0	AB11	IO218PPB5V3	AC17	IO188PDB4V4
AA6	GEA0/IO234NDB6V0	AB12	IO206NDB5V1	AC18	IO182PPB4V3
AA7	IO243PPB6V1	AB13	IO206PDB5V1	AC19	IO170NPB4V2
AA8	IO245NDB6V1	AB14	IO198NDB5V0	AC20	IO164NDB4V1

FG896		FG896		FG896	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
M23	IO104PPB2V2	N29	IO107PDB2V3	R5	GFB0/IO274NPB7V0
M24	IO102PDB2V2	N30	IO107NDB2V3	R6	IO271NDB6V4
M25	IO102NDB2V2	P1	IO276NDB7V0	R7	GFB2/IO271PDB6V4
M26	IO95PDB2V1	P2	IO278NDB7V0	R8	IO269PDB6V4
M27	IO97NDB2V1	P3	IO280NDB7V0	R9	IO269NDB6V4
M28	IO101NDB2V2	P4	IO284NDB7V1	R10	VCCIB7
M29	IO103NDB2V2	P5	IO279NDB7V0	R11	VCC
M30	IO119PDB3V0	P6	GFC1/IO275PDB7V0	R12	GND
N1	IO276PDB7V0	P7	GFC0/IO275NDB7V0	R13	GND
N2	IO278PDB7V0	P8	IO277PDB7V0	R14	GND
N3	IO280PDB7V0	P9	IO277NDB7V0	R15	GND
N4	IO284PDB7V1	P10	VCCIB7	R16	GND
N5	IO279PDB7V0	P11	VCC	R17	GND
N6	IO285NDB7V1	P12	GND	R18	GND
N7	IO287NDB7V1	P13	GND	R19	GND
N8	IO281NDB7V0	P14	GND	R20	VCC
N9	IO281PDB7V0	P15	GND	R21	VCCIB2
N10	VCCIB7	P16	GND	R22	GCC0/IO112NDB2V3
N11	VCC	P17	GND	R23	GCB2/IO116PDB3V0
N12	GND	P18	GND	R24	IO118PDB3V0
N13	GND	P19	GND	R25	IO111PPB2V3
N14	GND	P20	VCC	R26	IO122PPB3V1
N15	GND	P21	VCCIB2	R27	GCA0/IO114NPB3V0
N16	GND	P22	GCC1/IO112PDB2V3	R28	VCOMPLC
N17	GND	P23	IO110PDB2V3	R29	GCB1/IO113PPB2V3
N18	GND	P24	IO110NDB2V3	R30	IO115NPB3V0
N19	GND	P25	IO109PPB2V3	T1	IO270NDB6V4
N20	VCC	P26	IO111NPB2V3	T2	VCCPLF
N21	VCCIB2	P27	IO105PDB2V2	T3	GFA2/IO272PPB6V4
N22	IO106NDB2V3	P28	IO105NDB2V2	T4	GFA1/IO273PDB6V4
N23	IO106PDB2V3	P29	GCC2/IO117PDB3V0	T5	IO272NPB6V4
N24	IO108PDB2V3	P30	IO117NDB3V0	T6	IO267NDB6V4
N25	IO108NDB2V3	R1	GFC2/IO270PDB6V4	T7	IO267PDB6V4
N26	IO95NDB2V1	R2	GFB1/IO274PPB7V0	T8	IO265PDB6V3
N27	IO99NDB2V2	R3	VCOMPLF	T9	IO263PDB6V3
N28	IO99PDB2V2	R4	GFA0/IO273NDB6V4	T10	VCCIB6

Revision	Changes	Page
Revision 11 (August 2012)	Added a Note stating "VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information." to Table 2-1 • Absolute Maximum Ratings and Table 2-2 • Recommended Operating Conditions ¹ (SAR 38322).	2-1 3-1 2-1
	The drive strength, IOL, and IOH value for 3.3 V GTL and 2.5 V GTL was changed from 25 mA to 20 mA in the following tables (SAR 31924): "Summary of Maximum and Minimum DC Input and Output Levels" table "Summary of I/O Timing Characteristics—Software Default Settings" table "I/O Output Buffer Maximum Resistances ¹ " table "Minimum and Maximum DC Input and Output Levels" table "Minimum and Maximum DC Input and Output Levels" table Also added note stating "Output drive strength is below JEDEC specification" for Tables 2-17 and 2-19. Additionally, the IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected from 51 to 35 (for 3.3 V GTL+) and from 40 to 33 (for 2.5 V GTL+) in table Table 2-13 (SAR 39714).	2-16 2-19 2-20 2-39 2-40
	"Duration of Short Circuit Event Before Failure" table was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 37934).	2-22
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34796): "It uses a 5 V–tolerant input buffer and push-pull output buffer." This change was made in revision 10 and omitted from the change table in error.	2-30
	Figure 2-11 was updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34889).	2-38
Revision 11 (continued)	In Table 2-81 VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 37222).	2-52
	Figure 2-47 and Figure 2-48 are new (SAR 34848).	2-79
	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions and Packaging" chapter: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38322). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1