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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	516096
Number of I/O	341
Number of Gates	300000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3pe3000-1fg484i

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



ProASIC3E Device Family Overview

VersaTiles

The ProASIC3E core consists of VersaTiles, which have been enhanced beyond the ProASIC^{PLUS®} core tiles. The ProASIC3E VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-2 for VersaTile configurations.



User Nonvolatile FlashROM

ProASIC3E devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- · Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- · Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3E IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC3E development software solutions, Libero[®] System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

ProASIC3E DC and Switching Characteristics

Calculating Power Dissipation

Quiescent Supply Current

Table 2-7 • Quiescent Supply Current Characteristics

	A3PE600	A3PE1500	A3PE3000
Typical (25°C)	5 mA	12 mA	25 mA
Maximum (Commercial)	30 mA	70 mA	150 mA
Maximum (Industrial)	45 mA	105 mA	225 mA

Notes:

1. IDD Includes VCC, VPUMP, VCCI, and VMV currents. Values do not include I/O static contribution, which is shown in Table 2-8 and Table 2-9 on page 2-7.

2. -F speed grade devices may experience higher standby IDD of up to five times the standard IDD and higher I/O leakage.

Power per I/O Pin

Table 2-8 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings

	VMV (V)	Static Power PDC2 (mW) ¹	Dynamic Power PAC9 (µW/MHz) ²
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	_	17.39
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	-	25.51
3.3 V LVTTL/LVCMOS Wide Range ³	3.3	-	16.34
3.3 V LVTTL/LVCMOS Wide Range – Schmitt trigger ³	3.3	-	24.49
2.5 V LVCMOS	2.5	-	5.76
2.5 V LVCMOS – Schmitt trigger	2.5	-	7.16
1.8 V LVCMOS	1.8	-	2.72
1.8 V LVCMOS – Schmitt trigger	1.8	-	2.80
1.5 V LVCMOS (JESD8-11)	1.5	-	2.08
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	-	2.00
3.3 V PCI	3.3	-	18.82
3.3 V PCI – Schmitt trigger	3.3	-	20.12
3.3 V PCI-X	3.3	-	18.82
3.3 V PCI-X – Schmitt trigger	3.3	-	20.12
Voltage-Referenced			
3.3 V GTL	3.3	2.90	8.23
2.5 V GTL	2.5	2.13	4.78
3.3 V GTL+	3.3	2.81	4.14
2.5 V GTL+	2.5	2.57	3.71

Notes:

1. PDC2 is the static power (where applicable) measured on VMV.

2. PAC9 is the total dynamic power measured on VCC and VMV.

3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- · The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-11 on page 2-11.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-12 on page 2-11.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-12 on page 2-11. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—PTOTAL

 $P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

P_{STAT} = PDC1 + N_{INPUTS} * PDC2 + N_{OUTPUTS} * PDC3

N_{INPUTS} is the number of I/O input buffers used in the design.

N_{OUTPUTS} is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption—P_{DYN}

P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}

Global Clock Contribution—P_{CLOCK}

P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S-CELL} * PAC4) * F_{CLK}

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3E FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3E FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

Sequential Cells Contribution—P_{S-CELL}

 P_{S-CELL} = N_{S-CELL} * (PAC5 + α_1 / 2 * PAC6) * F_{CLK}

 $N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

 α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-11 on page 2-11.

F_{CLK} is the global clock signal frequency.



Detailed I/O DC Characteristics

Table 2-18 • Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
C _{IN}	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
C _{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

Table 2-19 • I/O Output Buffer Maximum Resistances¹

Standard	Drive Strength	R _{PULL-DOWN} (Ω) ²	R _{PULL-UP} (Ω) ³
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	100	300
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	4 mA	100	200
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75
3.3 V GTL	20 mA ⁴	11	-
2.5 V GTL	20 mA ⁴	14	_

Notes:

- These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website at www.microsemi.com/index.php?option=com_content&id=1671&lang=en&view=article.
- 2. R_(PULL-DOWN-MAX) = (VOLspec) / IOLspec
- 3. R_(PULL-UP-MAX) = (VCCImax VOHspec) / IOHspec
- 4. Output drive strength is below JEDEC specification.

Table 2-22	 Duration o 	f Short Ci	cuit Event	Before	Failure	(continued)
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Temperature	Time before Failure
85°C	2 years
100°C	6 months

Table 2-23 • Schmitt Trigger Input Hysteresis

Hysteresis Voltage Value (typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

Table 2-24 • I/O Input Rise Time, Fall Time, and Related I/O Reliability*

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns *	20 years (110°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis.	20 years (110°C)
HSTL/SSTL/GTL	No requirement	10 ns *	10 years (100°C)
LVDS/B-LVDS/M-LVDS/ LVPECL	No requirement	10 ns *	10 years (100°C)

Note: *For clock signals and similar edge-generating signals, refer to the "ProASIC3/E SSO and Pin Placement Guidelines" chapter of the ProASIC3E FPGA Fabric User's Guide. The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

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ProASIC3E DC and Switching Characteristics

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-51 • Minimum and Maximum DC Input and Output Levels

2.5 GTL	VIL		VIH		VOL	VOH	IOL	ЮН	IOSL	IOSH	IIL	IIH
Drive Strength	Min., V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA²	μA²
20 mA ³	-0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	_	20	20	124	169	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

2. Currents are measured at 85°C junction temperature.

3. Output drive strength is below JEDEC specification.



Figure 2-13 • AC Loading

Table 2-52 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.05	VREF + 0.05	0.8	0.8	1.2	10

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-53 • 2.5 V GTL

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V VREF = 0.8 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.60	2.13	0.04	2.46	0.43	2.16	2.13			4.40	4.36	ns
-1	0.51	1.81	0.04	2.09	0.36	1.84	1.81			3.74	3.71	ns
-2	0.45	1.59	0.03	1.83	0.32	1.61	1.59			3.28	3.26	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-72 • Minimum and Maximum	DC Input and Output Levels
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SSTL3 Class I		VIL	VIH		VOL	VOH	IOL	ЮН	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA²	μA²
14 mA	-0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14	54	51	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

2. Currents are measured at 85°C junction temperature.



Figure 2-20 • AC Loading

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-74 • SSTL3 Class I

```
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.5 V
```

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.66	2.31	0.04	1.25	0.43	2.35	1.84			4.59	4.07	ns
-1	0.56	1.96	0.04	1.06	0.36	2.00	1.56			3.90	3.46	ns
-2	0.49	1.72	0.03	0.93	0.32	1.75	1.37			3.42	3.04	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

I/O Register Specifications



Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Figure 2-25 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3E library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion*, *IGLOO®/e*, *and ProASIC3/E Macro Library Guide*.



Figure 2-34 • Sample of Combinatorial Cells





Figure 2-39 • Peak-to-Peak Jitter Definition

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ProASIC3E DC and Switching Characteristics

Timing Characteristics

Table 2-99 • RAM4K9

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{AS}	Address setup time	0.25	0.28	0.33	ns
t _{AH}	Address hold time	0.00	0.00	0.00	ns
t _{ENS}	REN, WEN setup time	0.14	0.16	0.19	ns
t _{ENH}	REN, WEN hold time	0.10	0.11	0.13	ns
t _{BKS}	BLK setup time	0.23	0.27	0.31	ns
t _{BKH}	BLK hold time	0.02	0.02	0.02	ns
t _{DS}	Input data (DIN) setup time	0.18	0.21	0.25	ns
t _{DH}	Input data (DIN) hold time	0.00	0.00	0.00	ns
t _{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	1.79	2.03	2.39	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.36	2.68	3.15	ns
t _{CKQ2}	Clock High to new data valid on DOUT (pipelined)	0.89	1.02	1.20	ns
t _{C2CWWL} 1	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Closing Edge	0.33	0.28	0.25	ns
t _{C2CWWH} 1	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge	0.30	0.26	0.23	ns
t _{C2CRWH} 1	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.45	0.38	0.34	ns
t _{C2CWRH} 1	Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge	0.49	0.42	0.37	ns
t _{RSTBQ}	RESET Low to data out Low on DO (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on DO (pipelined)	0.92	1.05	1.23	ns
t _{REMRSTB}	RESET removal	0.29	0.33	0.38	ns
t _{RECRSTB}	RESET recovery	1.50	1.71	2.01	ns
t _{MPWRSTB}	RESET minimum pulse width	0.21	0.24	0.29	ns
t _{CYC}	Clock cycle time	3.23	3.68	4.32	ns
F _{MAX}	Maximum frequency	310	272	231	MHz

Notes:

1. For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.



Figure 2-50 • FIFO EMPTY Flag and AEMPTY Flag Assertion

Refer to the I/O Structure section of the *ProASIC3E FPGA Fabric User's Guide* for an explanation of the naming of global pins.

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pullup/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 W to 1 k Ω will satisfy the requirements. Refer to Table 3-1 for more information.

VJTAG	Tie-Off Resistance
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Table 3-1 • Recommended Tie-Off Values for the TCK and TRST Pins

Notes:

- 1. Equivalent parallel resistance if more than one device is on the JTAG chain
- 2. The TCK pin can be pulled up/down.
- 3. The TRST pin is pulled down.

TDI

TMS

Test Data Input

Test Data Output

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-1 and must satisfy the parallel resistance value requirement. The values in Table 3-1 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements.



4 – Package Pin Assignments

PQ208



Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/products/fpga-soc/solutions*.



	PQ208	PQ208		
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	
118	IO134NDB3V2	157	VMV1	
119	IO134PDB3V2	158	GNDQ	
120	IO132NDB3V2	159	GBA1/IO81PDB1V4	
121	IO132PDB3V2	160	GBA0/IO81NDB1V4	
122	GND	161	GBB1/IO80PDB1V4	
123	VCCIB3	162	GND	
124	GCC2/IO117PSB3V0	163	GBB0/IO80NDB1V4	
125	GCB2/IO116PSB3V0	164	GBC1/IO79PDB1V4	
126	NC	165	GBC0/IO79NDB1V4	
127	IO115NDB3V0	166	IO74PDB1V4	
128	GCA2/IO115PDB3V0	167	IO74NDB1V4	
129	GCA1/IO114PPB3V0	168	IO70PDB1V3	
130	GND	169	IO70NDB1V3	
131	VCCPLC	170	VCCIB1	
132	GCA0/IO114NPB3V0	171	VCC	
133	VCOMPLC	172	IO56PSB1V1	
134	GCB0/IO113NDB2V3	173	IO55PDB1V1	
135	GCB1/IO113PDB2V3	174	IO55NDB1V1	
136	GCC1/IO112PSB2V3	175	IO54PDB1V1	
137	IO110NDB2V3	176	IO54NDB1V1	
138	IO110PDB2V3	177	IO40PDB0V4	
139	IO106PSB2V3	178	GND	
140	VCCIB2	179	IO40NDB0V4	
141	GND	180	IO37PDB0V4	
142	VCC	181	IO37NDB0V4	
143	IO99NDB2V2	182	IO35PDB0V4	
144	IO99PDB2V2	183	IO35NDB0V4	
145	IO96NDB2V1	184	IO32PDB0V3	
146	IO96PDB2V1	185	IO32NDB0V3	
147	IO91NDB2V1	186	VCCIB0	
148	IO91PDB2V1	187	VCC	
149	IO88NDB2V0	188	IO28PDB0V3	
150	IO88PDB2V0	189	IO28NDB0V3	
151	GBC2/IO84PSB2V0	190	IO24PDB0V2	
152	GBA2/IO82PSB2V0	191	IO24NDB0V2	
153	GBB2/IO83PSB2V0	192	IO21PSB0V2	
154	VMV2	193	IO16PDB0V1	
155	GNDQ	194	IO16NDB0V1	
156	GND	195	GND	

PQ208					
Pin Number	A3PE3000 Function				
196	IO11PDB0V1				
197	IO11NDB0V1				
198	IO08PDB0V0				
199	IO08NDB0V0				
200	VCCIB0				
201	GAC1/IO02PDB0V0				
202	GAC0/IO02NDB0V0				
203	GAB1/IO01PDB0V0				
204	GAB0/IO01NDB0V0				
205	GAA1/IO00PDB0V0				
206	GAA0/IO00NDB0V0				
207	GNDQ				
208	VMV0				



	FG896		FG896	FG896	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
AG9	IO225NPB5V3	AH15	IO195NDB5V0	AJ21	IO173PDB4V2
AG10	IO223NPB5V3	AH16	IO185NDB4V3	AJ22	IO163NDB4V1
AG11	IO221PDB5V3	AH17	IO185PDB4V3	AJ23	IO163PDB4V1
AG12	IO221NDB5V3	AH18	IO181PDB4V3	AJ24	IO167NPB4V1
AG13	IO205NPB5V1	AH19	IO177NDB4V2	AJ25	VCC
AG14	IO199NDB5V0	AH20	IO171NPB4V2	AJ26	IO156NPB4V0
AG15	IO199PDB5V0	AH21	IO165PPB4V1	AJ27	VCC
AG16	IO187NDB4V4	AH22	IO161PPB4V0	AJ28	TMS
AG17	IO187PDB4V4	AH23	IO157NDB4V0	AJ29	GND
AG18	IO181NDB4V3	AH24	IO157PDB4V0	AJ30	GND
AG19	IO171PPB4V2	AH25	IO155NDB4V0	AK2	GND
AG20	IO165NPB4V1	AH26	VCCIB4	AK3	GND
AG21	IO161NPB4V0	AH27	TDI	AK4	IO217PPB5V2
AG22	IO159NDB4V0	AH28	VCC	AK5	GND
AG23	IO159PDB4V0	AH29	VPUMP	AK6	IO215PPB5V2
AG24	IO158PPB4V0	AH30	GND	AK7	GND
AG25	GDB2/IO155PDB4V0	AJ1	GND	AK8	IO207NDB5V1
AG26	GDA2/IO154PPB4V0	AJ2	GND	AK9	IO207PDB5V1
AG27	GND	AJ3	GEA2/IO233PPB5V4	AK10	IO201NDB5V0
AG28	VJTAG	AJ4	VCC	AK11	IO201PDB5V0
AG29	VCC	AJ5	IO217NPB5V2	AK12	IO193NDB4V4
AG30	IO149NDB3V4	AJ6	VCC	AK13	IO193PDB4V4
AH1	GND	AJ7	IO215NPB5V2	AK14	IO197PDB5V0
AH2	IO233NPB5V4	AJ8	IO213NDB5V2	AK15	IO191NDB4V4
AH3	VCC	AJ9	IO213PDB5V2	AK16	IO191PDB4V4
AH4	GEB2/IO232PPB5V4	AJ10	IO209NDB5V1	AK17	IO189NDB4V4
AH5	VCCIB5	AJ11	IO209PDB5V1	AK18	IO189PDB4V4
AH6	IO219NDB5V3	AJ12	IO203NDB5V1	AK19	IO179PPB4V3
AH7	IO219PDB5V3	AJ13	IO203PDB5V1	AK20	IO175NDB4V2
AH8	IO227NDB5V4	AJ14	IO197NDB5V0	AK21	IO175PDB4V2
AH9	IO227PDB5V4	AJ15	IO195PDB5V0	AK22	IO169NDB4V1
AH10	IO225PPB5V3	AJ16	IO183NDB4V3	AK23	IO169PDB4V1
AH11	IO223PPB5V3	AJ17	IO183PDB4V3	AK24	GND
AH12	IO211NDB5V2	AJ18	IO179NPB4V3	AK25	IO167PPB4V1
AH13	IO211PDB5V2	AJ19	IO177PDB4V2	AK26	GND
AH14	IO205PPB5V1	AJ20	IO173NDB4V2	AK27	GDC2/IO156PPB4V0



Datasheet Information

Revision	Changes	Page				
Revision 11 (August 2012)	Added a Note stating "VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information." to Table 2-1 • Absolute Maximum Ratings and Table 2-2 • Recommended Operating Conditions ¹ (SAR 38322).	2-1 3-1 2-1				
	The drive strength, IOL, and IOH value for 3.3 V GTL and 2.5 V GTL was changed from 25 mA to 20 mA in the following tables (SAR 31924):					
	"Summary of Maximum and Minimum DC Input and Output Levels" table	2-16				
	"Summary of I/O Timing Characteristics—Software Default Settings" table	2-19				
	"I/O Output Buffer Maximum Resistances ¹ " table	2-20				
	"Minimum and Maximum DC Input and Output Levels" table)	2-39				
	"Minimum and Maximum DC Input and Output Levels" table	2-40				
	Also added note stating "Output drive strength is below JEDEC specification" for Tables 2-17 and 2-19.					
	Additionally, the IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected from 51 to 35 (for 3.3 V GTL+) and from 40 to 33 (for 2.5 V GTL+) in table Table 2-13 (SAR 39714).					
	"Duration of Short Circuit Event Before Failure" table was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 37934).	2-22				
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34796):	2-30				
	"It uses a 5 V–tolerant input buffer and push-pull output buffer." This change was made in revision 10 and omitted from the change table in error.					
Revision 11 (continued)	Figure 2-11 was updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34889).	2-38				
	In Table 2-81 VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 37222).	2-52				
	Figure 2-47and Figure 2-48 are new (SAR 34848).	2-79				
	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions and Packaging" chapter: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38322). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1				



Datasheet Information

Revision	Changes	Page
Revision 10 (continued)	"TBD" for 3.3 V LVCMOS Wide Range in Table 2-19 • I/O Output Buffer Maximum Resistances ¹ and Table 2-21 • I/O Short Currents IOSH/IOSL was replaced by "Same as regular 3.3 V LVCMOS" (SAR 33853).	2-20, 2-27
	3.3 V LVCMOS Wide Range information was separated from regular 3.3 V LVCMOS and placed into its own new section, "3.3 V LVCMOS Wide Range". Values of IOSH and IOSL were added in Table 2-29 • Minimum and Maximum DC Input and Output Levels (SAR 33853).	
	The formulas in the table notes for Table 2-20 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 34755).	2-21
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34889).	2-24
	The titles and subtitles for Table 2-31 • 3.3 V LVCMOS Wide Range High Slew and Table 2-32 • 3.3 V LVCMOS Wide Range Low Slew were corrected (SAR 37227).	2-28, 2-29
	The following notes were removed from Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels (SAR 34812): ±5%	2-50
	Differential input voltage = ±350 mV	
	Minimum pulse width High and Low values were added to the tables in the "Global Tree Timing Characteristics" section. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 36957).	2-68
	A note was added to Table 2-98 • ProASIC3E CCC/PLL Specification indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34824).	2-70
	The following figures were deleted. Reference was made to a new application note, <i>Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs</i> , which covers these cases in detail (SAR 34872).	2-74, 2-75, 2-79,
	Figure 2-44 • Write Access after Write onto Same Address	2-82
	Figure 2-45 • Read Access after Write onto Same Address	
	Figure 2-46 • Write Access after Read onto Same Address	
	Characteristics" tables, Figure 2-49 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35750).	
	The "Pin Descriptions and Packaging" chapter is new (SAR 34771).	3-1
	Package names used in the "Package Pin Assignments" section were revised to match standards given in <i>Package Mechanical Drawings</i> (SAR 34771).	4-1
	Pin E6 for the FG256 package was corrected from VvB0 to VCCIB0 (SARs 30364, 31597, 26243).	4-9
July 2010	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "ProASIC3E Device Status" table on page II indicates the status for each device in the device family.	N/A



Revision	Changes	Page
Advance v0.3 (continued)	The "Methodology" section was updated.	3-9
	The A3PE3000 "208-Pin PQFP" pin table was updated.	4-6



Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "ProASIC3E Device Status" table on page II, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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