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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 516096 |
| Number of I/O | 620 |
| Number of Gates | 3000000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 896-BGA |
| Supplier Device Package | 896-FBGA (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m1a3pe3000-1fgg896i |

### VersaTiles

The ProASIC3E core consists of VersaTiles, which have been enhanced beyond the ProASIC[PLUS]® core tiles. The ProASIC3E VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-2 for VersaTile configurations.

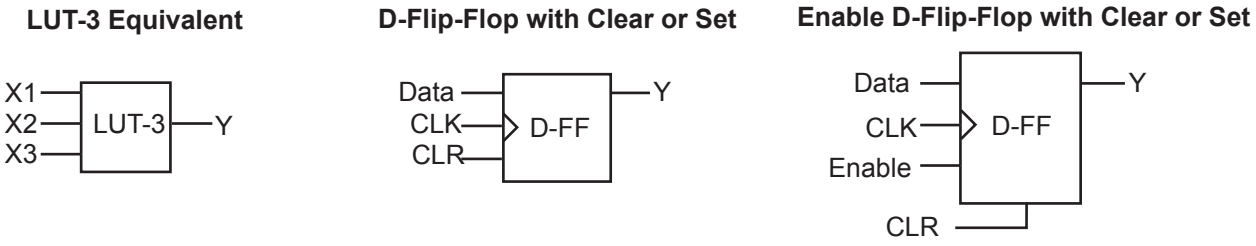


***Figure 1-2 •*** **VersaTile Configurations**

### User Nonvolatile FlashROM

ProASIC3E devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3E IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC3E development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

**Table 2-9 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings (continued) (continued)[1]**

| | $C_{LOAD}$ (pF) | VCCI (V) | Static Power PDC3 (mW)[2] | Dynamic Power PAC10 (µW/MHz)[3] |
|---|---|---|---|---|
| SSTL3 (I) | 30 | 3.3 | 26.02 | 114.87 |
| SSTL3 (II) | 30 | 3.3 | 42.21 | 131.76 |
| **Differential** | | | | |
| LVDS/B-LVDS/M-LVDS | – | 2.5 | 7.70 | 89.62 |
| LVPECL | – | 3.3 | 19.42 | 168.02 |

*Notes:*

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PDC3 is the static power (where applicable) measured on VCCI.*
3. *PAC10 is the total dynamic power measured on VCC and VCCI.*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

## Power Consumption of Various Internal Resources

**Table 2-10 • Different Components Contributing to the Dynamic Power Consumption in ProASIC3E Devices**

| Parameter | Definition | Device-Specific Dynamic Contributions (µW/MHz) | | |
|---|---|---|---|---|
| | | A3PE600 | A3PE1500 | A3PE3000 |
| PAC1 | Clock contribution of a Global Rib | 12.77 | 16.21 | 19.7 |
| PAC2 | Clock contribution of a Global Spine | 1.85 | 3.06 | 4.16 |
| PAC3 | Clock contribution of a VersaTile row | 0.88 | | |
| PAC4 | Clock contribution of a VersaTile used as a sequential module | 0.12 | | |
| PAC5 | First contribution of a VersaTile used as a sequential module | 0.07 | | |
| PAC6 | Second contribution of a VersaTile used as a sequential module | 0.29 | | |
| PAC7 | Contribution of a VersaTile used as a combinatorial module | 0.29 | | |
| PAC8 | Average contribution of a routing net | 0.70 | | |
| PAC9 | Contribution of an I/O input pin (standard-dependent) | See Table 2-8 on page 2-6. | | |
| PAC10 | Contribution of an I/O output pin (standard-dependent) | See Table 2-9 on page 2-7 | | |
| PAC11 | Average contribution of a RAM block during a read operation | 25.00 | | |
| PAC12 | Average contribution of a RAM block during a write operation | 30.00 | | |
| PAC13 | Static PLL contribution | 2.55 mW | | |
| PAC14 | Dynamic contribution for PLL | 2.60 | | |

*Note: For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power calculator or SmartPower in Libero SoC.*

### 3.3 V LVCMOS Wide Range

**Table 2-29 • Minimum and Maximum DC Input and Output Levels**

| 3.3 V LVCMOS Wide Range | Equivalent Software Default Drive Strength Option[1] | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[2] | IIH[3] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | µA | µA | Max. mA[4] | Max. mA[4] | µA[5] | µA[5] |
| 100 µA | 2 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 27 | 25 | 10 | 10 |
| 100 µA | 4 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 27 | 25 | 10 | 10 |
| 100 µA | 6 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 54 | 51 | 10 | 10 |
| 100 µA | 8 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 54 | 51 | 10 | 10 |
| 100 µA | 12 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 109 | 103 | 10 | 10 |
| 100 µA | 16 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 127 | 132 | 10 | 10 |
| 100 µA | 24 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 181 | 268 | 10 | 10 |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN< VCCI. Input current is larger when operating outside recommended ranges.*
4. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

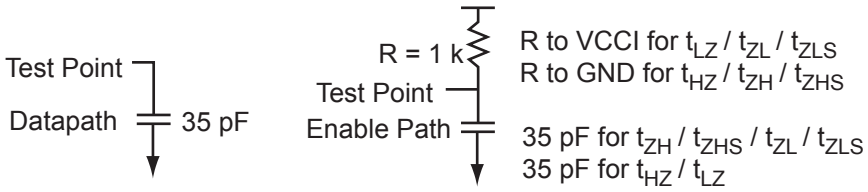


**Figure 2-7 • AC Loading**

**Table 2-30 • 3.3 V LVCMOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|
| 0 | 3.3 | 1.4 | – | 35 |

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

# Differential I/O Characteristics

## Physical Implementation

Configuration of the I/O modules as a differential pair is handled by the Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and DDR. However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

## LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-22. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3E also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

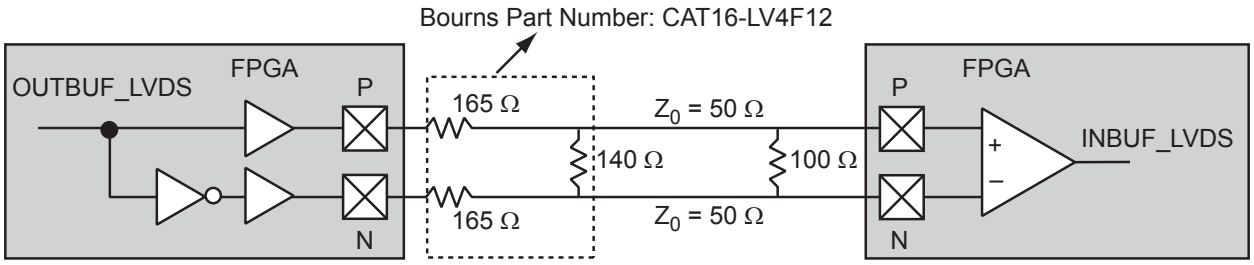


***Figure 2-22 •*** **LVDS Circuit Diagram and Board-Level Implementation**

## Output Register

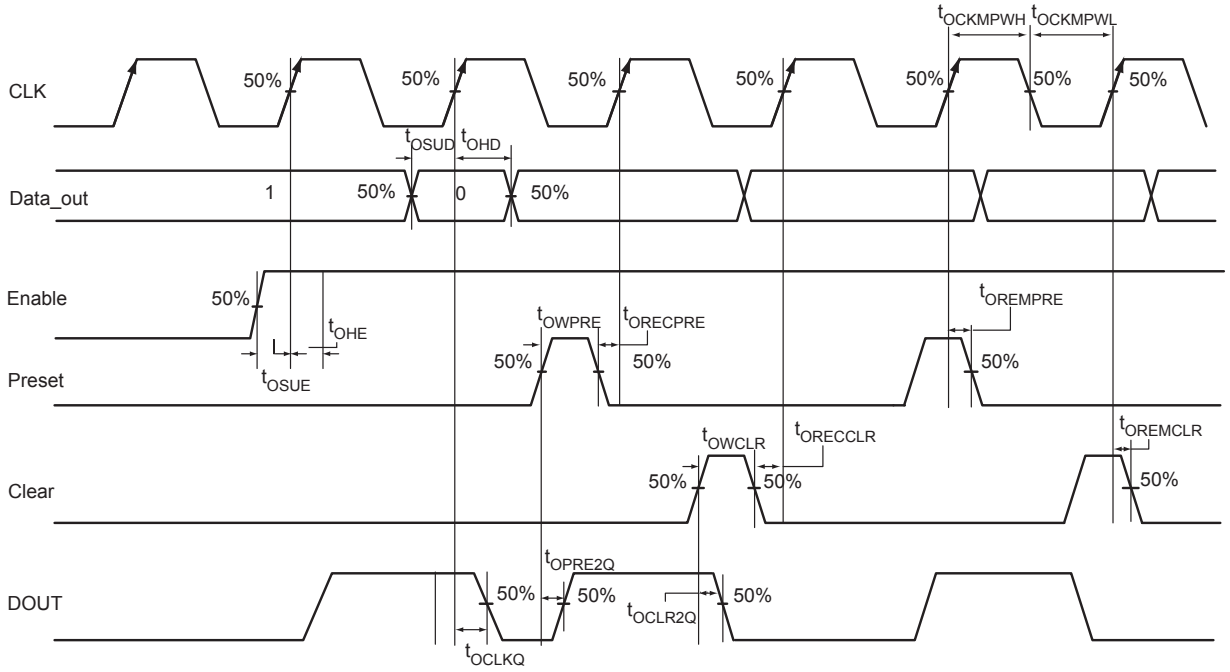


***Figure 2-28 •*** **Output Register Timing Diagram**

### Timing Characteristics

***Table 2-87 •*** **Output Data Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | 0.59 | 0.67 | 0.79 | ns |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | 0.31 | 0.36 | 0.42 | ns |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{OSUE}$ | Enable Setup Time for the Output Data Register | 0.44 | 0.50 | 0.59 | ns |
| $t_{OHE}$ | Enable Hold Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{OCLR2Q}$ | Asynchronous Clear-to-Q of the Output Data Register | 0.80 | 0.91 | 1.07 | ns |
| $t_{OPRE2Q}$ | Asynchronous Preset-to-Q of the Output Data Register | 0.80 | 0.91 | 1.07 | ns |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OCKMPWH}$ | Clock Minimum Pulse Width High for the Output Data Register | 0.36 | 0.41 | 0.48 | ns |
| $t_{OCKMPWL}$ | Clock Minimum Pulse Width Low for the Output Data Register | 0.32 | 0.37 | 0.43 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

## Timing Characteristics

**Table 2-101 • FIFO**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{ENS}$ | REN, WEN Setup Time | 1.38 | 1.57 | 1.84 | ns |
| $t_{ENH}$ | REN, WEN Hold Time | 0.02 | 0.02 | 0.02 | ns |
| $t_{BKS}$ | BLK Setup Time | 0.19 | 0.22 | 0.26 | ns |
| $t_{BKH}$ | BLK Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{DS}$ | Input Data (WD) Setup Time | 0.18 | 0.21 | 0.25 | ns |
| $t_{DH}$ | Input Data (WD) Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to New Data Valid on RD (pass-through) | 2.36 | 2.68 | 3.15 | ns |
| $t_{CKQ2}$ | Clock High to New Data Valid on RD (pipelined) | 0.89 | 1.02 | 1.20 | ns |
| $t_{RCKEF}$ | RCLK High to Empty Flag Valid | 1.72 | 1.96 | 2.30 | ns |
| $t_{WCKFF}$ | WCLK High to Full Flag Valid | 1.63 | 1.86 | 2.18 | ns |
| $t_{CKAF}$ | Clock High to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | ns |
| $t_{RSTFG}$ | RESET Low to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | ns |
| $t_{RSTAF}$ | RESET Low to Almost Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | ns |
| $t_{RSTBQ}$ | RESET Low to Data Out Low on RD (pass-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data Out Low on RD (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET Removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 0.21 | 0.24 | 0.29 | ns |
| $t_{CYC}$ | Clock Cycle Time | 3.23 | 3.68 | 4.32 | ns |
| $F_{MAX}$ | Maximum Frequency | 310 | 272 | 231 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

# 3 – Pin Descriptions and Packaging

## Supply Pins

**GND** **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

**GNDQ** **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

**VCC** **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

**VCCIBx** **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. In general, unused I/O banks should have their corresponding VCCIX pins tied to GND. If an output pad is terminated to ground through any resistor and if the corresponding VCCIX is left floating, then the leakage current to ground is ~ 0uA. However, if an output pad is terminated to ground through any resistor and the corresponding VCCIX grounded, then the leakage current to ground is ~ 3 uA. For unused banks the aforementioned behavior is to be taken into account while deciding if it’s better to float VCCIX of unused bank or tie it to GND.

**VMVx** **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

**VCCPLA/B/C/D/E/F** **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V.

When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *ProASIC3E FPGA Fabric User’s Guide* for a complete board solution for the PLL analog power supply and ground.

There are six VCCPLX pins on ProASIC3E devices.

**VCOMPLA/B/C/D/E/F** **PLL Ground**

Ground to analog PLL power supplies. When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There are six VCOMPL pins (PLL ground) on ProASIC3E devices.

**VJTAG** **JTAG Supply Voltage**

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

**VPUMP** **Programming Supply Voltage**

For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

# User-Defined Supply Pins

**VREF** **I/O Voltage Reference**

Reference voltage for I/O minibanks. VREF pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, can be designated the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One VREF pin can support the number of I/Os available in its minibank.

# User Pins

**I/O** **User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

**GL** **Globals**

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *ProASIC3E FPGA Fabric User's Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the I/O Structure section of the *ProASIC3E FPGA Fabric User's Guide* for an explanation of the naming of global pins.

# JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

### TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 W to 1 kΩ will satisfy the requirements. Refer to Table 3-1 for more information.

***Table 3-1* • Recommended Tie-Off Values for the TCK and TRST Pins**

| VJTAG | Tie-Off Resistance |
|---|---|
| VJTAG at 3.3 V | 200 Ω to 1 kΩ |
| VJTAG at 2.5 V | 200 Ω to 1 kΩ |
| VJTAG at 1.8 V | 500 Ω to 1 kΩ |
| VJTAG at 1.5 V | 500 Ω to 1 kΩ |

*Notes:*

1. *Equivalent parallel resistance if more than one device is on the JTAG chain*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin is pulled down.*

### TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

### TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

### TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

### TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-1 and must satisfy the parallel resistance value requirement. The values in Table 3-1 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

| FG484 | |
|---|---|
| Pin Number | A3PE1500 Function |
| A1 | GND |
| A2 | GND |
| A3 | VCCIB0 |
| A4 | IO05NDB0V0 |
| A5 | IO05PDB0V0 |
| A6 | IO11NDB0V1 |
| A7 | IO11PDB0V1 |
| A8 | IO15PDB0V1 |
| A9 | IO17PDB0V2 |
| A10 | IO27NDB0V3 |
| A11 | IO27PDB0V3 |
| A12 | IO32PDB1V0 |
| A13 | IO43PDB1V1 |
| A14 | IO47NDB1V1 |
| A15 | IO47PDB1V1 |
| A16 | IO51NDB1V2 |
| A17 | IO51PDB1V2 |
| A18 | IO54NDB1V3 |
| A19 | NC |
| A20 | VCCIB1 |
| A21 | GND |
| A22 | GND |
| AA1 | GND |
| AA2 | VCCIB6 |
| AA3 | NC |
| AA4 | IO161PDB5V3 |
| AA5 | IO155NDB5V2 |
| AA6 | IO155PDB5V2 |
| AA7 | IO154NDB5V2 |
| AA8 | IO154PDB5V2 |
| AA9 | IO143PDB5V1 |
| AA10 | IO143NDB5V1 |
| AA11 | IO131PPB4V2 |
| AA12 | IO129NDB4V2 |
| AA13 | IO129PDB4V2 |
| AA14 | NC |

| FG484 | |
|---|---|
| Pin Number | A3PE1500 Function |
| AA15 | NC |
| AA16 | IO117NDB4V0 |
| AA17 | IO117PDB4V0 |
| AA18 | IO115NDB4V0 |
| AA19 | IO115PDB4V0 |
| AA20 | NC |
| AA21 | VCCIB3 |
| AA22 | GND |
| AB1 | GND |
| AB2 | GND |
| AB3 | VCCIB5 |
| AB4 | IO159NDB5V3 |
| AB5 | IO159PDB5V3 |
| AB6 | IO149NDB5V1 |
| AB7 | IO149PDB5V1 |
| AB8 | IO138NDB5V0 |
| AB9 | IO138PDB5V0 |
| AB10 | NC |
| AB11 | NC |
| AB12 | IO127NDB4V2 |
| AB13 | IO127PDB4V2 |
| AB14 | IO125NDB4V1 |
| AB15 | IO125PDB4V1 |
| AB16 | IO122NDB4V1 |
| AB17 | IO122PDB4V1 |
| AB18 | NC |
| AB19 | NC |
| AB20 | VCCIB4 |
| AB21 | GND |
| AB22 | GND |
| B1 | GND |
| B2 | VCCIB7 |
| B3 | NC |
| B4 | IO03NDB0V0 |
| B5 | IO03PDB0V0 |
| B6 | IO10NDB0V1 |

| FG484 | |
|---|---|
| Pin Number | A3PE1500 Function |
| B7 | IO10PDB0V1 |
| B8 | IO15NDB0V1 |
| B9 | IO17NDB0V2 |
| B10 | IO20PDB0V2 |
| B11 | IO29PDB0V3 |
| B12 | IO32NDB1V0 |
| B13 | IO43NDB1V1 |
| B14 | NC |
| B15 | NC |
| B16 | IO53NDB1V2 |
| B17 | IO53PDB1V2 |
| B18 | IO54PDB1V3 |
| B19 | NC |
| B20 | NC |
| B21 | VCCIB2 |
| B22 | GND |
| C1 | VCCIB7 |
| C2 | NC |
| C3 | NC |
| C4 | NC |
| C5 | GND |
| C6 | IO07NDB0V0 |
| C7 | IO07PDB0V0 |
| C8 | VCC |
| C9 | VCC |
| C10 | IO20NDB0V2 |
| C11 | IO29NDB0V3 |
| C12 | NC |
| C13 | NC |
| C14 | VCC |
| C15 | VCC |
| C16 | NC |
| C17 | NC |
| C18 | GND |
| C19 | NC |
| C20 | NC |

| FG484 | |
|---|---|
| Pin Number | A3PE1500 Function |
| C21 | NC |
| C22 | VCCIB2 |
| D1 | NC |
| D2 | NC |
| D3 | NC |
| D4 | GND |
| D5 | GAA0/IO00NDB0V0 |
| D6 | GAA1/IO00PDB0V0 |
| D7 | GAB0/IO01NDB0V0 |
| D8 | IO09PDB0V1 |
| D9 | IO13PDB0V1 |
| D10 | IO21PDB0V2 |
| D11 | IO31NDB0V3 |
| D12 | IO37NDB1V0 |
| D13 | IO37PDB1V0 |
| D14 | IO49NDB1V2 |
| D15 | IO49PDB1V2 |
| D16 | GBB1/IO56PDB1V3 |
| D17 | GBA0/IO57NDB1V3 |
| D18 | GBA1/IO57PDB1V3 |
| D19 | GND |
| D20 | NC |
| D21 | IO69PDB2V1 |
| D22 | NC |
| E1 | NC |
| E2 | IO218PPB7V3 |
| E3 | GND |
| E4 | GAB2/IO220PDB7V3 |
| E5 | GAA2/IO221PDB7V3 |
| E6 | GNDQ |
| E7 | GAB1/IO01PDB0V0 |
| E8 | IO09NDB0V1 |
| E9 | IO13NDB0V1 |
| E10 | IO21NDB0V2 |
| E11 | IO31PDB0V3 |
| E12 | IO35NDB1V0 |

| FG484 | |
|---|---|
| Pin Number | A3PE1500 Function |
| E13 | IO41NDB1V1 |
| E14 | IO41PDB1V1 |
| E15 | GBC1/IO55PDB1V3 |
| E16 | GBB0/IO56NDB1V3 |
| E17 | GNDQ |
| E18 | GBA2/IO58PDB2V0 |
| E19 | IO63NDB2V0 |
| E20 | GND |
| E21 | IO69NDB2V1 |
| E22 | NC |
| F1 | IO218NPB7V3 |
| F2 | IO216NDB7V3 |
| F3 | IO216PDB7V3 |
| F4 | IO220NDB7V3 |
| F5 | IO221NDB7V3 |
| F6 | VMV7 |
| F7 | VCCPLA |
| F8 | GAC0/IO02NDB0V0 |
| F9 | GAC1/IO02PDB0V0 |
| F10 | IO23NDB0V2 |
| F11 | IO23PDB0V2 |
| F12 | IO35PDB1V0 |
| F13 | IO39NDB1V0 |
| F14 | IO45PDB1V1 |
| F15 | GBC0/IO55NDB1V3 |
| F16 | VCCPLB |
| F17 | VMV2 |
| F18 | IO58NDB2V0 |
| F19 | IO63PDB2V0 |
| F20 | NC |
| F21 | NC |
| F22 | NC |
| G1 | IO211NDB7V2 |
| G2 | IO211PDB7V2 |
| G3 | NC |
| G4 | IO214PDB7V3 |

| FG484 | |
|---|---|
| Pin Number | A3PE1500 Function |
| G5 | IO217PDB7V3 |
| G6 | GAC2/IO219PDB7V3 |
| G7 | VCOMPLA |
| G8 | GNDQ |
| G9 | IO19NDB0V2 |
| G10 | IO19PDB0V2 |
| G11 | IO25PDB0V3 |
| G12 | IO33PDB1V0 |
| G13 | IO39PDB1V0 |
| G14 | IO45NDB1V1 |
| G15 | GNDQ |
| G16 | VCOMPLB |
| G17 | GBB2/IO59PDB2V0 |
| G18 | IO62PDB2V0 |
| G19 | IO62NDB2V0 |
| G20 | IO71PDB2V2 |
| G21 | IO71NDB2V2 |
| G22 | NC |
| H1 | IO209PSB7V2 |
| H2 | NC |
| H3 | VCC |
| H4 | IO214NDB7V3 |
| H5 | IO217NDB7V3 |
| H6 | IO219NDB7V3 |
| H7 | IO215PDB7V3 |
| H8 | VMV0 |
| H9 | VCCIB0 |
| H10 | VCCIB0 |
| H11 | IO25NDB0V3 |
| H12 | IO33NDB1V0 |
| H13 | VCCIB1 |
| H14 | VCCIB1 |
| H15 | VMV1 |
| H16 | GBC2/IO60PDB2V0 |
| H17 | IO59NDB2V0 |
| H18 | IO67NDB2V1 |

| FG484 | |
|---|---|
| **Pin Number** | **A3PE3000 Function** |
| C21 | IO94PPB2V1 |
| C22 | VCCIB2 |
| D1 | IO293PDB7V2 |
| D2 | IO303NDB7V3 |
| D3 | IO305NDB7V3 |
| D4 | GND |
| D5 | GAA0/IO00NDB0V0 |
| D6 | GAA1/IO00PDB0V0 |
| D7 | GAB0/IO01NDB0V0 |
| D8 | IO20PDB0V2 |
| D9 | IO22PDB0V2 |
| D10 | IO30PDB0V3 |
| D11 | IO38NDB0V4 |
| D12 | IO52NDB1V1 |
| D13 | IO52PDB1V1 |
| D14 | IO66NDB1V3 |
| D15 | IO66PDB1V3 |
| D16 | GBB1/IO80PDB1V4 |
| D17 | GBA0/IO81NDB1V4 |
| D18 | GBA1/IO81PDB1V4 |
| D19 | GND |
| D20 | IO88PDB2V0 |
| D21 | IO90PDB2V1 |
| D22 | IO94NPB2V1 |
| E1 | IO293NDB7V2 |
| E2 | IO299PPB7V3 |
| E3 | GND |
| E4 | GAB2/IO308PDB7V4 |
| E5 | GAA2/IO309PDB7V4 |
| E6 | GNDQ |
| E7 | GAB1/IO01PDB0V0 |
| E8 | IO20NDB0V2 |
| E9 | IO22NDB0V2 |
| E10 | IO30NDB0V3 |
| E11 | IO38PDB0V4 |
| E12 | IO44NDB1V0 |

| FG484 | |
|---|---|
| **Pin Number** | **A3PE3000 Function** |
| E13 | IO58NDB1V2 |
| E14 | IO58PDB1V2 |
| E15 | GBC1/IO79PDB1V4 |
| E16 | GBB0/IO80NDB1V4 |
| E17 | GNDQ |
| E18 | GBA2/IO82PDB2V0 |
| E19 | IO86NDB2V0 |
| E20 | GND |
| E21 | IO90NDB2V1 |
| E22 | IO98PDB2V2 |
| F1 | IO299NPB7V3 |
| F2 | IO301NDB7V3 |
| F3 | IO301PDB7V3 |
| F4 | IO308NDB7V4 |
| F5 | IO309NDB7V4 |
| F6 | VMV7 |
| F7 | VCCPLA |
| F8 | GAC0/IO02NDB0V0 |
| F9 | GAC1/IO02PDB0V0 |
| F10 | IO32NDB0V3 |
| F11 | IO32PDB0V3 |
| F12 | IO44PDB1V0 |
| F13 | IO50NDB1V1 |
| F14 | IO60PDB1V2 |
| F15 | GBC0/IO79NDB1V4 |
| F16 | VCCPLB |
| F17 | VMV2 |
| F18 | IO82NDB2V0 |
| F19 | IO86PDB2V0 |
| F20 | IO96PDB2V1 |
| F21 | IO96NDB2V1 |
| F22 | IO98NDB2V2 |
| G1 | IO289NDB7V1 |
| G2 | IO289PDB7V1 |
| G3 | IO291PPB7V2 |
| G4 | IO295PDB7V2 |

| FG484 | |
|---|---|
| **Pin Number** | **A3PE3000 Function** |
| G5 | IO297PDB7V2 |
| G6 | GAC2/IO307PDB7V4 |
| G7 | VCOMPLA |
| G8 | GNDQ |
| G9 | IO26NDB0V3 |
| G10 | IO26PDB0V3 |
| G11 | IO36PDB0V4 |
| G12 | IO42PDB1V0 |
| G13 | IO50PDB1V1 |
| G14 | IO60NDB1V2 |
| G15 | GNDQ |
| G16 | VCOMPLB |
| G17 | GBB2/IO83PDB2V0 |
| G18 | IO92PDB2V1 |
| G19 | IO92NDB2V1 |
| G20 | IO102PDB2V2 |
| G21 | IO102NDB2V2 |
| G22 | IO105NDB2V2 |
| H1 | IO286PSB7V1 |
| H2 | IO291NPB7V2 |
| H3 | VCC |
| H4 | IO295NDB7V2 |
| H5 | IO297NDB7V2 |
| H6 | IO307NDB7V4 |
| H7 | IO287PDB7V1 |
| H8 | VMV0 |
| H9 | VCCIB0 |
| H10 | VCCIB0 |
| H11 | IO36NDB0V4 |
| H12 | IO42NDB1V0 |
| H13 | VCCIB1 |
| H14 | VCCIB1 |
| H15 | VMV1 |
| H16 | GBC2/IO84PDB2V0 |
| H17 | IO83NDB2V0 |
| H18 | IO100NDB2V2 |

| FG484 | |
|---|---|
| Pin Number | A3PE3000 Function |
| N17 | IO132NPB3V2 |
| N18 | IO117NPB3V0 |
| N19 | IO132PPB3V2 |
| N20 | GNDQ |
| N21 | IO126NDB3V1 |
| N22 | IO128PDB3V1 |
| P1 | IO247PDB6V1 |
| P2 | IO253PDB6V2 |
| P3 | IO270NPB6V4 |
| P4 | IO261NPB6V3 |
| P5 | IO249PPB6V1 |
| P6 | IO259PDB6V3 |
| P7 | IO259NDB6V3 |
| P8 | VCCIB6 |
| P9 | GND |
| P10 | VCC |
| P11 | VCC |
| P12 | VCC |
| P13 | VCC |
| P14 | GND |
| P15 | VCCIB3 |
| P16 | GDB0/IO152NPB3V4 |
| P17 | IO136NDB3V2 |
| P18 | IO136PDB3V2 |
| P19 | IO138PDB3V3 |
| P20 | VMV3 |
| P21 | IO130PDB3V2 |
| P22 | IO128NDB3V1 |
| R1 | IO247NDB6V1 |
| R2 | IO245PDB6V1 |
| R3 | VCC |
| R4 | IO249NPB6V1 |
| R5 | IO251NDB6V2 |
| R6 | IO251PDB6V2 |
| R7 | GEC0/IO236NPB6V0 |
| R8 | VMV5 |

| FG484 | |
|---|---|
| Pin Number | A3PE3000 Function |
| R9 | VCCIB5 |
| R10 | VCCIB5 |
| R11 | IO196NDB5V0 |
| R12 | IO196PDB5V0 |
| R13 | VCCIB4 |
| R14 | VCCIB4 |
| R15 | VMV3 |
| R16 | VCCPLD |
| R17 | GDB1/IO152PPB3V4 |
| R18 | GDC1/IO151PDB3V4 |
| R19 | IO138NDB3V3 |
| R20 | VCC |
| R21 | IO130NDB3V2 |
| R22 | IO134PDB3V2 |
| T1 | IO243PPB6V1 |
| T2 | IO245NDB6V1 |
| T3 | IO243NPB6V1 |
| T4 | IO241PDB6V0 |
| T5 | IO241NDB6V0 |
| T6 | GEC1/IO236PPB6V0 |
| T7 | VCOMPLE |
| T8 | GNDQ |
| T9 | GEA2/IO233PPB5V4 |
| T10 | IO206NDB5V1 |
| T11 | IO202NDB5V1 |
| T12 | IO194NDB5V0 |
| T13 | IO186NDB4V4 |
| T14 | IO186PDB4V4 |
| T15 | GNDQ |
| T16 | VCOMPLD |
| T17 | VJTAG |
| T18 | GDC0/IO151NDB3V4 |
| T19 | GDA1/IO153PDB3V4 |
| T20 | IO144PDB3V3 |
| T21 | IO140PDB3V3 |
| T22 | IO134NDB3V2 |

| FG484 | |
|---|---|
| Pin Number | A3PE3000 Function |
| U1 | IO240PPB6V0 |
| U2 | IO238PDB6V0 |
| U3 | IO238NDB6V0 |
| U4 | GEB1/IO235PDB6V0 |
| U5 | GEB0/IO235NDB6V0 |
| U6 | VMV6 |
| U7 | VCCPLE |
| U8 | IO233NPB5V4 |
| U9 | IO222PPB5V3 |
| U10 | IO206PDB5V1 |
| U11 | IO202PDB5V1 |
| U12 | IO194PDB5V0 |
| U13 | IO176NDB4V2 |
| U14 | IO176PDB4V2 |
| U15 | VMV4 |
| U16 | TCK |
| U17 | VPUMP |
| U18 | TRST |
| U19 | GDA0/IO153NDB3V4 |
| U20 | IO144NDB3V3 |
| U21 | IO140NDB3V3 |
| U22 | IO142PDB3V3 |
| V1 | IO239PDB6V0 |
| V2 | IO240NPB6V0 |
| V3 | GND |
| V4 | GEA1/IO234PDB6V0 |
| V5 | GEA0/IO234NDB6V0 |
| V6 | GNDQ |
| V7 | GEC2/IO231PDB5V4 |
| V8 | IO222NPB5V3 |
| V9 | IO204NDB5V1 |
| V10 | IO204PDB5V1 |
| V11 | IO195NDB5V0 |
| V12 | IO195PDB5V0 |
| V13 | IO178NDB4V3 |
| V14 | IO178PDB4V3 |

| FG676 | |
|---|---|
| **Pin Number** | **A3PE1500 Function** |
| W25 | IO96PDB3V1 |
| W26 | IO94NDB3V0 |
| Y1 | IO175NDB6V1 |
| Y2 | IO175PDB6V1 |
| Y3 | IO173NDB6V0 |
| Y4 | IO173PDB6V0 |
| Y5 | GEC1/IO169PPB6V0 |
| Y6 | GNDQ |
| Y7 | VMV6 |
| Y8 | VCCIB5 |
| Y9 | IO163NDB5V3 |
| Y10 | IO159PDB5V3 |
| Y11 | IO153PDB5V2 |
| Y12 | IO147PDB5V1 |
| Y13 | IO139PDB5V0 |
| Y14 | IO137PDB5V0 |
| Y15 | IO125NDB4V1 |
| Y16 | IO125PDB4V1 |
| Y17 | IO115NDB4V0 |
| Y18 | IO115PDB4V0 |
| Y19 | VCC |
| Y20 | VPUMP |
| Y21 | VCOMPLD |
| Y22 | VCCPLD |
| Y23 | IO100NDB3V1 |
| Y24 | IO100PDB3V1 |
| Y25 | IO96NDB3V1 |
| Y26 | IO98PDB3V1 |

| FG896 | |
|---|---|
| Pin Number | A3PE3000 Function |
| AG9 | IO225NPB5V3 |
| AG10 | IO223NPB5V3 |
| AG11 | IO221PDB5V3 |
| AG12 | IO221NDB5V3 |
| AG13 | IO205NPB5V1 |
| AG14 | IO199NDB5V0 |
| AG15 | IO199PDB5V0 |
| AG16 | IO187NDB4V4 |
| AG17 | IO187PDB4V4 |
| AG18 | IO181NDB4V3 |
| AG19 | IO171PPB4V2 |
| AG20 | IO165NPB4V1 |
| AG21 | IO161NPB4V0 |
| AG22 | IO159NDB4V0 |
| AG23 | IO159PDB4V0 |
| AG24 | IO158PPB4V0 |
| AG25 | GDB2/IO155PDB4V0 |
| AG26 | GDA2/IO154PPB4V0 |
| AG27 | GND |
| AG28 | VJTAG |
| AG29 | VCC |
| AG30 | IO149NDB3V4 |
| AH1 | GND |
| AH2 | IO233NPB5V4 |
| AH3 | VCC |
| AH4 | GEB2/IO232PPB5V4 |
| AH5 | VCCIB5 |
| AH6 | IO219NDB5V3 |
| AH7 | IO219PDB5V3 |
| AH8 | IO227NDB5V4 |
| AH9 | IO227PDB5V4 |
| AH10 | IO225PPB5V3 |
| AH11 | IO223PPB5V3 |
| AH12 | IO211NDB5V2 |
| AH13 | IO211PDB5V2 |
| AH14 | IO205PPB5V1 |

| FG896 | |
|---|---|
| Pin Number | A3PE3000 Function |
| AH15 | IO195NDB5V0 |
| AH16 | IO185NDB4V3 |
| AH17 | IO185PDB4V3 |
| AH18 | IO181PDB4V3 |
| AH19 | IO177NDB4V2 |
| AH20 | IO171NPB4V2 |
| AH21 | IO165PPB4V1 |
| AH22 | IO161PPB4V0 |
| AH23 | IO157NDB4V0 |
| AH24 | IO157PDB4V0 |
| AH25 | IO155NDB4V0 |
| AH26 | VCCIB4 |
| AH27 | TDI |
| AH28 | VCC |
| AH29 | VPUMP |
| AH30 | GND |
| AJ1 | GND |
| AJ2 | GND |
| AJ3 | GEA2/IO233PPB5V4 |
| AJ4 | VCC |
| AJ5 | IO217NPB5V2 |
| AJ6 | VCC |
| AJ7 | IO215NPB5V2 |
| AJ8 | IO213NDB5V2 |
| AJ9 | IO213PDB5V2 |
| AJ10 | IO209NDB5V1 |
| AJ11 | IO209PDB5V1 |
| AJ12 | IO203NDB5V1 |
| AJ13 | IO203PDB5V1 |
| AJ14 | IO197NDB5V0 |
| AJ15 | IO195PDB5V0 |
| AJ16 | IO183NDB4V3 |
| AJ17 | IO183PDB4V3 |
| AJ18 | IO179NPB4V3 |
| AJ19 | IO177PDB4V2 |
| AJ20 | IO173NDB4V2 |

| FG896 | |
|---|---|
| Pin Number | A3PE3000 Function |
| AJ21 | IO173PDB4V2 |
| AJ22 | IO163NDB4V1 |
| AJ23 | IO163PDB4V1 |
| AJ24 | IO167NPB4V1 |
| AJ25 | VCC |
| AJ26 | IO156NPB4V0 |
| AJ27 | VCC |
| AJ28 | TMS |
| AJ29 | GND |
| AJ30 | GND |
| AK2 | GND |
| AK3 | GND |
| AK4 | IO217PPB5V2 |
| AK5 | GND |
| AK6 | IO215PPB5V2 |
| AK7 | GND |
| AK8 | IO207NDB5V1 |
| AK9 | IO207PDB5V1 |
| AK10 | IO201NDB5V0 |
| AK11 | IO201PDB5V0 |
| AK12 | IO193NDB4V4 |
| AK13 | IO193PDB4V4 |
| AK14 | IO197PDB5V0 |
| AK15 | IO191NDB4V4 |
| AK16 | IO191PDB4V4 |
| AK17 | IO189NDB4V4 |
| AK18 | IO189PDB4V4 |
| AK19 | IO179PPB4V3 |
| AK20 | IO175NDB4V2 |
| AK21 | IO175PDB4V2 |
| AK22 | IO169NDB4V1 |
| AK23 | IO169PDB4V1 |
| AK24 | GND |
| AK25 | IO167PPB4V1 |
| AK26 | GND |
| AK27 | GDC2/IO156PPB4V0 |

| FG896 | |
|---|---|
| Pin Number | A3PE3000 Function |
| J5 | IO295NDB7V2 |
| J6 | IO299NDB7V3 |
| J7 | VCCIB7 |
| J8 | VCCPLA |
| J9 | VCC |
| J10 | IO04NPB0V0 |
| J11 | IO18NDB0V2 |
| J12 | IO20NDB0V2 |
| J13 | IO20PDB0V2 |
| J14 | IO32NDB0V3 |
| J15 | IO32PDB0V3 |
| J16 | IO42PDB1V0 |
| J17 | IO44NDB1V0 |
| J18 | IO44PDB1V0 |
| J19 | IO54NDB1V1 |
| J20 | IO54PDB1V1 |
| J21 | IO76NPB1V4 |
| J22 | VCC |
| J23 | VCCPLB |
| J24 | VCCIB2 |
| J25 | IO90PDB2V1 |
| J26 | IO90NDB2V1 |
| J27 | GBB2/IO83PDB2V0 |
| J28 | IO83NDB2V0 |
| J29 | IO91PDB2V1 |
| J30 | IO91NDB2V1 |
| K1 | IO288NDB7V1 |
| K2 | IO288PDB7V1 |
| K3 | IO304NDB7V3 |
| K4 | IO304PDB7V3 |
| K5 | GAB2/IO308PDB7V4 |
| K6 | IO308NDB7V4 |
| K7 | IO301PDB7V3 |
| K8 | IO301NDB7V3 |
| K9 | GAC2/IO307PPB7V4 |
| K10 | VCC |

| FG896 | |
|---|---|
| Pin Number | A3PE3000 Function |
| K11 | IO04PPB0V0 |
| K12 | VCCIB0 |
| K13 | VCCIB0 |
| K14 | VCCIB0 |
| K15 | VCCIB0 |
| K16 | VCCIB1 |
| K17 | VCCIB1 |
| K18 | VCCIB1 |
| K19 | VCCIB1 |
| K20 | IO76PPB1V4 |
| K21 | VCC |
| K22 | IO78PPB1V4 |
| K23 | IO88NDB2V0 |
| K24 | IO88PDB2V0 |
| K25 | IO94PDB2V1 |
| K26 | IO94NDB2V1 |
| K27 | IO85PDB2V0 |
| K28 | IO85NDB2V0 |
| K29 | IO93PDB2V1 |
| K30 | IO93NDB2V1 |
| L1 | IO286NDB7V1 |
| L2 | IO286PDB7V1 |
| L3 | IO298NDB7V3 |
| L4 | IO298PDB7V3 |
| L5 | IO283PDB7V1 |
| L6 | IO291NDB7V2 |
| L7 | IO291PDB7V2 |
| L8 | IO293PDB7V2 |
| L9 | IO293NDB7V2 |
| L10 | IO307NPB7V4 |
| L11 | VCC |
| L12 | VCC |
| L13 | VCC |
| L14 | VCC |
| L15 | VCC |
| L16 | VCC |

| FG896 | |
|---|---|
| Pin Number | A3PE3000 Function |
| L17 | VCC |
| L18 | VCC |
| L19 | VCC |
| L20 | VCC |
| L21 | IO78NPB1V4 |
| L22 | IO104NPB2V2 |
| L23 | IO98NDB2V2 |
| L24 | IO98PDB2V2 |
| L25 | IO87PDB2V0 |
| L26 | IO87NDB2V0 |
| L27 | IO97PDB2V1 |
| L28 | IO101PDB2V2 |
| L29 | IO103PDB2V2 |
| L30 | IO119NDB3V0 |
| M1 | IO282NDB7V1 |
| M2 | IO282PDB7V1 |
| M3 | IO292NDB7V2 |
| M4 | IO292PDB7V2 |
| M5 | IO283NDB7V1 |
| M6 | IO285PDB7V1 |
| M7 | IO287PDB7V1 |
| M8 | IO289PDB7V1 |
| M9 | IO289NDB7V1 |
| M10 | VCCIB7 |
| M11 | VCC |
| M12 | GND |
| M13 | GND |
| M14 | GND |
| M15 | GND |
| M16 | GND |
| M17 | GND |
| M18 | GND |
| M19 | GND |
| M20 | VCC |
| M21 | VCCIB2 |
| M22 | NC |

# 5 – Datasheet Information

## List of Changes

The following table lists critical changes that were made in each revision of the ProASIC3E datasheet.

| Revision | Changes | Page |
|---|---|---|
| Revision 15 (June 2015) | Updated "ProASIC3E Ordering Information". Interchanged the positions of Y- Security Feature and I- Application (Temperature Range) (SAR 67296).<br>Added Note "Only devices with package size greater than or equal to 5x5 are supported".<br>Updated Commercial and Industrial Junction Temperatures (SAR 67588). | *1-III* |
| | Added the A3PE3000 package to Table 2-5 (SARs 52320 and 58737). | *2-5* |
| | Updated "VCCIBx I/O Supply Voltage" (SAR 43323). | *3-1* |
| Revision 14 (May 2014) | Added 2 mA and 6 mA I/O short currents values in *"I/O Short Currents IOSH/IOSL"* (SAR 56295).<br>Added 2 mA and 6 mA minimum and maximum DC input and output levels in "Minimum and Maximum DC Input and Output Levels"(SAR 56295).<br>Added 3.3 V LVTTL / 3.3 V LVCMOS High Slew Commercial-Case Conditions for 2 mA and 6 mA in "3.3 V LVTTL / 3.3 V LVCMOS High Slew" (SAR 56295).<br>Added 3.3 V LVTTL / 3.3 V LVCMOS Low Slew Commercial-Case Conditions for 2 mA and 6 mA in "3.3 V LVTTL / 3.3 V LVCMOS Low Slew" (SAR 56295). | *2-22*<br>*2-24*<br>*2-25*<br>*2-25* |
| Revision 13 (January 2013) | In the "Features and Benefits" section, updated the Clock Conditioning Circuit (CCC) and PLL Wide Input Frequency Range from '1.5 MHz to 200 MHz' to '1.5MHz to 350 MHz' based on Table 2-98 (SAR 22196). | 1-I |
| | The "ProASIC3E Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43220). | 1-III |
| | Added a note to "Recommended Operating Conditions [1]" table (SAR 42716): The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C. | 2-2 |
| | The note in "ProASIC3E CCC/PLL Specification" table referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42571). | 2-70 |
| | Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40285).<br>Live at Power-Up (LAPU) has been replaced with 'Instant On'. | NA |
| Revision 12 (September 2012) | The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data. | 1-1 |

| Revision | Changes | Page |
|---|---|---|
| Revision 11 (August 2012) | Added a Note stating "VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information." to Table 2-1 • Absolute Maximum Ratings and Table 2-2 • Recommended Operating Conditions [1] (SAR 38322). | 2-1<br>3-1<br>2-1 |
| | The drive strength, IOL, and IOH value for 3.3 V GTL and 2.5 V GTL was changed from 25 mA to 20 mA in the following tables (SAR 31924):<br>"Summary of Maximum and Minimum DC Input and Output Levels" table<br>"Summary of I/O Timing Characteristics—Software Default Settings" table<br>"I/O Output Buffer Maximum Resistances[1]" table<br>"Minimum and Maximum DC Input and Output Levels" table)<br>"Minimum and Maximum DC Input and Output Levels" table<br>Also added note stating "Output drive strength is below JEDEC specification" for Tables 2-17 and 2-19.<br>Additionally, the IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected from 51 to 35 (for 3.3 V GTL+) and from 40 to 33 (for 2.5 V GTL+) in table Table 2-13 (SAR 39714). | <br><br>2-16<br>2-19<br>2-20<br>2-39<br>2-40 |
| | "Duration of Short Circuit Event Before Failure" table was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 37934). | 2-22 |
| | The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34796):<br>"It uses a 5 V–tolerant input buffer and push-pull output buffer." This change was made in revision 10 and omitted from the change table in error. | 2-30 |
| Revision 11 (continued) | Figure 2-11 was updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34889). | 2-38 |
| | In Table 2-81 VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 37222). | 2-52 |
| | Figure 2-47and Figure 2-48 are new (SAR 34848). | 2-79 |
| | The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions and Packaging" chapter: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with “Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks” (SAR 38322). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement. | 3-1 |

| Revision | Changes | Page |
|---|---|---|
| Revision 10 (continued) | "TBD" for 3.3 V LVCMOS Wide Range in Table 2-19 • I/O Output Buffer Maximum Resistances[1] and Table 2-21 • I/O Short Currents IOSH/IOSL was replaced by "Same as regular 3.3 V LVCMOS" (SAR 33853).<br>3.3 V LVCMOS Wide Range information was separated from regular 3.3 V LVCMOS and placed into its own new section, "3.3 V LVCMOS Wide Range". Values of IOSH and IOSL were added in Table 2-29 • Minimum and Maximum DC Input and Output Levels (SAR 33853). | 2-20, 2-27 |
| | The formulas in the table notes for Table 2-20 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 34755). | 2-21 |
| | The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34889). | 2-24 |
| | The titles and subtitles for Table 2-31 • 3.3 V LVCMOS Wide Range High Slew and Table 2-32 • 3.3 V LVCMOS Wide Range Low Slew were corrected (SAR 37227). | 2-28, 2-29 |
| | The following notes were removed from Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels (SAR 34812):<br>±5%<br>Differential input voltage = ±350 mV | 2-50 |
| | Minimum pulse width High and Low values were added to the tables in the "Global Tree Timing Characteristics" section. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 36957). | 2-68 |
| | A note was added to Table 2-98 • ProASIC3E CCC/PLL Specification indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34824). | 2-70 |
| | The following figures were deleted. Reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 34872).<br>Figure 2-44 • Write Access after Write onto Same Address<br>Figure 2-45 • Read Access after Write onto Same Address<br>Figure 2-46 • Write Access after Read onto Same Address<br>The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-49 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35750). | 2-74, 2-75, 2-79, 2-82 |
| | The "Pin Descriptions and Packaging" chapter is new (SAR 34771). | 3-1 |
| | Package names used in the "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 34771). | 4-1 |
| | Pin E6 for the FG256 package was corrected from VvB0 to VCCIB0 (SARs 30364, 31597, 26243). | 4-9 |
| July 2010 | The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "ProASIC3E Device Status" table on page II indicates the status for each device in the device family. | N/A |

| Revision | Changes | Page |
|---|---|---|
| Advance v0.5 (continued) | The "RESET" section was updated. | 2-25 |
| | The "RESET" section was updated. | 2-27 |
| | The "Introduction" of the "Introduction" section was updated. | 2-28 |
| | PCI-X 3.3 V was added to the Compatible Standards for 3.3 V in Table 2-11 • VCCI Voltages and Compatible Standards | 2-29 |
| | Table 2-35 • ProASIC3E I/O Features was updated. | 2-54 |
| | The "Double Data Rate (DDR) Support" section was updated to include information concerning implementation of the feature. | 2-32 |
| | The "Electrostatic Discharge (ESD) Protection" section was updated to include testing information. | 2-35 |
| | Level 3 and 4 descriptions were updated in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices. | 2-64 |
| | The notes in Table 2-45 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3E Devices were updated. | 2-64 |
| | The "Simultaneous Switching Outputs (SSOs) and Printed Circuit Board Layout" section is new. | 2-41 |
| | A footnote was added to Table 2-37 • Maximum I/O Frequency for Single-Ended and Differential I/Os in All Banks in ProASIC3E Devices (maximum drive strength and high slew selected). | 2-55 |
| | Table 2-48 • ProASIC3E I/O Attributes vs. I/O Standard Applications | 2-81 |
| | Table 2-55 • ProASIC3 I/O Standards—SLEW and Output Drive (OUT_DRIVE) Settings | 2-85 |
| | The "x" was updated in the "Pin Descriptions" section. | 2-50 |
| | The "VCC Core Supply Voltage" pin description was updated. | 2-50 |
| | The "VMVx I/O Supply Voltage (quiet)" pin description was updated to include information concerning leaving the pin unconnected. | 2-50 |
| | EXTFB was removed from Figure 2-24 • ProASIC3E CCC Options. | 2-24 |
| | The CCC Output Peak-to-Peak Period Jitter $F_{CCC\_OUT}$ was updated in Table 2-13 • ProASIC3E CCC/PLL Specification. | 2-30 |
| | EXTFB was removed from Figure 2-27 • CCC/PLL Macro. | 2-28 |
| | The LVPECL specification in Table 2-45 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3E Devices was updated. | 2-64 |
| | Table 2-15 • Levels of Hot-Swap Support was updated. | 2-34 |
| | The "Cold-Sparing Support" section was updated. | 2-34 |
| | "Electrostatic Discharge (ESD) Protection" section was updated. | 2-35 |
| | The VJTAG and I/O pin descriptions were updated in the "Pin Descriptions" section. | 2-50 |
| | The "VJTAG JTAG Supply Voltage" pin description was updated. | 2-50 |
| | The "VPUMP Programming Supply Voltage" pin description was updated to include information on what happens when the pin is tied to ground. | 2-50 |