Microchip Technology - M1A3PE3000-1PQ208 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	516096
Number of I/O	147
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3pe3000-1pq208

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-11 on page 2-11.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-11 on page 2-11.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-11 on page 2-11.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-11 on page 2-11.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-12 on page 2-11.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = PAC11 * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in Table 2-12 on page 2-11.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-12 on page 2-11.

PLL Contribution—P_{PLL}

$P_{PLL} = PAC13 + PAC14 * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.[1]

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[1] *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution (PAC14 * F_{CLKOUT} product) to the total PLL contribution.*

Table 2-22 • **Duration of Short Circuit Event Before Failure (continued)**

Temperature	Time before Failure
85°C	2 years
100°C	6 months

Table 2-23 • **Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

Table 2-24 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability***

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns *	20 years (110°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis.	20 years (110°C)
HSTL/SSTL/GTL	No requirement	10 ns *	10 years (100°C)
LVDS/B-LVDS/M-LVDS/ LVPECL	No requirement	10 ns *	10 years (100°C)

*Note: *For clock signals and similar edge-generating signals, refer to the "ProASIC3/E SSO and Pin Placement Guidelines" chapter of the ProASIC3E FPGA Fabric User's Guide. The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

***Table 2-51* • Minimum and Maximum DC Input and Output Levels**

2.5 GTL	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	**Min., V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[1]**	**Max. mA[1]**	**μA[2]**	**μA[2]**
20 mA[3]	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

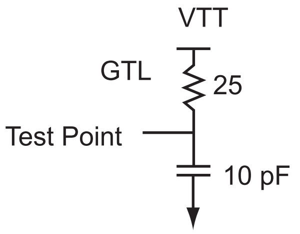


***Figure 2-13* • AC Loading**

***Table 2-52* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.05	VREF + 0.05	0.8	0.8	1.2	10

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

***Table 2-53* • 2.5 V GTL**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V VREF = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.60	2.13	0.04	2.46	0.43	2.16	2.13			4.40	4.36	ns
–1	0.51	1.81	0.04	2.09	0.36	1.84	1.81			3.74	3.71	ns
–2	0.45	1.59	0.03	1.83	0.32	1.61	1.59			3.28	3.26	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-66 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[1]**	**Max. mA[1]**	**μA[2]**	**μA[2]**
15 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15	87	83	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

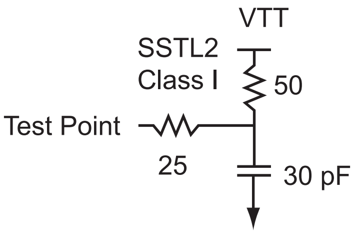


Figure 2-18 • AC Loading

Table 2-67 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

Note: **Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-68 • SSTL 2 Class I
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.13	0.04	1.33	0.43	2.17	1.85			4.40	4.08	ns
–1	0.56	1.81	0.04	1.14	0.36	1.84	1.57			3.74	3.47	ns
–2	0.49	1.59	0.03	1.00	0.32	1.62	1.38			3.29	3.05	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-69 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
18 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

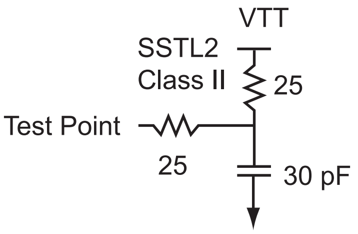


Figure 2-19 • AC Loading

Table 2-70 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

Note: **Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-71 • SSTL 2 Class II
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	0.66	2.17	0.04	1.33	0.43	2.21	1.77			4.44	ns
–1	0.56	0.56	1.84	0.04	1.14	0.36	1.88	1.51			3.78	ns
–2	0.49	0.49	1.62	0.03	1.00	0.32	1.65	1.32			3.32	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

Timing Characteristics

Table 2-80 • LVDS
Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.66	1.87	0.04	1.82	ns
–1	0.56	1.59	0.04	1.55	ns
–2	0.49	1.40	0.03	1.36	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-23. The input and output buffer delays are available in the LVDS section in Table 2-80.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: R_S = 60 Ω and R_T = 70 Ω, given Z_0 = 50 Ω (2") and Z_{stub} = 50 Ω (~1.5").

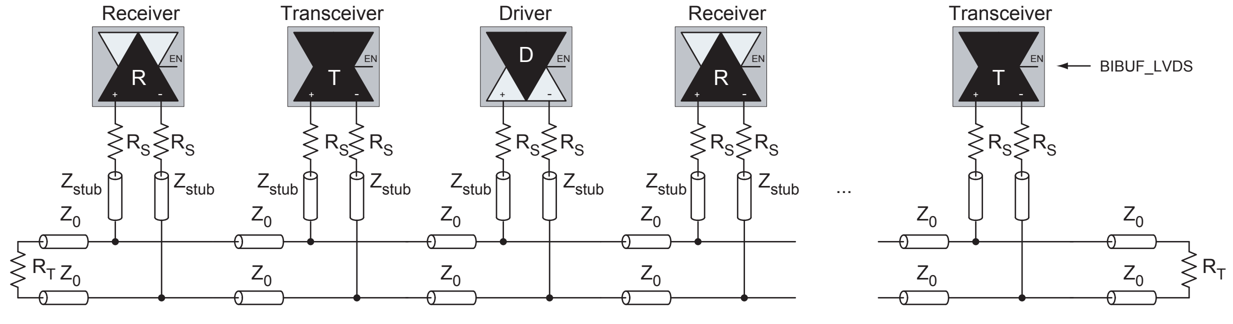


Figure 2-23 • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-24. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

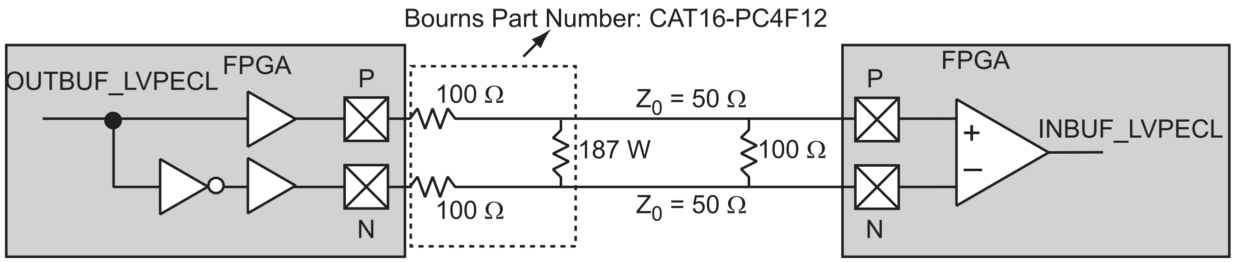


***Figure 2-24* • LVPECL Circuit Diagram and Board-Level Implementation**

***Table 2-81* • Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

***Table 2-82* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)
1.64	1.94	Cross point	–

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

***Table 2-83* • LVPECL**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.66	1.83	0.04	1.63	ns
–1	0.56	1.55	0.04	1.39	ns
–2	0.49	1.36	0.03	1.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

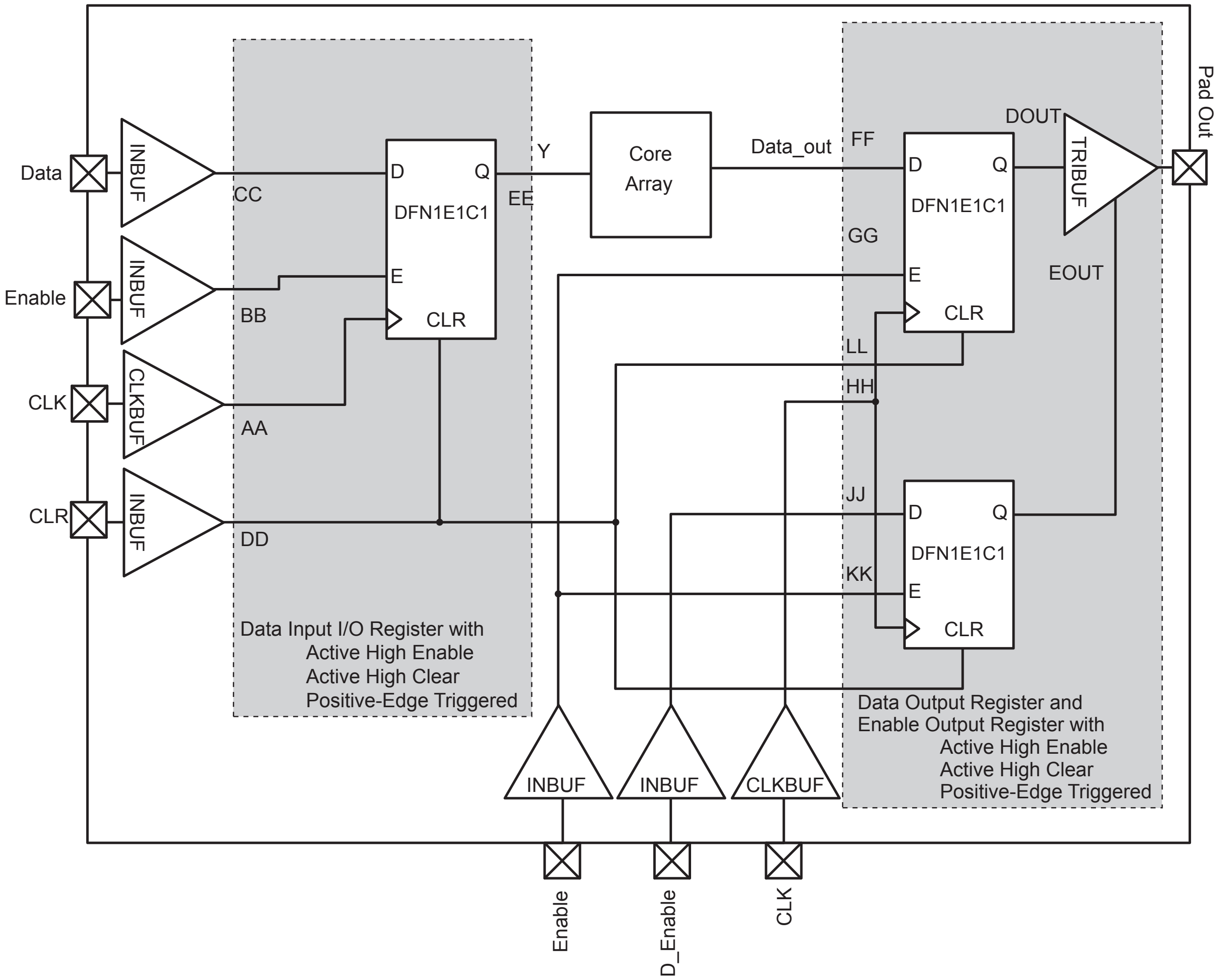


Figure 2-26 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

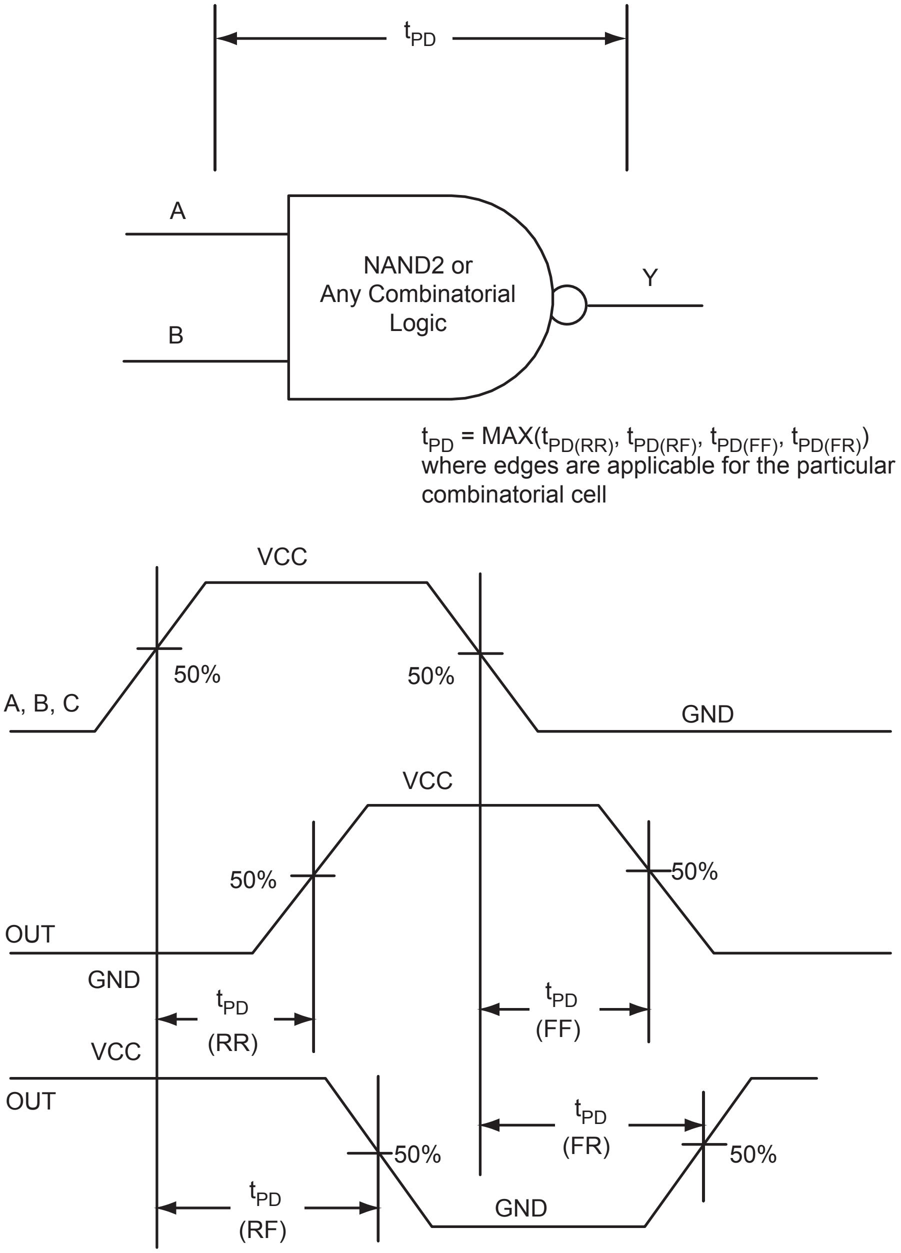


Figure 2-35 • **Timing Model and Waveforms**

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

***Table 2-98* • ProASIC3E CCC/PLL Specification**

Parameter	Minimum	Typical	Maximum	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		350	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		160[3]		ps
Serial Clock (SCLK) for Dynamic PLL[4]			125	MHz
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Max Peak-to-Peak Period Jitter			
	1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%		0.70%	
24 MHz to 100 MHz	1.00%		1.20%	
100 MHz to 250 MHz	1.75%		2.00%	
250 MHz to 350 MHz	2.50%		5.60%	
Acquisition Time LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter [5] LockControl = 0			1.6	ns
LockControl = 1			0.8	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2 [1,2]	0.025		5.56	ns
Delay Range in Block: Fixed Delay[1,4]		2.2		ns

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-5 for deratings*
2. *T_J = 25°C, VCC = 1.5 V.*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help for more information.*
4. *Maximum value obtained for a –2 speed-grade device in worst-case commercial conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*
5. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*

Refer to the I/O Structure section of the *ProASIC3E FPGA Fabric User's Guide* for an explanation of the naming of global pins.

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 W to 1 kΩ will satisfy the requirements. Refer to Table 3-1 for more information.

***Table 3-1* • Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on the JTAG chain*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin is pulled down.*

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-1 and must satisfy the parallel resistance value requirement. The values in Table 3-1 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

PQ208	
Pin Number	**A3PE600 Function**
108	TDO
109	TRST
110	VJTAG
111	VMV3
112	GDA0/IO67NPB3V1
113	GDB0/IO66NPB3V1
114	GDA1/IO67PPB3V1
115	GDB1/IO66PPB3V1
116	GDC0/IO65NDB3V1
117	GDC1/IO65PDB3V1
118	IO62NDB3V1
119	IO62PDB3V1
120	IO58NDB3V0
121	IO58PDB3V0
122	GND
123	VCCIB3
124	GCC2/IO55PSB3V0
125	GCB2/IO54PSB3V0
126	NC
127	IO53NDB3V0
128	GCA2/IO53PDB3V0
129	GCA1/IO52PPB3V0
130	GND
131	VCCPLC
132	GCA0/IO52NPB3V0
133	VCOMPLC
134	GCB0/IO51NDB2V1
135	GCB1/IO51PDB2V1
136	GCC1/IO50PSB2V1
137	IO49NDB2V1
138	IO49PDB2V1
139	IO48PSB2V1
140	VCCIB2
141	GND
142	VCC
143	IO47NDB2V1

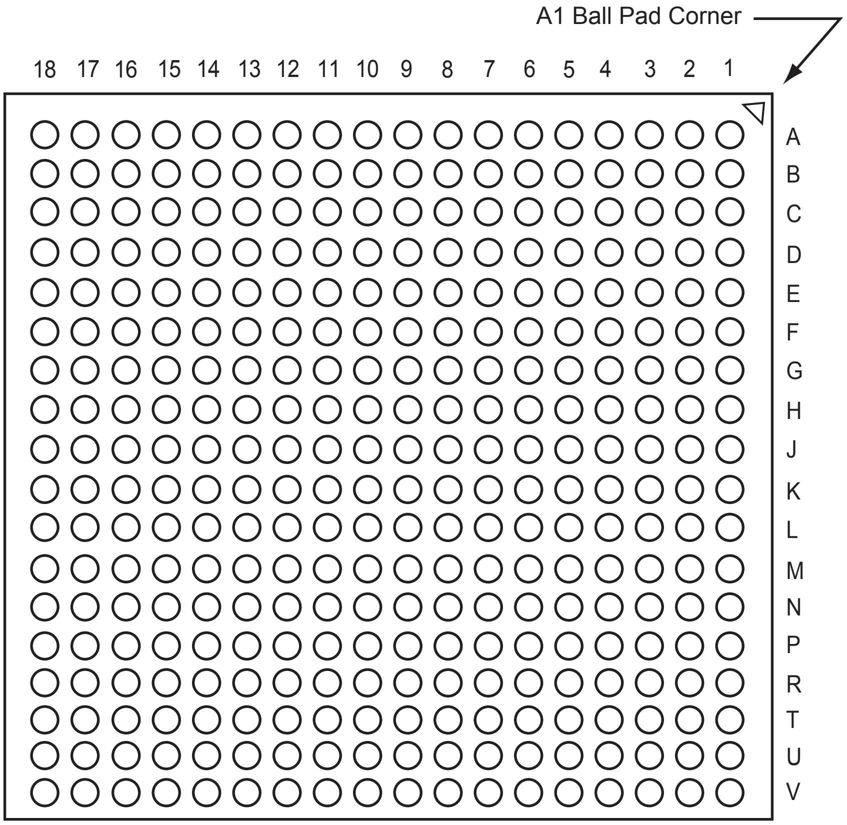
PQ208	
Pin Number	**A3PE600 Function**
144	IO47PDB2V1
145	IO44NDB2V1
146	IO44PDB2V1
147	IO43NDB2V0
148	IO43PDB2V0
149	IO40NDB2V0
150	IO40PDB2V0
151	GBC2/IO38PSB2V0
152	GBA2/IO36PSB2V0
153	GBB2/IO37PSB2V0
154	VMV2
155	GNDQ
156	GND
157	VMV1
158	GNDQ
159	GBA1/IO35PDB1V1
160	GBA0/IO35NDB1V1
161	GBB1/IO34PDB1V1
162	GND
163	GBB0/IO34NDB1V1
164	GBC1/IO33PDB1V1
165	GBC0/IO33NDB1V1
166	IO31PDB1V1
167	IO31NDB1V1
168	IO27PDB1V0
169	IO27NDB1V0
170	VCCIB1
171	VCC
172	IO23PPB1V0
173	IO22PSB1V0
174	IO23NPB1V0
175	IO21PDB1V0
176	IO21NDB1V0
177	IO19PPB0V2
178	GND
179	IO18PPB0V2

PQ208	
Pin Number	**A3PE600 Function**
180	IO19NPB0V2
181	IO18NPB0V2
182	IO17PPB0V2
183	IO16PPB0V2
184	IO17NPB0V2
185	IO16NPB0V2
186	VCCIB0
187	VCC
188	IO15PDB0V2
189	IO15NDB0V2
190	IO13PDB0V2
191	IO13NDB0V2
192	IO11PSB0V1
193	IO09PDB0V1
194	IO09NDB0V1
195	GND
196	IO07PDB0V1
197	IO07NDB0V1
198	IO05PDB0V0
199	IO05NDB0V0
200	VCCIB0
201	GAC1/IO02PDB0V0
202	GAC0/IO02NDB0V0
203	GAB1/IO01PDB0V0
204	GAB0/IO01NDB0V0
205	GAA1/IO00PDB0V0
206	GAA0/IO00NDB0V0
207	GNDQ
208	VMV0

PQ208	
Pin Number	**A3PE3000 Function**
118	IO134NDB3V2
119	IO134PDB3V2
120	IO132NDB3V2
121	IO132PDB3V2
122	GND
123	VCCIB3
124	GCC2/IO117PSB3V0
125	GCB2/IO116PSB3V0
126	NC
127	IO115NDB3V0
128	GCA2/IO115PDB3V0
129	GCA1/IO114PPB3V0
130	GND
131	VCCPLC
132	GCA0/IO114NPB3V0
133	VCOMPLC
134	GCB0/IO113NDB2V3
135	GCB1/IO113PDB2V3
136	GCC1/IO112PSB2V3
137	IO110NDB2V3
138	IO110PDB2V3
139	IO106PSB2V3
140	VCCIB2
141	GND
142	VCC
143	IO99NDB2V2
144	IO99PDB2V2
145	IO96NDB2V1
146	IO96PDB2V1
147	IO91NDB2V1
148	IO91PDB2V1
149	IO88NDB2V0
150	IO88PDB2V0
151	GBC2/IO84PSB2V0
152	GBA2/IO82PSB2V0
153	GBB2/IO83PSB2V0
154	VMV2
155	GNDQ
156	GND
157	VMV1
158	GNDQ
159	GBA1/IO81PDB1V4
160	GBA0/IO81NDB1V4
161	GBB1/IO80PDB1V4
162	GND
163	GBB0/IO80NDB1V4
164	GBC1/IO79PDB1V4
165	GBC0/IO79NDB1V4
166	IO74PDB1V4
167	IO74NDB1V4
168	IO70PDB1V3
169	IO70NDB1V3
170	VCCIB1
171	VCC
172	IO56PSB1V1
173	IO55PDB1V1
174	IO55NDB1V1
175	IO54PDB1V1
176	IO54NDB1V1
177	IO40PDB0V4
178	GND
179	IO40NDB0V4
180	IO37PDB0V4
181	IO37NDB0V4
182	IO35PDB0V4
183	IO35NDB0V4
184	IO32PDB0V3
185	IO32NDB0V3
186	VCCIB0
187	VCC
188	IO28PDB0V3
189	IO28NDB0V3
190	IO24PDB0V2
191	IO24NDB0V2
192	IO21PSB0V2
193	IO16PDB0V1
194	IO16NDB0V1
195	GND
196	IO11PDB0V1
197	IO11NDB0V1
198	IO08PDB0V0
199	IO08NDB0V0
200	VCCIB0
201	GAC1/IO02PDB0V0
202	GAC0/IO02NDB0V0
203	GAB1/IO01PDB0V0
204	GAB0/IO01NDB0V0
205	GAA1/IO00PDB0V0
206	GAA0/IO00NDB0V0
207	GNDQ
208	VMV0

FG256	
Pin Number	**A3PE600 Function**
A1	GND
A2	GAA0/IO00NDB0V0
A3	GAA1/IO00PDB0V0
A4	GAB0/IO01NDB0V0
A5	IO05PDB0V0
A6	IO10PDB0V1
A7	IO12PDB0V2
A8	IO16NDB0V2
A9	IO23NDB1V0
A10	IO23PDB1V0
A11	IO28NDB1V1
A12	IO28PDB1V1
A13	GBB1/IO34PDB1V1
A14	GBA0/IO35NDB1V1
A15	GBA1/IO35PDB1V1
A16	GND
B1	GAB2/IO133PDB7V1
B2	GAA2/IO134PDB7V1
B3	GNDQ
B4	GAB1/IO01PDB0V0
B5	IO05NDB0V0
B6	IO10NDB0V1
B7	IO12NDB0V2
B8	IO16PDB0V2
B9	IO20NDB1V0
B10	IO24NDB1V0
B11	IO24PDB1V0
B12	GBC1/IO33PDB1V1
B13	GBB0/IO34NDB1V1
B14	GNDQ
B15	GBA2/IO36PDB2V0
B16	IO42NDB2V0
C1	IO133NDB7V1
C2	IO134NDB7V1
C3	VMV7
C4	VCCPLA
C5	GAC0/IO02NDB0V0
C6	GAC1/IO02PDB0V0
C7	IO15NDB0V2
C8	IO15PDB0V2
C9	IO20PDB1V0
C10	IO25NDB1V0
C11	IO27PDB1V0
C12	GBC0/IO33NDB1V1
C13	VCCPLB
C14	VMV2
C15	IO36NDB2V0
C16	IO42PDB2V0
D1	IO128PDB7V1
D2	IO129PDB7V1
D3	GAC2/IO132PDB7V1
D4	VCOMPLA
D5	GNDQ
D6	IO09NDB0V1
D7	IO09PDB0V1
D8	IO13PDB0V2
D9	IO21PDB1V0
D10	IO25PDB1V0
D11	IO27NDB1V0
D12	GNDQ
D13	VCOMPLB
D14	GBB2/IO37PDB2V0
D15	IO39PDB2V0
D16	IO39NDB2V0
E1	IO128NDB7V1
E2	IO129NDB7V1
E3	IO132NDB7V1
E4	IO130PDB7V1
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO13NDB0V2
E9	IO21NDB1V0
E10	VCCIB1
E11	VCCIB1
E12	VMV1
E13	GBC2/IO38PDB2V0
E14	IO37NDB2V0
E15	IO41NDB2V0
E16	IO41PDB2V0
F1	IO124PDB7V0
F2	IO125PDB7V0
F3	IO126PDB7V0
F4	IO130NDB7V1
F5	VCCIB7
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB2
F13	IO38NDB2V0
F14	IO40NDB2V0
F15	IO40PDB2V0
F16	IO45PSB2V1
G1	IO124NDB7V0
G2	IO125NDB7V0
G3	IO126NDB7V0
G4	GFC1/IO120PPB7V0
G5	VCCIB7
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB2

FG324



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/products/fpga-soc/solutions*.

FG484	
Pin Number	**A3PE600 Function**
A1	GND
A2	GND
A3	VCCIB0
A4	IO06NDB0V1
A5	IO06PDB0V1
A6	IO08NDB0V1
A7	IO08PDB0V1
A8	IO11PDB0V1
A9	IO17PDB0V2
A10	IO18NDB0V2
A11	IO18PDB0V2
A12	IO22PDB1V0
A13	IO26PDB1V0
A14	IO29NDB1V1
A15	IO29PDB1V1
A16	IO31NDB1V1
A17	IO31PDB1V1
A18	IO32NDB1V1
A19	NC
A20	VCCIB1
A21	GND
A22	GND
AA1	GND
AA2	VCCIB6
AA3	NC
AA4	IO98PDB5V2
AA5	IO96NDB5V2
AA6	IO96PDB5V2
AA7	IO86NDB5V0
AA8	IO86PDB5V0
AA9	IO85PDB5V0
AA10	IO85NDB5V0
AA11	IO78PPB4V1
AA12	IO79NDB4V1
AA13	IO79PDB4V1
AA14	NC
AA15	NC
AA16	IO71NDB4V0
AA17	IO71PDB4V0
AA18	NC
AA19	NC
AA20	NC
AA21	VCCIB3
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB5
AB4	IO97NDB5V2
AB5	IO97PDB5V2
AB6	IO93NDB5V1
AB7	IO93PDB5V1
AB8	IO87NDB5V0
AB9	IO87PDB5V0
AB10	NC
AB11	NC
AB12	IO75NDB4V1
AB13	IO75PDB4V1
AB14	IO72NDB4V0
AB15	IO72PDB4V0
AB16	IO73NDB4V0
AB17	IO73PDB4V0
AB18	NC
AB19	NC
AB20	VCCIB4
AB21	GND
AB22	GND
B1	GND
B2	VCCIB7
B3	NC
B4	IO03NDB0V0
B5	IO03PDB0V0
B6	IO07NDB0V1
B7	IO07PDB0V1
B8	IO11NDB0V1
B9	IO17NDB0V2
B10	IO14PDB0V2
B11	IO19PDB0V2
B12	IO22NDB1V0
B13	IO26NDB1V0
B14	NC
B15	NC
B16	IO30NDB1V1
B17	IO30PDB1V1
B18	IO32PDB1V1
B19	NC
B20	NC
B21	VCCIB2
B22	GND
C1	VCCIB7
C2	NC
C3	NC
C4	NC
C5	GND
C6	IO04NDB0V0
C7	IO04PDB0V0
C8	VCC
C9	VCC
C10	IO14NDB0V2
C11	IO19NDB0V2
C12	NC
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC

FG484	
Pin Number	**A3PE600 Function**
H19	IO41PDB2V0
H20	VCC
H21	NC
H22	NC
J1	IO123NDB7V0
J2	IO123PDB7V0
J3	NC
J4	IO124PDB7V0
J5	IO125PDB7V0
J6	IO126PDB7V0
J7	IO130NDB7V1
J8	VCCIB7
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB2
J16	IO38NDB2V0
J17	IO40NDB2V0
J18	IO40PDB2V0
J19	IO45PPB2V1
J20	NC
J21	IO48PDB2V1
J22	IO46PDB2V1
K1	IO121NDB7V0
K2	IO121PDB7V0
K3	NC
K4	IO124NDB7V0
K5	IO125NDB7V0
K6	IO126NDB7V0
K7	GFC1/IO120PPB7V0
K8	VCCIB7
K9	VCC
K10	GND
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB2
K16	GCC1/IO50PPB2V1
K17	IO44NDB2V1
K18	IO44PDB2V1
K19	IO49NPB2V1
K20	IO45NPB2V1
K21	IO48NDB2V1
K22	IO46NDB2V1
L1	NC
L2	IO122PDB7V0
L3	IO122NDB7V0
L4	GFB0/IO119NPB7V0
L5	GFA0/IO118NDB6V1
L6	GFB1/IO119PPB7V0
L7	VCOMPLF
L8	GFC0/IO120NPB7V0
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO50NPB2V1
L16	GCB1/IO51PPB2V1
L17	GCA0/IO52NPB3V0
L18	VCOMPLC
L19	GCB0/IO51NPB2V1
L20	IO49PPB2V1
L21	IO47NDB2V1
L22	IO47PDB2V1
M1	NC
M2	IO114NPB6V1
M3	IO117NDB6V1
M4	GFA2/IO117PDB6V1
M5	GFA1/IO118PDB6V1
M6	VCCPLF
M7	IO116NDB6V1
M8	GFB2/IO116PDB6V1
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO54PPB3V0
M16	GCA1/IO52PPB3V0
M17	GCC2/IO55PPB3V0
M18	VCCPLC
M19	GCA2/IO53PDB3V0
M20	IO53NDB3V0
M21	IO56PDB3V0
M22	NC
N1	IO114PPB6V1
N2	IO111NDB6V1
N3	NC
N4	GFC2/IO115PPB6V1
N5	IO113PPB6V1
N6	IO112PDB6V1
N7	IO112NDB6V1
N8	VCCIB6
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB3
N16	IO54NPB3V0

FG676	
Pin Number	**A3PE1500 Function**
G13	IO21NDB0V2
G14	IO27PDB0V3
G15	IO35NDB1V0
G16	IO39PDB1V0
G17	IO51NDB1V2
G18	IO53NDB1V2
G19	VCCIB1
G20	GBA2/IO58PPB2V0
G21	GNDQ
G22	IO64NDB2V1
G23	IO64PDB2V1
G24	IO72PDB2V2
G25	IO72NDB2V2
G26	IO78PDB2V2
H1	IO208NDB7V2
H2	IO208PDB7V2
H3	IO209NDB7V2
H4	IO209PDB7V2
H5	IO219NDB7V3
H6	GAC2/IO219PDB7V3
H7	VCCIB7
H8	VCC
H9	VCCIB0
H10	VCCIB0
H11	VCCIB0
H12	VCCIB0
H13	VCCIB0
H14	VCCIB1
H15	VCCIB1
H16	VCCIB1
H17	VCCIB1
H18	VCCIB1
H19	VCC
H20	VCC
H21	IO58NPB2V0
H22	IO70PDB2V1

FG676	
Pin Number	**A3PE1500 Function**
H23	IO69PDB2V1
H24	IO76PDB2V2
H25	IO76NDB2V2
H26	IO78NDB2V2
J1	IO197NDB7V0
J2	IO197PDB7V0
J3	VMV7
J4	IO215NDB7V3
J5	IO215PDB7V3
J6	IO214PDB7V3
J7	IO214NDB7V3
J8	VCCIB7
J9	VCC
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	VCC
J15	VCC
J16	VCC
J17	VCC
J18	VCC
J19	VCCIB2
J20	IO62PDB2V0
J21	IO62NDB2V0
J22	IO70NDB2V1
J23	IO69NDB2V1
J24	VMV2
J25	IO80PDB2V3
J26	IO80NDB2V3
K1	IO195PDB7V0
K2	IO199NDB7V1
K3	IO199PDB7V1
K4	IO205NDB7V1
K5	IO205PDB7V1
K6	IO217PDB7V3

FG676	
Pin Number	**A3PE1500 Function**
K7	IO217NDB7V3
K8	VCCIB7
K9	VCC
K10	GND
K11	GND
K12	GND
K13	GND
K14	GND
K15	GND
K16	GND
K17	GND
K18	VCC
K19	VCCIB2
K20	IO65PDB2V1
K21	IO65NDB2V1
K22	IO74PDB2V2
K23	IO74NDB2V2
K24	IO75PDB2V2
K25	IO75NDB2V2
K26	IO84PDB2V3
L1	IO195NDB7V0
L2	IO198PPB7V0
L3	GNDQ
L4	IO201PDB7V1
L5	IO201NDB7V1
L6	IO210NDB7V2
L7	IO210PDB7V2
L8	VCCIB7
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	GND
L15	GND
L16	GND

FG896	
Pin Number	A3PE3000 Function
E17	IO49PDB1V1
E18	IO50PDB1V1
E19	IO58PDB1V2
E20	IO60NDB1V2
E21	IO77PDB1V4
E22	IO68NDB1V3
E23	IO68PDB1V3
E24	VCCIB1
E25	IO74PDB1V4
E26	VCC
E27	GBB1/IO80PPB1V4
E28	VCCIB2
E29	IO82NPB2V0
E30	GND
F1	IO296PPB7V2
F2	VCC
F3	IO306PDB7V4
F4	IO297PDB7V2
F5	VMV7
F6	GND
F7	GNDQ
F8	IO12NDB0V1
F9	IO12PDB0V1
F10	IO10PDB0V1
F11	IO16PDB0V1
F12	IO22NDB0V2
F13	IO30NDB0V3
F14	IO30PDB0V3
F15	IO36PDB0V4
F16	IO48NDB1V0
F17	IO48PDB1V0
F18	IO50NDB1V1
F19	IO58NDB1V2
F20	IO60PDB1V2
F21	IO77NDB1V4
F22	IO72NDB1V3
F23	IO72PDB1V3
F24	GNDQ
F25	GND
F26	VMV2
F27	IO86PDB2V0
F28	IO92PDB2V1
F29	VCC
F30	IO100NPB2V2
G1	GND
G2	IO296NPB7V2
G3	IO306NDB7V4
G4	IO297NDB7V2
G5	VCCIB7
G6	GNDQ
G7	VCC
G8	VMV0
G9	VCCIB0
G10	IO10NDB0V1
G11	IO16NDB0V1
G12	IO22PDB0V2
G13	IO26PPB0V3
G14	IO38NPB0V4
G15	IO36NDB0V4
G16	IO46NDB1V0
G17	IO46PDB1V0
G18	IO56NDB1V1
G19	IO56PDB1V1
G20	IO66NDB1V3
G21	IO66PDB1V3
G22	VCCIB1
G23	VMV1
G24	VCC
G25	GNDQ
G26	VCCIB2
G27	IO86NDB2V0
G28	IO92NDB2V1
G29	IO100PPB2V2
G30	GND
H1	IO294PDB7V2
H2	IO294NDB7V2
H3	IO300NDB7V3
H4	IO300PDB7V3
H5	IO295PDB7V2
H6	IO299PDB7V3
H7	VCOMPLA
H8	GND
H9	IO08NDB0V0
H10	IO08PDB0V0
H11	IO18PDB0V2
H12	IO26NPB0V3
H13	IO28NDB0V3
H14	IO28PDB0V3
H15	IO38PPB0V4
H16	IO42NDB1V0
H17	IO52NDB1V1
H18	IO52PDB1V1
H19	IO62NDB1V2
H20	IO62PDB1V2
H21	IO70NDB1V3
H22	IO70PDB1V3
H23	GND
H24	VCOMPLB
H25	GBC2/IO84PDB2V0
H26	IO84NDB2V0
H27	IO96PDB2V1
H28	IO96NDB2V1
H29	IO89PDB2V0
H30	IO89NDB2V0
J1	IO290NDB7V2
J2	IO290PDB7V2
J3	IO302NDB7V3
J4	IO302PDB7V3

Revision	Changes	Page
v2.0 (continued)	Table 3-6 • Temperature and Voltage Derating Factors for Timing Delays was updated.	3-5
	Table 3-5 • Package Thermal Resistivities was updated.	3-5
	Table 3-10 • Different Components Contributing to the Dynamic Power Consumption in ProASIC3E Devices was updated.	3-8
	t_{WRO} and t_{CCKH} were added to Table 3-94 • RAM4K9 and Table 3-95 • RAM512X18.	3-74 to 3-74
	The note in Table 3-24 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was updated.	3-23
	Figure 3-43 • Write Access After Write onto Same Address, Figure 3-44 • Read Access After Write onto Same Address, and Figure 3-45 • Write Access After Read onto Same Address are new.	3-71 to 3-73
	Figure 3-53 • Timing Diagram was updated.	3-80
	Notes were added to the package diagrams identifying if they were top or bottom view.	N/A
	The A3PE1500 "208-Pin PQFP" table is new.	4-4
	The A3PE1500 "484-Pin FBGA" table is new.	4-18
	The A3PE1500 "A3PE1500 Function" table is new.	4-24
Advance v0.6 (January 2007)	In the "Packaging Tables" table, the number of I/Os for the A3PE1500 was changed for the FG484 and FG676 packages.	ii
Advance v0.5 (April 2006)	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	Figure 2-8 • Very-Long-Line Resources was updated.	2-8
	The footnotes in Figure 2-27 • CCC/PLL Macro were updated.	2-28
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options.	2-24
	The "SRAM and FIFO" section was updated.	2-21
	The "RESET" section was updated.	2-25
	The "WCLK and RCLK" section was updated.	2-25
	The "RESET" section was updated.	2-25
	The "RESET" section was updated.	2-27
	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	Figure 2-8 • Very-Long-Line Resources was updated.	2-8
	The footnotes in Figure 2-27 • CCC/PLL Macro were updated.	2-28
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options.	2-24
	The "SRAM and FIFO" section was updated.	2-21
	The "RESET" section was updated.	2-25
	The "WCLK and RCLK" section was updated.	2-25