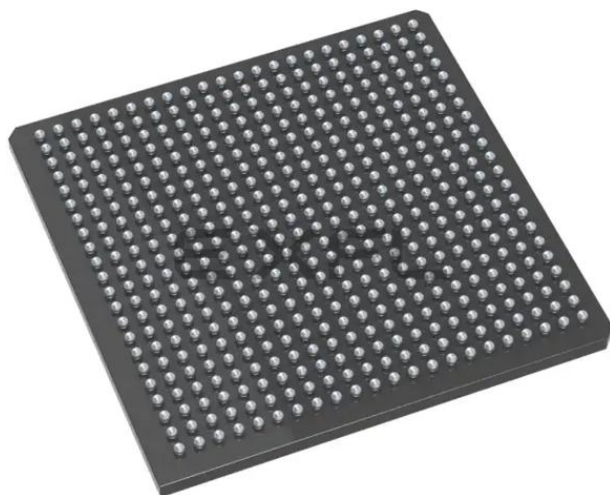




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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	516096
Number of I/O	341
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3pe3000-2fg484i

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Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-15 • Summary of AC Measuring Points

Standard	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_REF)	Measuring Trip Point (Vtrip)
3.3 V LVTTTL / 3.3 V LVCMOS	–	–	1.4 V
3.3 V LVCMOS Wide Range	–	–	1.4 V
2.5 V LVCMOS	–	–	1.2 V
1.8 V LVCMOS	–	–	0.90 V
1.5 V LVCMOS	–	–	0.75 V
3.3 V PCI	–	–	0.285 * VCCI (RR) 0.615 * VCCI (FF))
3.3 V PCI-X	–	–	0.285 * VCCI (RR) 0.615 * VCCI (FF)
3.3 V GTL	0.8 V	1.2 V	VREF
2.5 V GTL	0.8 V	1.2 V	VREF
3.3 V GTL+	1.0 V	1.5 V	VREF
2.5 V GTL+	1.0 V	1.5 V	VREF
HSTL (I)	0.75 V	0.75 V	VREF
HSTL (II)	0.75 V	0.75 V	VREF
SSTL2 (I)	1.25 V	1.25 V	VREF
SSTL2 (II)	1.25 V	1.25 V	VREF
SSTL3 (I)	1.5 V	1.485 V	VREF
SSTL3 (II)	1.5 V	1.485 V	VREF
LVDS	–	–	Cross point
LVPECL	–	–	Cross point

Table 2-16 • I/O AC Parameter Definitions

Parameter	Definition
t _{DP}	Data to Pad delay through the Output Buffer
t _{PY}	Pad to Data delay through the Input Buffer with Schmitt trigger disabled
t _{DOUT}	Data to Output Buffer delay through the I/O interface
t _{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t _{DIN}	Input Buffer to Data delay through the I/O interface
t _{PYS}	Pad to Data delay through the Input Buffer with Schmitt trigger enabled
t _{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t _{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t _{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t _{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t _{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t _{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

Table 2-19 • I/O Output Buffer Maximum Resistances¹ (continued)

Standard	Drive Strength	R _{PULL-DOWN} (Ω) ²	R _{PULL-UP} (Ω) ³
3.3 V GTL+	35 mA	12	–
2.5 V GTL+	33 mA	15	–
HSTL (I)	8 mA	50	50
HSTL (II)	15 mA ⁴	25	25
SSTL2 (I)	15 mA	27	31
SSTL2 (II)	18 mA	13	15
SSTL3 (I)	14 mA	44	69
SSTL3 (II)	21 mA	18	32

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website at www.microsemi.com/index.php?option=com_content&id=1671&lang=en&view=article.
2. $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / IOL_{spec}$
3. $R_{(PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / IOH_{spec}$
4. Output drive strength is below JEDEC specification.

**Table 2-20 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values**

VCCI	R _(WEAK PULL-UP) ¹ (Ω)		R _(WEAK PULL-DOWN) ² (Ω)	
	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
3.3 V (Wide Range I/Os)	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / I_{(WEAK PULL-UP-MIN)}$
2. $R_{(WEAK PULL-DOWN-MAX)} = (VOL_{spec}) / I_{(WEAK PULL-DOWN-MIN)}$

Timing Characteristics

Table 2-31 • 3.3 V LVCMOS Wide Range High Slew
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	4 mA	Std.	0.66	12.19	0.04	1.83	2.38	0.43	12.19	10.17	4.16	4.00	15.58	13.57	ns
		–1	0.56	10.37	0.04	1.55	2.02	0.36	10.37	8.66	3.54	3.41	13.26	11.54	ns
		–2	0.49	9.10	0.03	1.36	1.78	0.32	9.10	7.60	3.11	2.99	11.64	10.13	ns
100 μA	8 mA	Std.	0.66	7.85	0.04	1.83	2.38	0.43	7.85	6.29	4.71	4.97	11.24	9.68	ns
		–1	0.56	6.68	0.04	1.55	2.02	0.36	6.68	5.35	4.01	4.22	9.57	8.24	ns
		–2	0.49	5.86	0.03	1.36	1.78	0.32	5.86	4.70	3.52	3.71	8.40	7.23	ns
100 μA	12 mA	Std.	0.66	5.67	0.04	1.83	2.38	0.43	5.67	4.36	5.06	5.59	9.07	7.75	ns
		–1	0.56	4.82	0.04	1.55	2.02	0.36	4.82	3.71	4.31	4.75	7.71	6.59	ns
		–2	0.49	4.24	0.03	1.36	1.78	0.32	4.24	3.25	3.78	4.17	6.77	5.79	ns
100 μA	16 mA	Std.	0.66	5.35	0.04	1.83	2.38	0.43	5.35	3.96	5.15	5.76	8.75	7.35	ns
		–1	0.56	4.55	0.04	1.55	2.02	0.36	4.55	3.36	4.38	4.90	7.44	6.25	ns
		–2	0.49	4.00	0.03	1.36	1.78	0.32	4.00	2.95	3.85	4.30	6.53	5.49	ns
100 μA	24 mA	Std.	0.66	4.96	0.04	1.83	2.38	0.43	4.96	3.27	5.23	6.38	8.35	6.67	ns
		–1	0.56	4.22	0.04	1.55	2.02	0.36	4.22	2.78	4.45	5.43	7.11	5.67	ns
		–2	0.49	3.70	0.03	1.36	1.78	0.32	3.70	2.44	3.91	4.76	6.24	4.98	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. Software default selection highlighted in gray.
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

Timing Characteristics

Table 2-35 • 2.5 V LVCMOS High Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	8.82	0.04	1.51	1.66	0.43	8.13	8.82	2.72	2.29	10.37	11.05	ns
	–1	0.56	7.50	0.04	1.29	1.41	0.36	6.92	7.50	2.31	1.95	8.82	9.40	ns
	–2	0.49	6.58	0.03	1.13	1.24	0.32	6.07	6.58	2.03	1.71	7.74	8.25	ns
8 mA	Std.	0.66	5.27	0.04	1.51	1.66	0.43	5.27	5.27	3.10	3.03	7.50	7.51	ns
	–1	0.56	4.48	0.04	1.29	1.41	0.36	4.48	4.48	2.64	2.58	6.38	6.38	ns
	–2	0.49	3.94	0.03	1.13	1.24	0.32	3.93	3.94	2.32	2.26	5.60	5.61	ns
12 mA	Std.	0.66	3.74	0.04	1.51	1.66	0.43	3.81	3.49	3.37	3.49	6.05	5.73	ns
	–1	0.56	3.18	0.04	1.29	1.41	0.36	3.24	2.97	2.86	2.97	5.15	4.87	ns
	–2	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28	ns
16 mA	Std.	0.66	3.53	0.04	1.51	1.66	0.43	3.59	3.12	3.42	3.62	5.83	5.35	ns
	–1	0.56	3.00	0.04	1.29	1.41	0.36	3.06	2.65	2.91	3.08	4.96	4.55	ns
	–2	0.49	2.63	0.03	1.13	1.24	0.32	2.68	2.33	2.56	2.71	4.35	4.00	ns
24 mA	Std.	0.66	3.26	0.04	1.51	1.66	0.43	3.32	2.48	3.49	4.11	5.56	4.72	ns
	–1	0.56	2.77	0.04	1.29	1.41	0.36	2.83	2.11	2.97	3.49	4.73	4.01	ns
	–2	0.49	2.44	0.03	1.13	1.24	0.32	2.48	1.85	2.61	3.07	4.15	3.52	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

Timing Characteristics

Table 2-39 • 1.8 V LVCMOS High Slew

Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.7\text{ V}$

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	12.10	0.04	1.45	1.91	0.43	9.59	12.10	2.78	1.64	11.83	14.34	ns
	–1	0.56	10.30	0.04	1.23	1.62	0.36	8.16	10.30	2.37	1.39	10.06	12.20	ns
	–2	0.49	9.04	0.03	1.08	1.42	0.32	7.16	9.04	2.08	1.22	8.83	10.71	ns
4 mA	Std.	0.66	7.05	0.04	1.45	1.91	0.43	6.20	7.05	3.25	2.86	8.44	9.29	ns
	–1	0.56	6.00	0.04	1.23	1.62	0.36	5.28	6.00	2.76	2.44	7.18	7.90	ns
	–2	0.49	5.27	0.03	1.08	1.42	0.32	4.63	5.27	2.43	2.14	6.30	6.94	ns
6 mA	Std.	0.66	4.52	0.04	1.45	1.91	0.43	4.47	4.52	3.57	3.47	6.70	6.76	ns
	–1	0.56	3.85	0.04	1.23	1.62	0.36	3.80	3.85	3.04	2.95	5.70	5.75	ns
	–2	0.49	3.38	0.03	1.08	1.42	0.32	3.33	3.38	2.66	2.59	5.00	5.05	ns
8 mA	Std.	0.66	4.12	0.04	1.45	1.91	0.43	4.20	3.99	3.63	3.62	6.43	6.23	ns
	–1	0.56	3.51	0.04	1.23	1.62	0.36	3.57	3.40	3.09	3.08	5.47	5.30	ns
	–2	0.49	3.08	0.03	1.08	1.42	0.32	3.14	2.98	2.71	2.71	4.81	4.65	ns
12 mA	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	–1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	–2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns
16 mA	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	–1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	–2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

Voltage-Referenced I/O Characteristics

3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-48 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
20 mA ³	−0.3	VREF − 0.05	VREF + 0.05	3.6	0.4	−	20	20	181	268	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Output drive strength is below JEDEC specification.

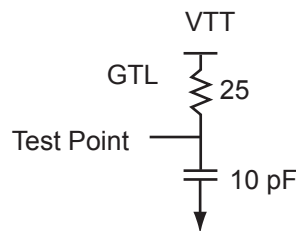


Figure 2-12 • AC Loading

Table 2-49 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF − 0.05	VREF + 0.05	0.8	0.8	1.2	10

Note: *Measuring point = V_{trip}. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-50 • 3.3 V GTL

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V VREF = 0.8 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.60	2.08	0.04	2.93	0.43	2.04	2.08			4.27	4.31	ns
−1	0.51	1.77	0.04	2.50	0.36	1.73	1.77			3.63	3.67	ns
−2	0.45	1.55	0.03	2.19	0.32	1.52	1.55			3.19	3.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-60 • Minimum and Maximum DC Input and Output Levels

HSTL Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
8 mA	−0.3	VREF − 0.1	VREF + 0.1	3.6	0.4	VCCI − 0.4	8	8	39	32	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.

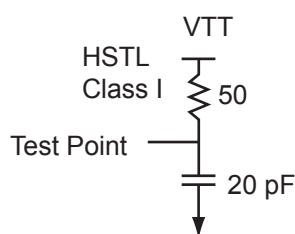


Figure 2-16 • AC Loading

Table 2-61 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF − 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-62 • HSTL Class I

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = .4 V, VREF = 0.75 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.66	3.18	0.04	2.12	0.43	3.24	3.14			5.47	5.38	ns
−1	0.56	2.70	0.04	1.81	0.36	2.75	2.67			4.66	4.58	ns
−2	0.49	2.37	0.03	1.59	0.32	2.42	2.35			4.09	4.02	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-63 • Minimum and Maximum DC Input and Output Levels

HSTL Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
15 mA ³	-0.3	VREF - 0.1	VREF + 0.1	3.6	0.4	VCCI - 0.4	15	15	55	66	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Output drive strength is below JEDEC specification.

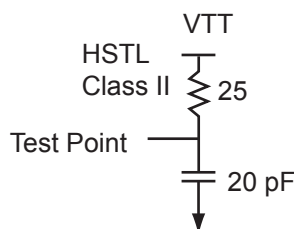


Figure 2-17 • AC Loading

Table 2-64 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF - 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-65 • HSTL Class II

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 1.4 V, VREF = 0.75 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.66	3.02	0.04	2.12	0.43	3.08	2.71			5.32	4.95	ns
-1	0.56	2.57	0.04	1.81	0.36	2.62	2.31			4.52	4.21	ns
-2	0.49	2.26	0.03	1.59	0.32	2.30	2.03			3.97	3.70	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-75 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
21 mA	−0.3	VREF − 0.2	VREF + 0.2	3.6	0.5	VCCI − 0.9	21	21	109	103	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.

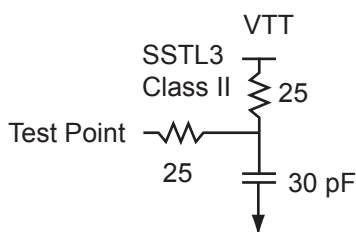


Figure 2-21 • AC Loading

Table 2-76 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF − 0.2	VREF + 0.2	1.5	1.5	1.485	30

Note: *Measuring point = V_{trip}. See [Table 2-15 on page 2-18](#) for a complete table of trip points.

Timing Characteristics

Table 2-77 • SSTL3 Class II

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 1.5 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.66	2.07	0.04	1.25	0.43	2.10	1.67			4.34	3.91	ns
−1	0.56	1.76	0.04	1.06	0.36	1.79	1.42			3.69	3.32	ns
−2	0.49	1.54	0.03	0.93	0.32	1.57	1.25			3.24	2.92	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

Global Resource Characteristics

A3PE600 Clock Tree Topology

Clock delays are device-specific. [Figure 2-38](#) is an example of a global tree used for clock routing. The global tree presented in [Figure 2-38](#) is driven by a CCC located on the west side of the A3PE600 device. It is used to drive all D-flip-flops in the device.

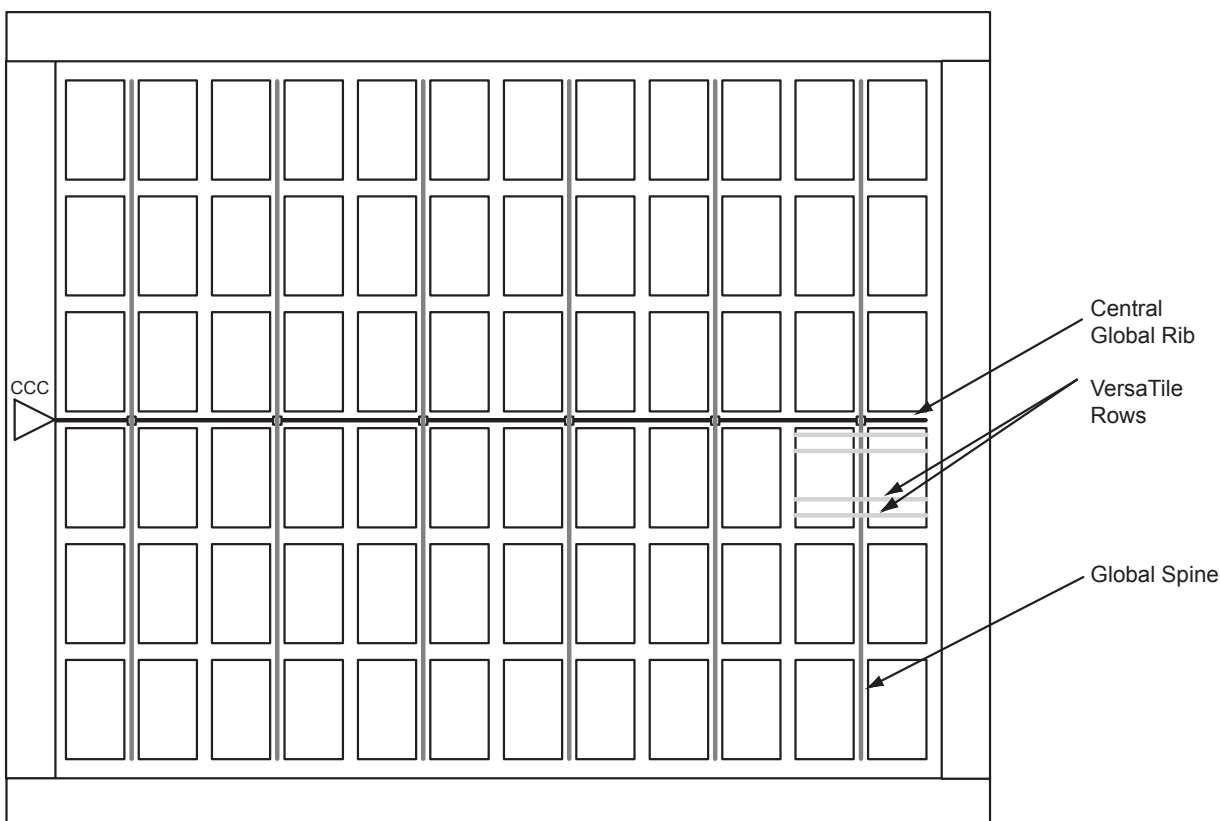


Figure 2-38 • Example of Global Tree Use in an A3PE600 Device for Clock Routing

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the ["Clock Conditioning Circuits"](#) section on [page 2-70](#). [Table 2-95](#) on [page 2-69](#), [Table 2-96](#) on [page 2-69](#), and [Table 2-97](#) on [page 2-69](#) present minimum and maximum global clock delays within the device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Waveforms

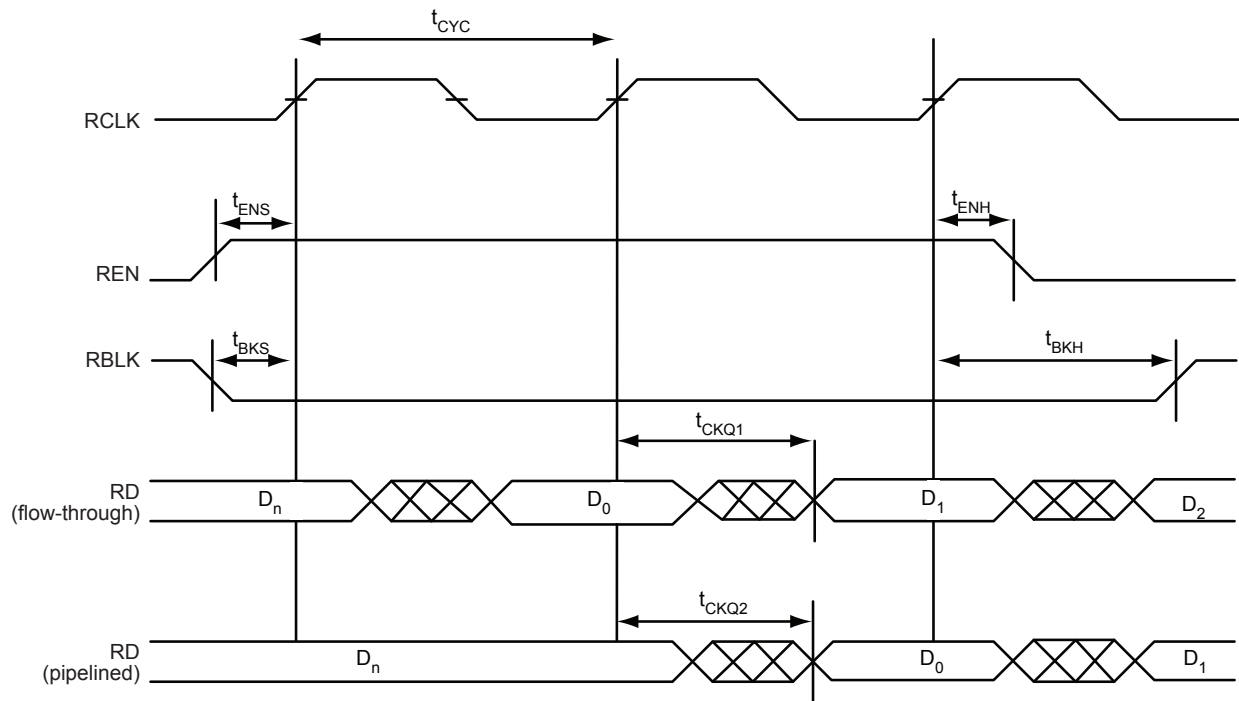


Figure 2-47 • FIFO Read

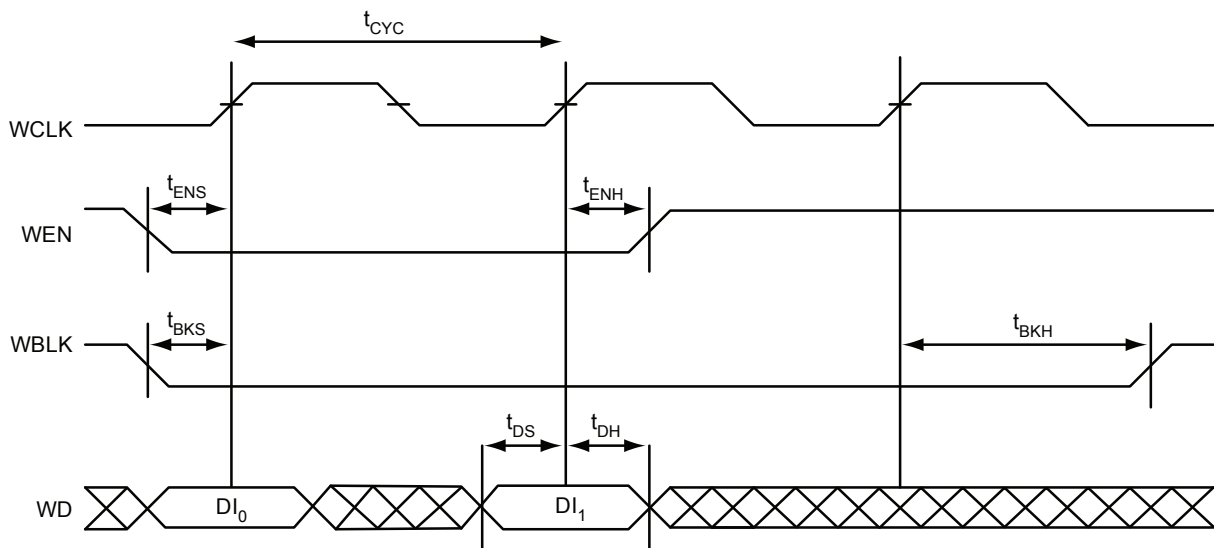


Figure 2-48 • FIFO Write

Timing Characteristics

Table 2-101 • FIFO

Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–2	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.38	1.57	1.84	ns
t_{ENH}	REN, WEN Hold Time	0.02	0.02	0.02	ns
t_{BKS}	BLK Setup Time	0.19	0.22	0.26	ns
t_{BKH}	BLK Hold Time	0.00	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (pass-through)	2.36	2.68	3.15	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.89	1.02	1.20	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (pass-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on RD (pipelined)	0.92	1.05	1.23	ns
t_{REMRSTB}	RESET Removal	0.29	0.33	0.38	ns
t_{RECRSTB}	RESET Recovery	1.50	1.71	2.01	ns
t_{MPWRSTB}	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency	310	272	231	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

PQ208	
Pin Number	A3PE3000 Function
1	GND
2	GNDQ
3	VMV7
4	GAB2/IO308PSB7V4
5	GAA2/IO309PDB7V4
6	IO309NDB7V4
7	GAC2/IO307PDB7V4
8	IO307NDB7V4
9	IO303PDB7V3
10	IO303NDB7V3
11	IO299PDB7V3
12	IO299NDB7V3
13	IO295PDB7V2
14	IO295NDB7V2
15	IO291PSB7V2
16	VCC
17	GND
18	VCCIB7
19	IO285PDB7V1
20	IO285NDB7V1
21	IO279PSB7V0
22	GFC1/IO275PSB7V0
23	GFB1/IO274PDB7V0
24	GFB0/IO274NDB7V0
25	VCOMPLF
26	GFA0/IO273NPB6V4
27	VCCPLF
28	GFA1/IO273PPB6V4
29	GND
30	GFA2/IO272PDB6V4
31	IO272NDB6V4
32	GFB2/IO271PPB6V4
33	GFC2/IO270PPB6V4
34	IO271NPB6V4
35	IO270NPB6V4
36	VCC
37	IO252PDB6V2
38	IO252NDB6V2
39	IO248PSB6V1

PQ208	
Pin Number	A3PE3000 Function
40	VCCIB6
41	GND
42	IO244PDB6V1
43	IO244NDB6V1
44	GEC1/IO236PDB6V0
45	GEC0/IO236NDB6V0
46	GEB1/IO235PPB6V0
47	GEA1/IO234PPB6V0
48	GEB0/IO235NPB6V0
49	GEA0/IO234NPB6V0
50	VMV6
51	GNDQ
52	GND
53	VMV5
54	GNDQ
55	IO233NDB5V4
56	GEA2/IO233PDB5V4
57	IO232NDB5V4
58	GEB2/IO232PDB5V4
59	IO231NDB5V4
60	GEC2/IO231PDB5V4
61	IO230PSB5V4
62	VCCIB5
63	IO218NDB5V3
64	IO218PDB5V3
65	GND
66	IO214PSB5V2
67	IO212NDB5V2
68	IO212PDB5V2
69	IO208NDB5V1
70	IO208PDB5V1
71	VCC
72	VCCIB5
73	IO202NDB5V1
74	IO202PDB5V1
75	IO198NDB5V0
76	IO198PDB5V0
77	IO197NDB5V0
78	IO197PDB5V0

PQ208	
Pin Number	A3PE3000 Function
79	IO194NDB5V0
80	IO194PDB5V0
81	GND
82	IO184NDB4V3
83	IO184PDB4V3
84	IO180NDB4V3
85	IO180PDB4V3
86	IO176NDB4V2
87	IO176PDB4V2
88	VCC
89	VCCIB4
90	IO170NDB4V2
91	IO170PDB4V2
92	IO166NDB4V1
93	IO166PDB4V1
94	IO156NDB4V0
95	GDC2/IO156PDB4V0
96	IO154NPB4V0
97	GND
98	GDB2/IO155PSB4V0
99	GDA2/IO154PPB4V0
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV4
105	GND
106	VPUMP
107	GNDQ
108	TDO
109	TRST
110	VJTAG
111	VMV3
112	GDA0/IO153NPB3V4
113	GDB0/IO152NPB3V4
114	GDA1/IO153PPB3V4
115	GDB1/IO152PPB3V4
116	GDC0/IO151NDB3V4
117	GDC1/IO151PDB3V4

FG324	
Pin Number	A3PE3000 FBGA
G1	GND
G2	IO287PDB7V1
G3	IO287NDB7V1
G4	IO283PPB7V1
G5	VCCIB7
G6	IO279PDB7V0
G7	IO291NPB7V2
G8	VCC
G9	IO26NDB0V3
G10	IO34NDB0V4
G11	VCC
G12	IO94NPB2V1
G13	IO98PDB2V2
G14	VCCIB2
G15	GCC0/IO112NPB2V3
G16	IO104PDB2V2
G17	IO104NDB2V2
G18	GND
H1	IO267PDB6V4
H2	VCCIB7
H3	IO283NPB7V1
H4	GFB1/IO274PPB7V0
H5	GND
H6	IO279NDB7V0
H7	VCC
H8	VCC
H9	GND
H10	GND
H11	VCC
H12	VCC
H13	IO98NDB2V2
H14	GND
H15	GCB1/IO113PDB2V3
H16	GCC1/IO112PPB2V3
H17	VCCIB2
H18	IO108PDB2V3

FG324	
Pin Number	A3PE3000 FBGA
J1	IO267NDB6V4
J2	GFA0/IO273NDB6V4
J3	VCOMPLF
J4	GFA2/IO272PDB6V4
J5	GFB0/IO274NPB7V0
J6	GFC0/IO275NDB7V0
J7	GFC1/IO275PDB7V0
J8	GND
J9	GND
J10	GND
J11	GND
J12	GCA2/IO115PDB3V0
J13	GCA1/IO114PDB3V0
J14	GCA0/IO114NDB3V0
J15	GCB0/IO113NDB2V3
J16	VCOMPLC
J17	IO120NPB3V0
J18	IO108NDB2V3
K1	IO263PDB6V3
K2	GFA1/IO273PDB6V4
K3	VCCPLF
K4	IO272NDB6V4
K5	GFC2/IO270PPB6V4
K6	GFB2/IO271PDB6V4
K7	IO271NDB6V4
K8	GND
K9	GND
K10	GND
K11	GND
K12	IO115NDB3V0
K13	GCB2/IO116PDB3V0
K14	IO116NDB3V0
K15	GCC2/IO117PDB3V0
K16	VCCPLC
K17	IO124NPB3V1
K18	IO120PPB3V0

FG324	
Pin Number	A3PE3000 FBGA
L1	IO263NDB6V3
L2	VCCIB6
L3	IO259PDB6V3
L4	IO259NDB6V3
L5	GND
L6	IO270NPB6V4
L7	VCC
L8	VCC
L9	GND
L10	GND
L11	VCC
L12	VCC
L13	IO132PDB3V2
L14	GND
L15	IO117NDB3V0
L16	IO128NPB3V1
L17	VCCIB3
L18	IO124PPB3V1
M1	GND
M2	IO255PDB6V2
M3	IO255NDB6V2
M4	IO251PPB6V2
M5	VCCIB6
M6	GEB0/IO235NDB6V0
M7	GEB1/IO235PDB6V0
M8	VCC
M9	IO192PPB4V4
M10	IO154NPB4V0
M11	VCC
M12	GDA0/IO153NPB3V4
M13	IO132NDB3V2
M14	VCCIB3
M15	IO134NDB3V2
M16	IO134PDB3V2
M17	IO128PPB3V1
M18	GND

FG484	
Pin Number	A3PE600 Function
N17	IO57NPB3V0
N18	IO55NPB3V0
N19	IO57PPB3V0
N20	NC
N21	IO56NDB3V0
N22	IO58PDB3V0
P1	NC
P2	IO111PDB6V1
P3	IO115NPB6V1
P4	IO113NPB6V1
P5	IO109PPB6V0
P6	IO108PDB6V0
P7	IO108NDB6V0
P8	VCCIB6
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB3
P16	GDB0/IO66NPB3V1
P17	IO60NDB3V1
P18	IO60PDB3V1
P19	IO61PDB3V1
P20	NC
P21	IO59PDB3V0
P22	IO58NDB3V0
R1	NC
R2	IO110PDB6V0
R3	VCC
R4	IO109NPB6V0
R5	IO106NDB6V0
R6	IO106PDB6V0
R7	GEC0/IO104NPB6V0
R8	VMV5

FG484	
Pin Number	A3PE600 Function
R9	VCCIB5
R10	VCCIB5
R11	IO84NDB5V0
R12	IO84PDB5V0
R13	VCCIB4
R14	VCCIB4
R15	VMV3
R16	VCCPLD
R17	GDB1/IO66PPB3V1
R18	GDC1/IO65PDB3V1
R19	IO61NDB3V1
R20	VCC
R21	IO59NDB3V0
R22	IO62PDB3V1
T1	NC
T2	IO110NDB6V0
T3	NC
T4	IO105PDB6V0
T5	IO105NDB6V0
T6	GEC1/IO104PPB6V0
T7	VCOMPLE
T8	GNDQ
T9	GEA2/IO101PPB5V2
T10	IO92NDB5V1
T11	IO90NDB5V1
T12	IO82NDB5V0
T13	IO74NDB4V1
T14	IO74PDB4V1
T15	GNDQ
T16	VCOMPLD
T17	VJTAG
T18	GDC0/IO65NDB3V1
T19	GDA1/IO67PDB3V1
T20	NC
T21	IO64PDB3V1
T22	IO62NDB3V1

FG484	
Pin Number	A3PE600 Function
U1	NC
U2	IO107PDB6V0
U3	IO107NDB6V0
U4	GEB1/IO103PDB6V0
U5	GEB0/IO103NDB6V0
U6	VMV6
U7	VCCPLE
U8	IO101NPB5V2
U9	IO95PPB5V1
U10	IO92PDB5V1
U11	IO90PDB5V1
U12	IO82PDB5V0
U13	IO76NDB4V1
U14	IO76PDB4V1
U15	VMV4
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO67NDB3V1
U20	NC
U21	IO64NDB3V1
U22	IO63PDB3V1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO102PDB6V0
V5	GEA0/IO102NDB6V0
V6	GNDQ
V7	GEC2/IO99PDB5V2
V8	IO95NPB5V1
V9	IO91NDB5V1
V10	IO91PDB5V1
V11	IO83NDB5V0
V12	IO83PDB5V0
V13	IO77NDB4V1
V14	IO77PDB4V1

FG484	
Pin Number	A3PE1500 Function
C21	NC
C22	VCCIB2
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0
D7	GAB0/IO01NDB0V0
D8	IO09PDB0V1
D9	IO13PDB0V1
D10	IO21PDB0V2
D11	IO31NDB0V3
D12	IO37NDB1V0
D13	IO37PDB1V0
D14	IO49NDB1V2
D15	IO49PDB1V2
D16	GBB1/IO56PDB1V3
D17	GBA0/IO57NDB1V3
D18	GBA1/IO57PDB1V3
D19	GND
D20	NC
D21	IO69PDB2V1
D22	NC
E1	NC
E2	IO218PPB7V3
E3	GND
E4	GAB2/IO220PDB7V3
E5	GAA2/IO221PDB7V3
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO09NDB0V1
E9	IO13NDB0V1
E10	IO21NDB0V2
E11	IO31PDB0V3
E12	IO35NDB1V0

FG484	
Pin Number	A3PE1500 Function
E13	IO41NDB1V1
E14	IO41PDB1V1
E15	GBC1/IO55PDB1V3
E16	GBB0/IO56NDB1V3
E17	GNDQ
E18	GBA2/IO58PDB2V0
E19	IO63NDB2V0
E20	GND
E21	IO69NDB2V1
E22	NC
F1	IO218NPB7V3
F2	IO216NDB7V3
F3	IO216PDB7V3
F4	IO220NDB7V3
F5	IO221NDB7V3
F6	VMV7
F7	VCCPLA
F8	GAC0/IO02NDB0V0
F9	GAC1/IO02PDB0V0
F10	IO23NDB0V2
F11	IO23PDB0V2
F12	IO35PDB1V0
F13	IO39NDB1V0
F14	IO45PDB1V1
F15	GBC0/IO55NDB1V3
F16	VCCPLB
F17	VMV2
F18	IO58NDB2V0
F19	IO63PDB2V0
F20	NC
F21	NC
F22	NC
G1	IO211NDB7V2
G2	IO211PDB7V2
G3	NC
G4	IO214PDB7V3

FG484	
Pin Number	A3PE1500 Function
G5	IO217PDB7V3
G6	GAC2/IO219PDB7V3
G7	VCOMPLA
G8	GNDQ
G9	IO19NDB0V2
G10	IO19PDB0V2
G11	IO25PDB0V3
G12	IO33PDB1V0
G13	IO39PDB1V0
G14	IO45NDB1V1
G15	GNDQ
G16	VCOMPLB
G17	GBB2/IO59PDB2V0
G18	IO62PDB2V0
G19	IO62NDB2V0
G20	IO71PDB2V2
G21	IO71NDB2V2
G22	NC
H1	IO209PSB7V2
H2	NC
H3	VCC
H4	IO214NDB7V3
H5	IO217NDB7V3
H6	IO219NDB7V3
H7	IO215PDB7V3
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO25NDB0V3
H12	IO33NDB1V0
H13	VCCIB1
H14	VCCIB1
H15	VMV1
H16	GBC2/IO60PDB2V0
H17	IO59NDB2V0
H18	IO67NDB2V1

FG896		FG896		FG896	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
AG9	IO225NPB5V3	AH15	IO195NDB5V0	AJ21	IO173PDB4V2
AG10	IO223NPB5V3	AH16	IO185NDB4V3	AJ22	IO163NDB4V1
AG11	IO221PDB5V3	AH17	IO185PDB4V3	AJ23	IO163PDB4V1
AG12	IO221NDB5V3	AH18	IO181PDB4V3	AJ24	IO167NPB4V1
AG13	IO205NPB5V1	AH19	IO177NDB4V2	AJ25	VCC
AG14	IO199NDB5V0	AH20	IO171NPB4V2	AJ26	IO156NPB4V0
AG15	IO199PDB5V0	AH21	IO165PPB4V1	AJ27	VCC
AG16	IO187NDB4V4	AH22	IO161PPB4V0	AJ28	TMS
AG17	IO187PDB4V4	AH23	IO157NDB4V0	AJ29	GND
AG18	IO181NDB4V3	AH24	IO157PDB4V0	AJ30	GND
AG19	IO171PPB4V2	AH25	IO155NDB4V0	AK2	GND
AG20	IO165NPB4V1	AH26	VCCIB4	AK3	GND
AG21	IO161NPB4V0	AH27	TDI	AK4	IO217PPB5V2
AG22	IO159NDB4V0	AH28	VCC	AK5	GND
AG23	IO159PDB4V0	AH29	VPUMP	AK6	IO215PPB5V2
AG24	IO158PPB4V0	AH30	GND	AK7	GND
AG25	GDB2/IO155PDB4V0	AJ1	GND	AK8	IO207NDB5V1
AG26	GDA2/IO154PPB4V0	AJ2	GND	AK9	IO207PDB5V1
AG27	GND	AJ3	GEA2/IO233PPB5V4	AK10	IO201NDB5V0
AG28	VJTAG	AJ4	VCC	AK11	IO201PDB5V0
AG29	VCC	AJ5	IO217NPB5V2	AK12	IO193NDB4V4
AG30	IO149NDB3V4	AJ6	VCC	AK13	IO193PDB4V4
AH1	GND	AJ7	IO215NPB5V2	AK14	IO197PDB5V0
AH2	IO233NPB5V4	AJ8	IO213NDB5V2	AK15	IO191NDB4V4
AH3	VCC	AJ9	IO213PDB5V2	AK16	IO191PDB4V4
AH4	GEB2/IO232PPB5V4	AJ10	IO209NDB5V1	AK17	IO189NDB4V4
AH5	VCCIB5	AJ11	IO209PDB5V1	AK18	IO189PDB4V4
AH6	IO219NDB5V3	AJ12	IO203NDB5V1	AK19	IO179PPB4V3
AH7	IO219PDB5V3	AJ13	IO203PDB5V1	AK20	IO175NDB4V2
AH8	IO227NDB5V4	AJ14	IO197NDB5V0	AK21	IO175PDB4V2
AH9	IO227PDB5V4	AJ15	IO195PDB5V0	AK22	IO169NDB4V1
AH10	IO225PPB5V3	AJ16	IO183NDB4V3	AK23	IO169PDB4V1
AH11	IO223PPB5V3	AJ17	IO183PDB4V3	AK24	GND
AH12	IO211NDB5V2	AJ18	IO179NPB4V3	AK25	IO167PPB4V1
AH13	IO211PDB5V2	AJ19	IO177PDB4V2	AK26	GND
AH14	IO205PPB5V1	AJ20	IO173NDB4V2	AK27	GDC2/IO156PPB4V0

FG896		FG896		FG896	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
M23	IO104PPB2V2	N29	IO107PDB2V3	R5	GFB0/IO274NPB7V0
M24	IO102PDB2V2	N30	IO107NDB2V3	R6	IO271NDB6V4
M25	IO102NDB2V2	P1	IO276NDB7V0	R7	GFB2/IO271PDB6V4
M26	IO95PDB2V1	P2	IO278NDB7V0	R8	IO269PDB6V4
M27	IO97NDB2V1	P3	IO280NDB7V0	R9	IO269NDB6V4
M28	IO101NDB2V2	P4	IO284NDB7V1	R10	VCCIB7
M29	IO103NDB2V2	P5	IO279NDB7V0	R11	VCC
M30	IO119PDB3V0	P6	GFC1/IO275PDB7V0	R12	GND
N1	IO276PDB7V0	P7	GFC0/IO275NDB7V0	R13	GND
N2	IO278PDB7V0	P8	IO277PDB7V0	R14	GND
N3	IO280PDB7V0	P9	IO277NDB7V0	R15	GND
N4	IO284PDB7V1	P10	VCCIB7	R16	GND
N5	IO279PDB7V0	P11	VCC	R17	GND
N6	IO285NDB7V1	P12	GND	R18	GND
N7	IO287NDB7V1	P13	GND	R19	GND
N8	IO281NDB7V0	P14	GND	R20	VCC
N9	IO281PDB7V0	P15	GND	R21	VCCIB2
N10	VCCIB7	P16	GND	R22	GCC0/IO112NDB2V3
N11	VCC	P17	GND	R23	GCB2/IO116PDB3V0
N12	GND	P18	GND	R24	IO118PDB3V0
N13	GND	P19	GND	R25	IO111PPB2V3
N14	GND	P20	VCC	R26	IO122PPB3V1
N15	GND	P21	VCCIB2	R27	GCA0/IO114NPB3V0
N16	GND	P22	GCC1/IO112PDB2V3	R28	VCOMPLC
N17	GND	P23	IO110PDB2V3	R29	GCB1/IO113PPB2V3
N18	GND	P24	IO110NDB2V3	R30	IO115NPB3V0
N19	GND	P25	IO109PPB2V3	T1	IO270NDB6V4
N20	VCC	P26	IO111NPB2V3	T2	VCCPLF
N21	VCCIB2	P27	IO105PDB2V2	T3	GFA2/IO272PPB6V4
N22	IO106NDB2V3	P28	IO105NDB2V2	T4	GFA1/IO273PDB6V4
N23	IO106PDB2V3	P29	GCC2/IO117PDB3V0	T5	IO272NPB6V4
N24	IO108PDB2V3	P30	IO117NDB3V0	T6	IO267NDB6V4
N25	IO108NDB2V3	R1	GFC2/IO270PDB6V4	T7	IO267PDB6V4
N26	IO95NDB2V1	R2	GFB1/IO274PPB7V0	T8	IO265PDB6V3
N27	IO99NDB2V2	R3	VCOMPLF	T9	IO263PDB6V3
N28	IO99PDB2V2	R4	GFA0/IO273NDB6V4	T10	VCCIB6

Revision	Changes	Page														
Revision 9 (Aug 2009) Product Brief v1.2	All references to speed grade –F have been removed from this document.	N/A														
DC and Switching Characteristics v1.3	The "Pro I/Os with Advanced I/O Standards" section was revised to add definitions of hot-swap and cold-sparing.	1-6														
	3.3 V LVCMOS and 1.2 V LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained 3.3 V LVCMOS and 1.2 V LVCMOS data.	N/A														
	IIL and IIH input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables.	N/A														
	–F was removed from the datasheet. The speed grade is no longer supported.	N/A														
	In the Table 2-2 • Recommended Operating Conditions ¹ "3.0 V DC supply voltage" and note 4 are new.	2-2														
	The Table 2-4 • Overshoot and Undershoot Limits ¹ table was updated.	2-3														
	The Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays table was updated.	2-5														
	There are new parameters and data was updated in the Table 2-99 • RAM4K9 table.	2-76														
	There are new parameters and data was updated in the Table 2-100 • RAM512X18 table.	2-77														
Revision 8 (Feb 2008) Product Brief v1.1	Table 1-2 • ProASIC3E FPGAs Package Sizes Dimensions is new.	1-II														
Revision 7 (Jun 2008) DC and Switching Characteristics v1.2	The title of Table 2-4 • Overshoot and Undershoot Limits ¹ was modified to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted.	2-3														
	Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels was updated.	2-50														
Revision 6 (Jun 2008)	The A3PE600 "FG484" table was missing G22. The pin and its function were added to the table.	4-27														
Revision 5 (Jun 2008) Packaging v1.4	The naming conventions changed for the following pins in the "FG484" for the A3PE600: <table><tr><th>Pin Number</th><th>New Function Name</th></tr><tr><td>J19</td><td>IO45PPB2V1</td></tr><tr><td>K20</td><td>IO45NPB2V1</td></tr><tr><td>M2</td><td>IO114NPB6V1</td></tr><tr><td>N1</td><td>IO114PPB6V1</td></tr><tr><td>N4</td><td>GFC2/IO115PPB6V1</td></tr><tr><td>P3</td><td>IO115NPB6V1</td></tr></table>	Pin Number	New Function Name	J19	IO45PPB2V1	K20	IO45NPB2V1	M2	IO114NPB6V1	N1	IO114PPB6V1	N4	GFC2/IO115PPB6V1	P3	IO115NPB6V1	4-22
Pin Number	New Function Name															
J19	IO45PPB2V1															
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N1	IO114PPB6V1															
N4	GFC2/IO115PPB6V1															
P3	IO115NPB6V1															
Revision 4 (Apr 2008) Product Brief v1.0	The product brief portion of the datasheet was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.	N/A														
Packaging v1.3	The "FG324" package diagram was replaced.	4-12														