# Microchip Technology - M1A3PE3000-2FGG484 Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 516096 |
| Number of I/O | 341 |
| Number of Gates | 3000000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m1a3pe3000-2fgg484 |

## SRAM and FIFO

ProASIC3E devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

## PLL and CCC

ProASIC3E devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC3E family contains six CCCs, each with an integrated PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

To maximize user I/Os, only the center east and west PLLs are available in devices using the PQ208 package. However, all six CCC blocks are still usable; the four corner CCCs allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range ($f_{IN\_CCC}$) = 1.5 MHz to 350 MHz
- Output frequency range ($f_{OUT\_CCC}$) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from –7.56 ns to +11.12 ns
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration.
- Output duty cycle = 50% ± 1.5% or better
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used
- Maximum acquisition time = 300 µs
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter— allowable input jitter is up to 1.5 ns
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × (350 MHz / $f_{OUT\_CCC}$)

## Global Clocking

ProASIC3E devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high fanout nets.

*Table 2-2 •* **Recommended Operating Conditions** [1]

| Symbol | Parameter | | Commercial | Industrial | Units |
|---|---|---|---|---|---|
| $T_A$ | Ambient temperature | | 0 to +70 | –40 to +85 | °C |
| $T_J$ | Junction temperature | | 0 to +85 | –40 to +100 | °C |
| VCC | 1.5 V DC core supply voltage | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| VJTAG | JTAG DC voltage | | 1.4 to 3.6 | 1.4 to 3.6 | V |
| VPUMP | Programming voltage | Programming Mode[2] | 3.15 to 3.45 | 3.15 to 3.45 | V |
| | | Operation[3] | 0 to 3.6 | 0 to 3.6 | V |
| VCCPLL | Analog power supply (PLL) | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| VCCI and VMV [4] | 1.5 V DC supply voltage | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | 1.8 V DC supply voltage | | 1.7 to 1.9 | 1.7 to 1.9 | V |
| | 2.5 V DC supply voltage | | 2.3 to 2.7 | 2.3 to 2.7 | V |
| | 3.3 V DC supply voltage | | 3.0 to 3.6 | 3.0 to 3.6 | V |
| | 3.0 V DC supply voltage[5] | | 2.7 to 3.6 | 2.7 to 3.6 | V |
| | LVDS/B-LVDS/M-LVDS differential I/O | | 2.375 to 2.625 | 2.375 to 2.625 | V |
| | LVPECL differential I/O | | 3.0 to 3.6 | 3.0 to 3.6 | V |

*Notes:*

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.*
3. *VPUMP can be left floating during normal operation (not programming mode).*
4. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-13 on page 2-16. VMV and VCCI should be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information.*
5. *To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microsemi recommends that the user follow best design practices using Microsemi's timing and power simulation tools.*
6. *3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.*

*Table 2-3 •* **Flash Programming Limits – Retention, Storage and Operating Temperature** [1]

| Product Grade | Programming Cycles | Program Retention (biased/unbiased) | Maximum Storage Temperature $T_{STG}$ (°C) [2] | Maximum Operating Junction Temperature $T_J$ (°C) [2] |
|---|---|---|---|---|
| Commercial | 500 | 20 years | 110 | 100 |
| Industrial | 500 | 20 years | 110 | 100 |

*Notes:*

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

## PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLXL exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-1 on page 2-4 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *ProASIC3E FPGA Fabric User's Guide* for information on clock and lock recovery.

## Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

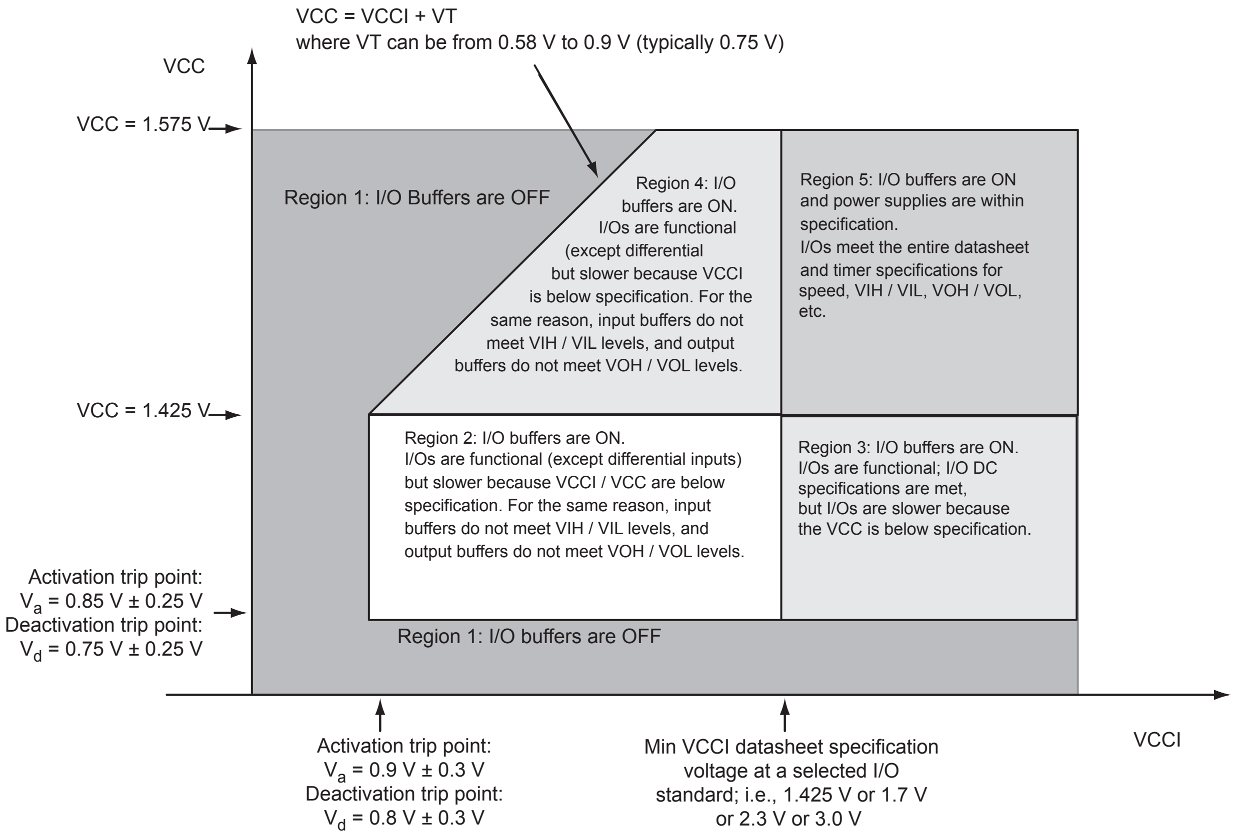


***Figure 2-1 •*** **I/O State as a Function of VCCI and VCC Voltage Levels**

***Table 2-21* • I/O Short Currents IOSH/IOSL**

| | Drive Strength | IOSH (mA)* | IOSL (mA)* |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 25 | 27 |
| | 4 mA | 25 | 27 |
| | 6 mA | 51 | 54 |
| | 8 mA | 51 | 54 |
| | 12 mA | 103 | 109 |
| | 16 mA | 132 | 127 |
| | 24 mA | 268 | 181 |
| 3.3 V LVCMOS Wide Range | 100 µA | Same as regular 3.3 V LVCMOS | Same as regular 3.3 V LVCMOS |
| 2.5 V LVCMOS | 4 mA | 16 | 18 |
| | 8 mA | 32 | 37 |
| | 12 mA | 65 | 74 |
| | 16 mA | 83 | 87 |
| | 24 mA | 169 | 124 |
| 1.8 V LVCMOS | 2 mA | 9 | 11 |
| | 4 mA | 17 | 22 |
| | 6 mA | 35 | 44 |
| | 8 mA | 45 | 51 |
| | 12 mA | 91 | 74 |
| | 16 mA | 91 | 74 |
| 1.5 V LVCMOS | 2 mA | 13 | 16 |
| | 4 mA | 25 | 33 |
| | 6 mA | 32 | 39 |
| | 8 mA | 66 | 55 |
| | 12 mA | 66 | 55 |

*Notes:*

1. *$T_J$ = 100°C*
2. *Applicable to 3.3 V LVCMOS Wide Range. IOSL/IOSH dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.*

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

***Table 2-22* • Duration of Short Circuit Event Before Failure**

| Temperature | Time before Failure |
|---|---|
| –40°C | > 20 years |
| 0°C | > 20 years |
| 25°C | > 20 years |
| 70°C | 5 years |

**Table 2-28 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 12 mA | Std. | 0.66 | 6.03 | 0.04 | 1.20 | 1.57 | 0.43 | 6.14 | 5.02 | 3.28 | 3.47 | 8.37 | 7.26 | ns |
| | –1 | 0.56 | 5.13 | 0.04 | 1.02 | 1.33 | 0.36 | 5.22 | 4.27 | 2.79 | 2.95 | 7.12 | 6.17 | ns |
| | –2 | 0.49 | 4.50 | 0.03 | 0.90 | 1.17 | 0.32 | 4.58 | 3.75 | 2.45 | 2.59 | 6.25 | 5.42 | ns |
| 16 mA | Std. | 0.66 | 5.62 | 0.04 | 1.20 | 1.57 | 0.43 | 5.72 | 4.72 | 3.32 | 3.58 | 7.96 | 6.96 | ns |
| | –1 | 0.56 | 4.78 | 0.04 | 1.02 | 1.33 | 0.36 | 4.87 | 4.02 | 2.83 | 3.04 | 6.77 | 5.92 | ns |
| | –2 | 0.49 | 4.20 | 0.03 | 0.90 | 1.17 | 0.32 | 4.27 | 3.53 | 2.48 | 2.67 | 5.94 | 5.20 | ns |
| 24 mA | Std. | 0.66 | 5.24 | 0.04 | 1.20 | 1.57 | 0.43 | 5.34 | 4.69 | 3.39 | 3.96 | 7.58 | 6.93 | ns |
| | –1 | 0.56 | 4.46 | 0.04 | 1.02 | 1.33 | 0.36 | 4.54 | 3.99 | 2.88 | 3.37 | 6.44 | 5.89 | ns |
| | –2 | 0.49 | 3.92 | 0.03 | 0.90 | 1.17 | 0.32 | 3.99 | 3.50 | 2.53 | 2.96 | 5.66 | 5.17 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

**Table 2-36 • 2.5 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 0.66 | 12.00 | 0.04 | 1.51 | 1.66 | 0.43 | 12.23 | 11.61 | 2.72 | 2.20 | 14.46 | 13.85 | ns |
| | –1 | 0.56 | 10.21 | 0.04 | 1.29 | 1.41 | 0.36 | 10.40 | 9.88 | 2.31 | 1.87 | 12.30 | 11.78 | ns |
| | –2 | 0.49 | 8.96 | 0.03 | 1.13 | 1.24 | 0.32 | 9.13 | 8.67 | 2.03 | 1.64 | 10.80 | 10.34 | ns |
| 8 mA | Std. | 0.66 | 8.73 | 0.04 | 1.51 | 1.66 | 0.43 | 8.89 | 8.01 | 3.10 | 2.93 | 11.13 | 10.25 | ns |
| | –1 | 0.56 | 7.43 | 0.04 | 1.29 | 1.41 | 0.36 | 7.57 | 6.82 | 2.64 | 2.49 | 9.47 | 8.72 | ns |
| | –2 | 0.49 | 6.52 | 0.03 | 1.13 | 1.24 | 0.32 | 6.64 | 5.98 | 2.32 | 2.19 | 8.31 | 7.65 | ns |
| 12 mA | Std. | 0.66 | 6.77 | 0.04 | 1.51 | 1.66 | 0.43 | 6.90 | 6.11 | 3.37 | 3.39 | 9.14 | 8.34 | ns |
| | –1 | 0.56 | 5.76 | 0.04 | 1.29 | 1.41 | 0.36 | 5.87 | 5.20 | 2.86 | 2.89 | 7.77 | 7.10 | ns |
| | –2 | 0.49 | 5.06 | 0.03 | 1.13 | 1.24 | 0.32 | 5.15 | 4.56 | 2.51 | 2.53 | 6.82 | 6.23 | ns |
| 16 mA | Std. | 0.66 | 6.31 | 0.04 | 1.51 | 1.66 | 0.43 | 6.42 | 5.73 | 3.42 | 3.52 | 8.66 | 7.96 | ns |
| | –1 | 0.56 | 5.37 | 0.04 | 1.29 | 1.41 | 0.36 | 5.46 | 4.87 | 2.91 | 3.00 | 7.37 | 6.77 | ns |
| | –2 | 0.49 | 4.71 | 0.03 | 1.13 | 1.24 | 0.32 | 4.80 | 4.28 | 2.56 | 2.63 | 6.47 | 5.95 | ns |
| 24 mA | Std. | 0.66 | 5.93 | 0.04 | 1.51 | 1.66 | 0.43 | 6.04 | 5.70 | 3.49 | 4.00 | 8.28 | 7.94 | ns |
| | –1 | 0.56 | 5.05 | 0.04 | 1.29 | 1.41 | 0.36 | 5.14 | 4.85 | 2.97 | 3.40 | 7.04 | 6.75 | ns |
| | –2 | 0.49 | 4.43 | 0.03 | 1.13 | 1.24 | 0.32 | 4.51 | 4.26 | 2.61 | 2.99 | 6.18 | 5.93 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

***Table 2-40* • 1.8 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 15.84 | 0.04 | 1.45 | 1.91 | 0.43 | 15.65 | 15.84 | 2.78 | 1.58 | 17.89 | 18.07 | ns |
| | –1 | 0.56 | 13.47 | 0.04 | 1.23 | 1.62 | 0.36 | 13.31 | 13.47 | 2.37 | 1.35 | 15.22 | 15.37 | ns |
| | –2 | 0.49 | 11.83 | 0.03 | 1.08 | 1.42 | 0.32 | 11.69 | 11.83 | 2.08 | 1.18 | 13.36 | 13.50 | ns |
| 4 mA | Std. | 0.66 | 11.39 | 0.04 | 1.45 | 1.91 | 0.43 | 11.60 | 10.76 | 3.26 | 2.77 | 13.84 | 12.99 | ns |
| | –1 | 0.56 | 9.69 | 0.04 | 1.23 | 1.62 | 0.36 | 9.87 | 9.15 | 2.77 | 2.36 | 11.77 | 11.05 | ns |
| | –2 | 0.49 | 8.51 | 0.03 | 1.08 | 1.42 | 0.32 | 8.66 | 8.03 | 2.43 | 2.07 | 10.33 | 9.70 | ns |
| 6 mA | Std. | 0.66 | 8.97 | 0.04 | 1.45 | 1.91 | 0.43 | 9.14 | 8.10 | 3.57 | 3.36 | 11.37 | 10.33 | ns |
| | –1 | 0.56 | 7.63 | 0.04 | 1.23 | 1.62 | 0.36 | 7.77 | 6.89 | 3.04 | 2.86 | 9.67 | 8.79 | ns |
| | –2 | 0.49 | 6.70 | 0.03 | 1.08 | 1.42 | 0.32 | 6.82 | 6.05 | 2.66 | 2.51 | 8.49 | 7.72 | ns |
| 8 mA | Std. | 0.66 | 8.35 | 0.04 | 1.45 | 1.91 | 0.43 | 8.50 | 7.59 | 3.64 | 3.52 | 10.74 | 9.82 | ns |
| | –1 | 0.56 | 7.10 | 0.04 | 1.23 | 1.62 | 0.36 | 7.23 | 6.45 | 3.10 | 3.00 | 9.14 | 8.35 | ns |
| | –2 | 0.49 | 6.24 | 0.03 | 1.08 | 1.42 | 0.32 | 6.35 | 5.66 | 2.72 | 2.63 | 8.02 | 7.33 | ns |
| 12 mA | Std. | 0.66 | 7.94 | 0.04 | 1.45 | 1.91 | 0.43 | 8.09 | 7.56 | 3.74 | 4.11 | 10.32 | 9.80 | ns |
| | –1 | 0.56 | 6.75 | 0.04 | 1.23 | 1.62 | 0.36 | 6.88 | 6.43 | 3.18 | 3.49 | 8.78 | 8.33 | ns |
| | –2 | 0.49 | 5.93 | 0.03 | 1.08 | 1.42 | 0.32 | 6.04 | 5.65 | 2.79 | 3.07 | 7.71 | 7.32 | ns |
| 16 mA | Std. | 0.66 | 7.94 | 0.04 | 1.45 | 1.91 | 0.43 | 8.09 | 7.56 | 3.74 | 4.11 | 10.32 | 9.80 | ns |
| | –1 | 0.56 | 6.75 | 0.04 | 1.23 | 1.62 | 0.36 | 6.88 | 6.43 | 3.18 | 3.49 | 8.78 | 8.33 | ns |
| | –2 | 0.49 | 5.93 | 0.03 | 1.08 | 1.42 | 0.32 | 6.04 | 5.65 | 2.79 | 3.07 | 7.71 | 7.32 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

## Voltage-Referenced I/O Characteristics

### 3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

***Table 2-48*** **• Minimum and Maximum DC Input and Output Levels**

| 3.3 V GTL | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL | IIH |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[1] | Max. mA[1] | µA[2] | µA[2] |
| 20 mA[3] | –0.3 | VREF – 0.05 | VREF + 0.05 | 3.6 | 0.4 | – | 20 | 20 | 181 | 268 | 10 | 10 |

*Notes:*

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

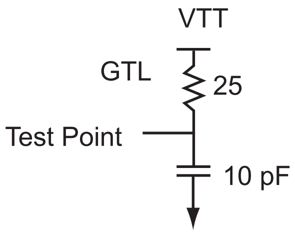


***Figure 2-12*** **• AC Loading**

***Table 2-49*** **• AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|---|
| VREF – 0.05 | VREF + 0.05 | 0.8 | 0.8 | 1.2 | 10 |

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

#### *Timing Characteristics*

***Table 2-50*** **• 3.3 V GTL**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V,**
**Worst-Case VCCI = 3.0 V VREF = 0.8 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.60 | 2.08 | 0.04 | 2.93 | 0.43 | 2.04 | 2.08 | | | 4.27 | 4.31 | ns |
| –1 | 0.51 | 1.77 | 0.04 | 2.50 | 0.36 | 1.73 | 1.77 | | | 3.63 | 3.67 | ns |
| –2 | 0.45 | 1.55 | 0.03 | 2.19 | 0.32 | 1.52 | 1.55 | | | 3.19 | 3.22 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

### Timing Characteristics

***Table 2-80* • LVDS**
**Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | Units |
|---|---|---|---|---|---|
| Std. | 0.66 | 1.87 | 0.04 | 1.82 | ns |
| –1 | 0.56 | 1.59 | 0.04 | 1.55 | ns |
| –2 | 0.49 | 1.40 | 0.03 | 1.36 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

## B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-23. The input and output buffer delays are available in the LVDS section in Table 2-80.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: $R_S = 60\ \Omega$ and $R_T = 70\ \Omega$, given $Z_0 = 50\ \Omega$ (2") and $Z_{stub} = 50\ \Omega$ (~1.5").

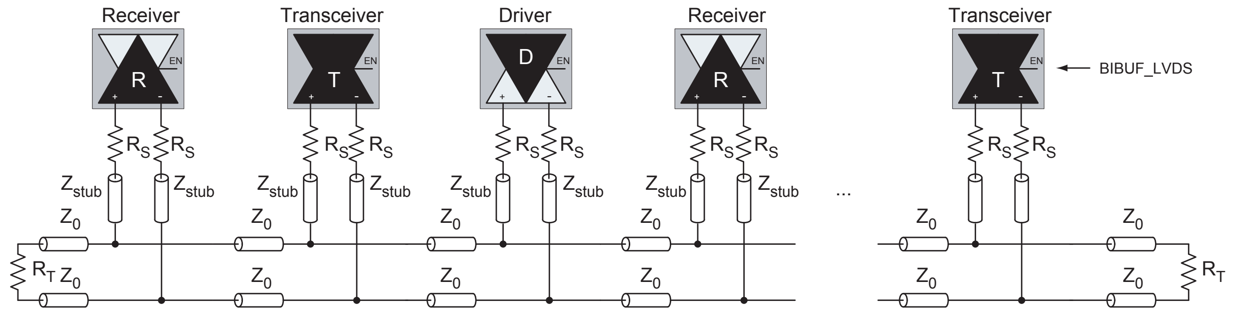


***Figure 2-23* • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers**

# Embedded SRAM and FIFO Characteristics

## SRAM

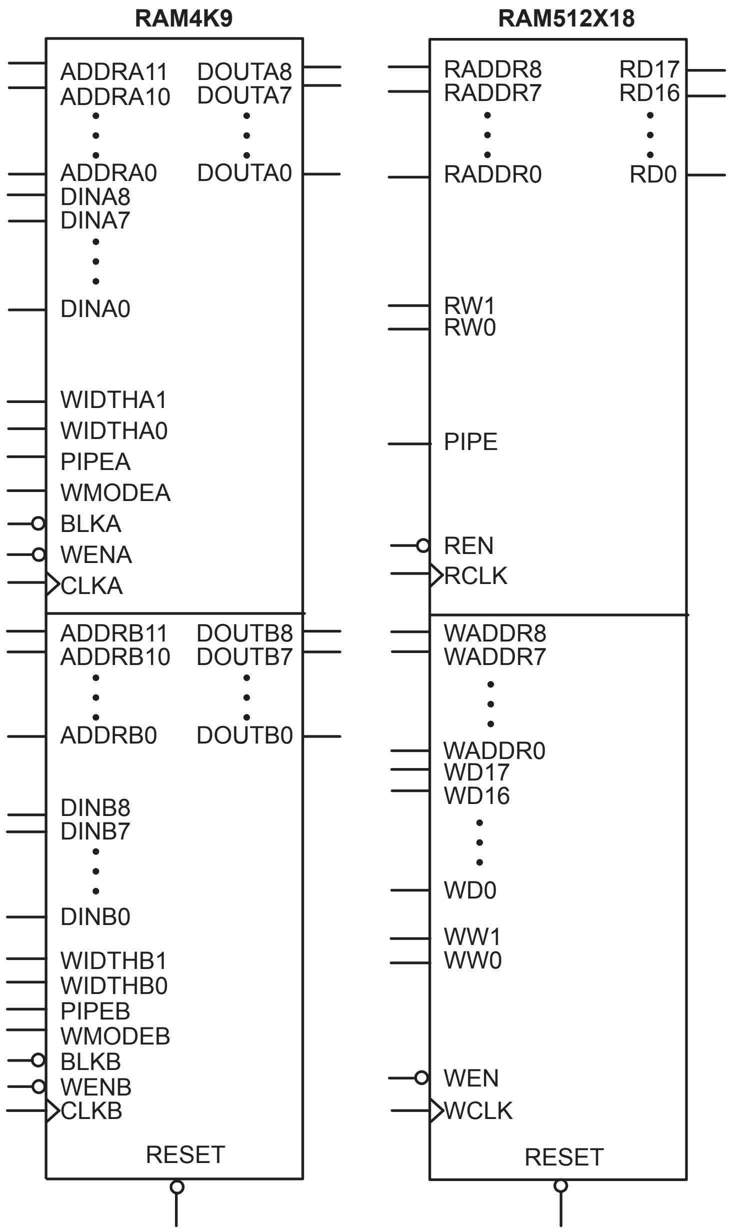


*Figure 2-40* • **RAM Models**

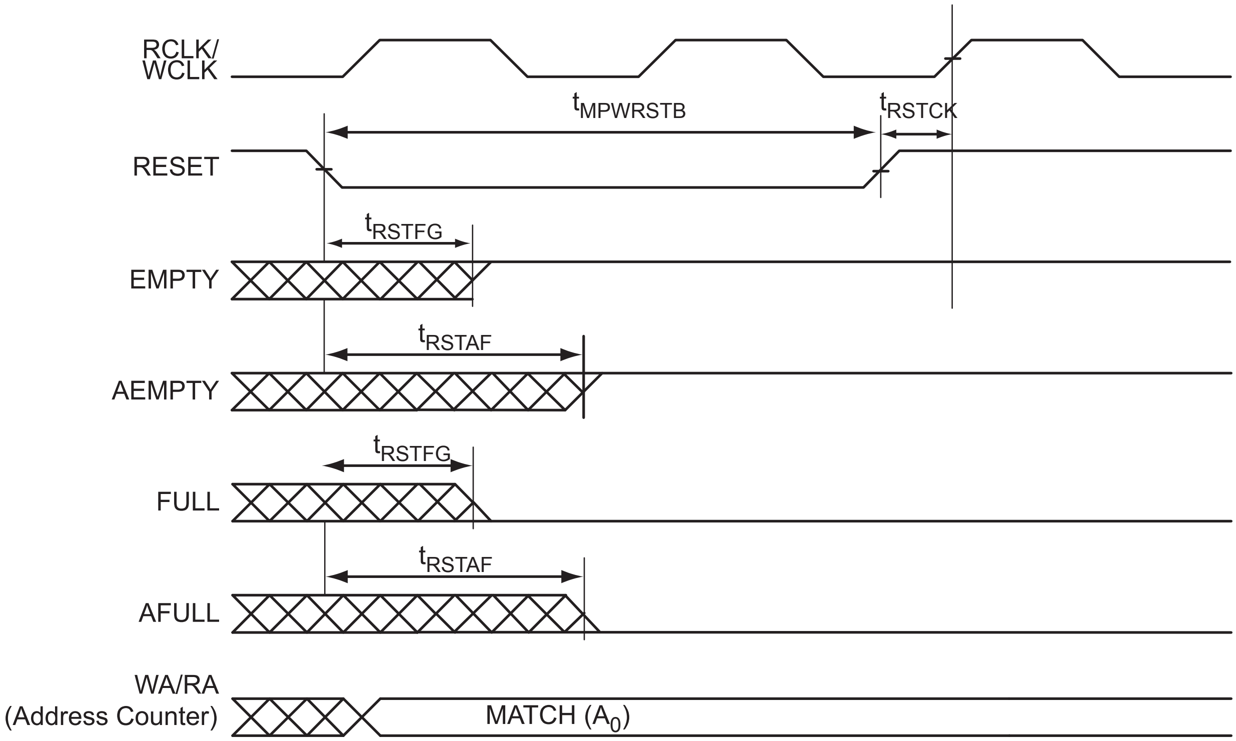


*Figure 2-49* **• FIFO Reset**

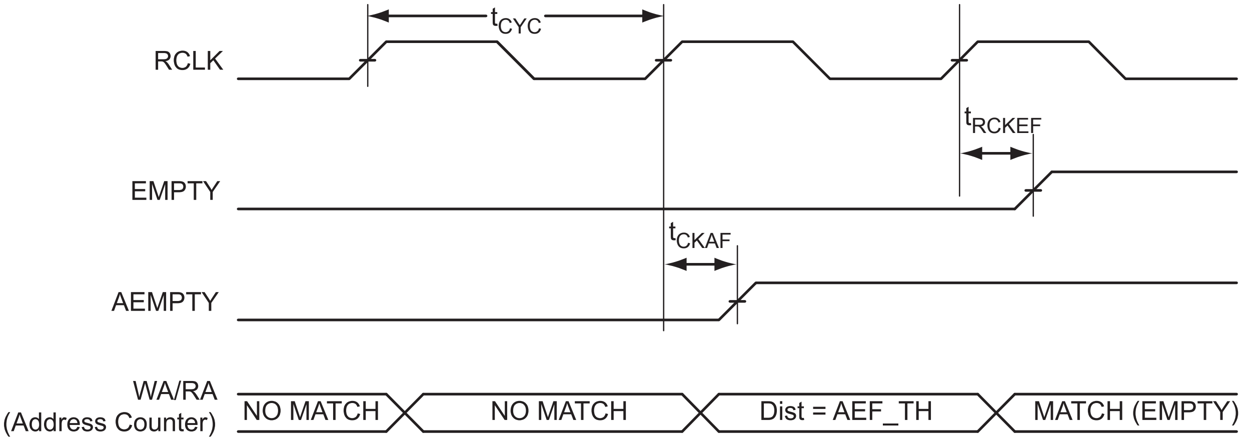


*Figure 2-50* **• FIFO EMPTY Flag and AEMPTY Flag Assertion**

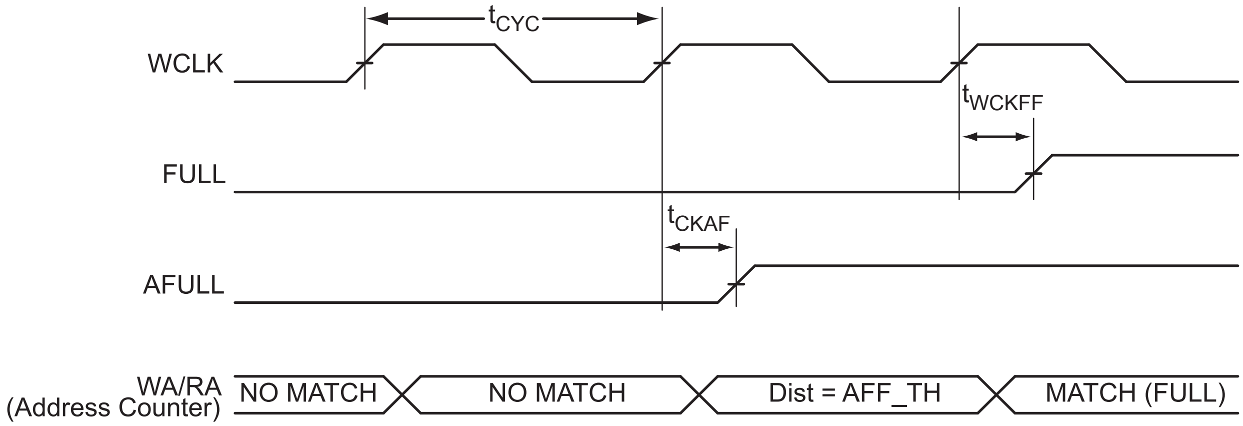


***Figure 2-51* • FIFO FULL Flag and AFULL Flag Assertion**

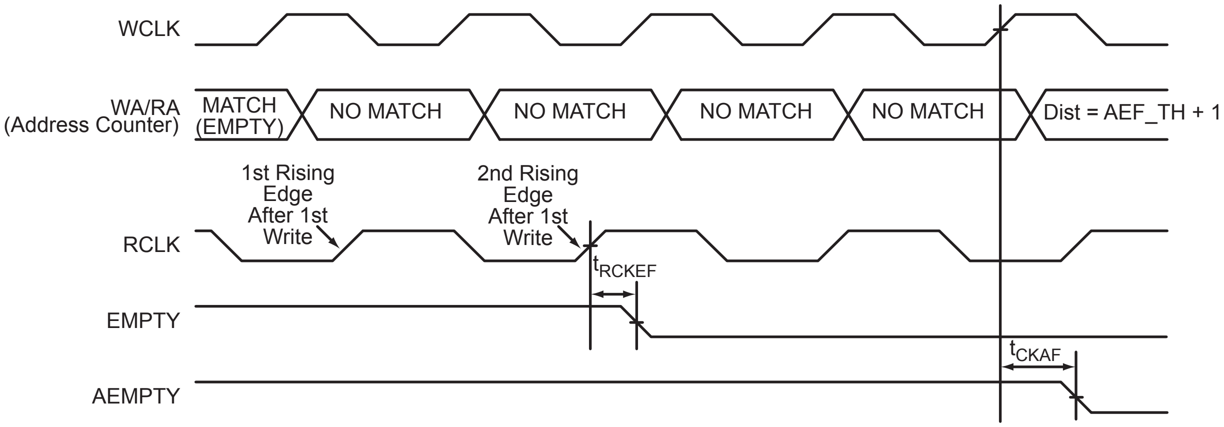


***Figure 2-52* • FIFO EMPTY Flag and AEMPTY Flag Deassertion**

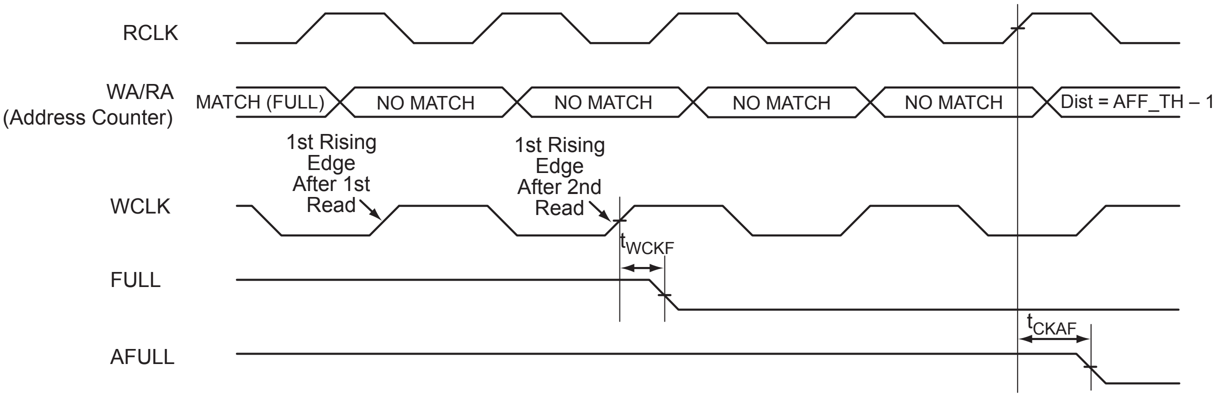


***Figure 2-53* • FIFO FULL Flag and AFULL Flag Deassertion**

# 3 – Pin Descriptions and Packaging

## Supply Pins

### GND Ground

Ground supply voltage to the core, I/O outputs, and I/O logic.

### GNDQ Ground (quiet)

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

### VCC Core Supply Voltage

Supply voltage to the FPGA core, nominally 1.5 V. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

### VCCIBx I/O Supply Voltage

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. In general, unused I/O banks should have their corresponding VCCIX pins tied to GND. If an output pad is terminated to ground through any resistor and if the corresponding VCCIX is left floating, then the leakage current to ground is ~ 0uA. However, if an output pad is terminated to ground through any resistor and the corresponding VCCIX grounded, then the leakage current to ground is ~ 3 uA. For unused banks the aforementioned behavior is to be taken into account while deciding if it's better to float VCCIX of unused bank or tie it to GND.

### VMVx I/O Supply Voltage (quiet)

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

### VCCPLA/B/C/D/E/F PLL Supply Voltage

Supply voltage to analog PLL, nominally 1.5 V.

When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *ProASIC3E FPGA Fabric User's Guide* for a complete board solution for the PLL analog power supply and ground.

There are six VCCPLX pins on ProASIC3E devices.

### VCOMPLA/B/C/D/E/F PLL Ground

Ground to analog PLL power supplies. When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There are six VCOMPL pins (PLL ground) on ProASIC3E devices.

### VJTAG JTAG Supply Voltage

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

### VPUMP Programming Supply Voltage

For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

## User-Defined Supply Pins

### VREF I/O Voltage Reference

Reference voltage for I/O minibanks. VREF pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, can be designated the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One VREF pin can support the number of I/Os available in its minibank.

## User Pins

### I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

### GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *ProASIC3E FPGA Fabric User's Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

# 4 – Package Pin Assignments

## PQ208

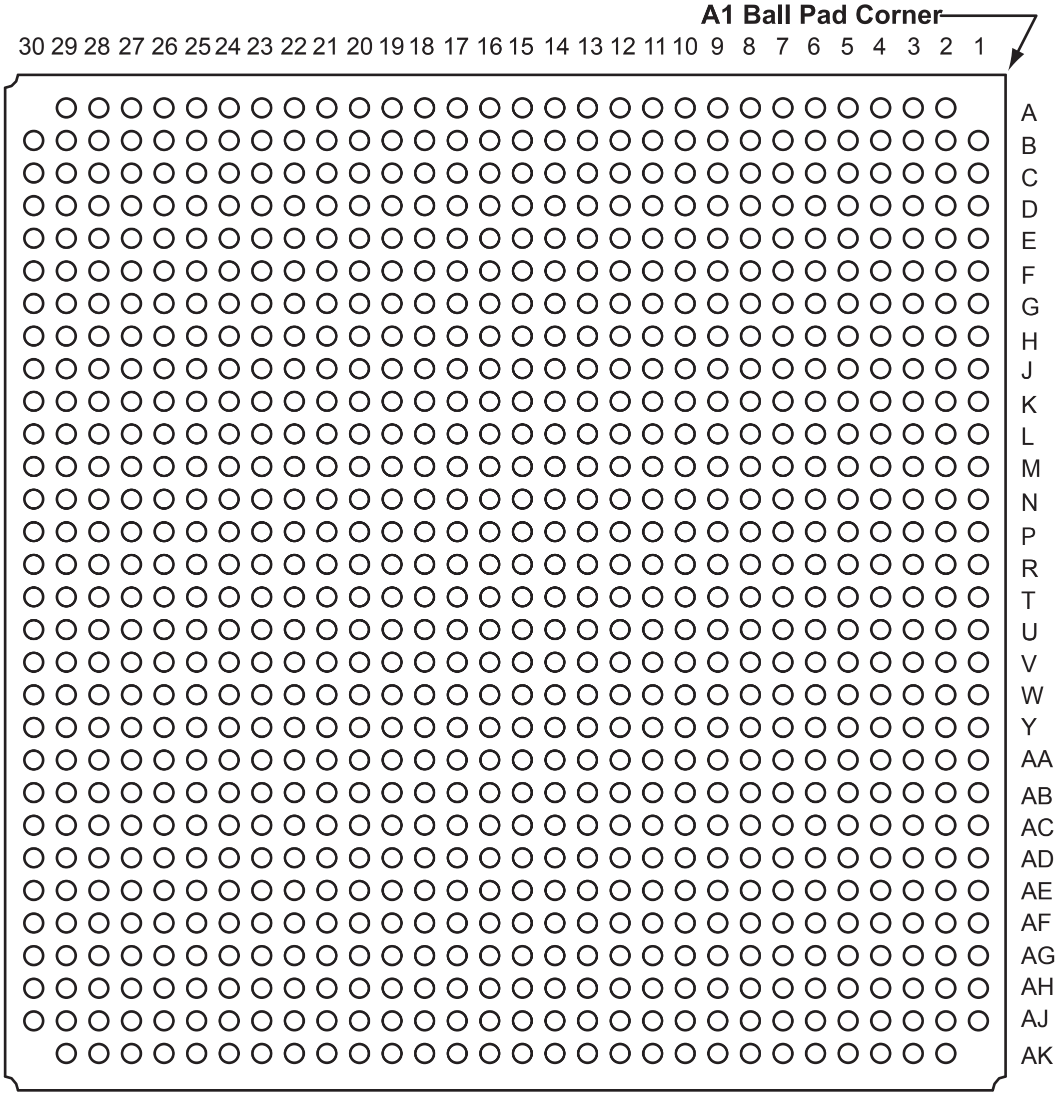
*Note: This is the top view of the package.*

### *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/products/fpga-soc/solutions*.

| FG676 | |
|---|---|
| **Pin Number** | **A3PE1500 Function** |
| G13 | IO21NDB0V2 |
| G14 | IO27PDB0V3 |
| G15 | IO35NDB1V0 |
| G16 | IO39PDB1V0 |
| G17 | IO51NDB1V2 |
| G18 | IO53NDB1V2 |
| G19 | VCCIB1 |
| G20 | GBA2/IO58PPB2V0 |
| G21 | GNDQ |
| G22 | IO64NDB2V1 |
| G23 | IO64PDB2V1 |
| G24 | IO72PDB2V2 |
| G25 | IO72NDB2V2 |
| G26 | IO78PDB2V2 |
| H1 | IO208NDB7V2 |
| H2 | IO208PDB7V2 |
| H3 | IO209NDB7V2 |
| H4 | IO209PDB7V2 |
| H5 | IO219NDB7V3 |
| H6 | GAC2/IO219PDB7V3 |
| H7 | VCCIB7 |
| H8 | VCC |
| H9 | VCCIB0 |
| H10 | VCCIB0 |
| H11 | VCCIB0 |
| H12 | VCCIB0 |
| H13 | VCCIB0 |
| H14 | VCCIB1 |
| H15 | VCCIB1 |
| H16 | VCCIB1 |
| H17 | VCCIB1 |
| H18 | VCCIB1 |
| H19 | VCC |
| H20 | VCC |
| H21 | IO58NPB2V0 |
| H22 | IO70PDB2V1 |
| H23 | IO69PDB2V1 |
| H24 | IO76PDB2V2 |
| H25 | IO76NDB2V2 |
| H26 | IO78NDB2V2 |
| J1 | IO197NDB7V0 |
| J2 | IO197PDB7V0 |
| J3 | VMV7 |
| J4 | IO215NDB7V3 |
| J5 | IO215PDB7V3 |
| J6 | IO214PDB7V3 |
| J7 | IO214NDB7V3 |
| J8 | VCCIB7 |
| J9 | VCC |
| J10 | VCC |
| J11 | VCC |
| J12 | VCC |
| J13 | VCC |
| J14 | VCC |
| J15 | VCC |
| J16 | VCC |
| J17 | VCC |
| J18 | VCC |
| J19 | VCCIB2 |
| J20 | IO62PDB2V0 |
| J21 | IO62NDB2V0 |
| J22 | IO70NDB2V1 |
| J23 | IO69NDB2V1 |
| J24 | VMV2 |
| J25 | IO80PDB2V3 |
| J26 | IO80NDB2V3 |
| K1 | IO195PDB7V0 |
| K2 | IO199NDB7V1 |
| K3 | IO199PDB7V1 |
| K4 | IO205NDB7V1 |
| K5 | IO205PDB7V1 |
| K6 | IO217PDB7V3 |
| K7 | IO217NDB7V3 |
| K8 | VCCIB7 |
| K9 | VCC |
| K10 | GND |
| K11 | GND |
| K12 | GND |
| K13 | GND |
| K14 | GND |
| K15 | GND |
| K16 | GND |
| K17 | GND |
| K18 | VCC |
| K19 | VCCIB2 |
| K20 | IO65PDB2V1 |
| K21 | IO65NDB2V1 |
| K22 | IO74PDB2V2 |
| K23 | IO74NDB2V2 |
| K24 | IO75PDB2V2 |
| K25 | IO75NDB2V2 |
| K26 | IO84PDB2V3 |
| L1 | IO195NDB7V0 |
| L2 | IO198PPB7V0 |
| L3 | GNDQ |
| L4 | IO201PDB7V1 |
| L5 | IO201NDB7V1 |
| L6 | IO210NDB7V2 |
| L7 | IO210PDB7V2 |
| L8 | VCCIB7 |
| L9 | VCC |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L13 | GND |
| L14 | GND |
| L15 | GND |
| L16 | GND |

# FG896



*Note: This is the bottom view of the package.*

## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/products/fpga-soc/solutions*.

| Revision | Changes | Page |
|---|---|---|
| v2.0<br>(continued) | Table 3-6 • Temperature and Voltage Derating Factors for Timing Delays was updated. | 3-5 |
| | Table 3-5 • Package Thermal Resistivities was updated. | 3-5 |
| | Table 3-10 • Different Components Contributing to the Dynamic Power Consumption in ProASIC3E Devices was updated. | 3-8 |
| | $t_{WRO}$ and $t_{CCKH}$ were added to Table 3-94 • RAM4K9 and Table 3-95 • RAM512X18. | 3-74 to 3-74 |
| | The note in Table 3-24 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was updated. | 3-23 |
| | Figure 3-43 • Write Access After Write onto Same Address, Figure 3-44 • Read Access After Write onto Same Address, and Figure 3-45 • Write Access After Read onto Same Address are new. | 3-71 to 3-73 |
| | Figure 3-53 • Timing Diagram was updated. | 3-80 |
| | Notes were added to the package diagrams identifying if they were top or bottom view. | N/A |
| | The A3PE1500 "208-Pin PQFP" table is new. | 4-4 |
| | The A3PE1500 "484-Pin FBGA" table is new. | 4-18 |
| | The A3PE1500 "A3PE1500 Function" table is new. | 4-24 |
| Advance v0.6<br>(January 2007) | In the "Packaging Tables" table, the number of I/Os for the A3PE1500 was changed for the FG484 and FG676 packages. | ii |
| Advance v0.5<br>(April 2006) | B-LVDS and M-LDVS are new I/O standards added to the datasheet. | N/A |
| | The term flow-through was changed to pass-through. | N/A |
| | Figure 2-8 • Very-Long-Line Resources was updated. | 2-8 |
| | The footnotes in Figure 2-27 • CCC/PLL Macro were updated. | 2-28 |
| | The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options. | 2-24 |
| | The "SRAM and FIFO" section was updated. | 2-21 |
| | The "RESET" section was updated. | 2-25 |
| | The "WCLK and RCLK" section was updated. | 2-25 |
| | The "RESET" section was updated. | 2-25 |
| | The "RESET" section was updated. | 2-27 |
| | B-LVDS and M-LDVS are new I/O standards added to the datasheet. | N/A |
| | The term flow-through was changed to pass-through. | N/A |
| | Figure 2-8 • Very-Long-Line Resources was updated. | 2-8 |
| | The footnotes in Figure 2-27 • CCC/PLL Macro were updated. | 2-28 |
| | The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options. | 2-24 |
| | The "SRAM and FIFO" section was updated. | 2-21 |
| | The "RESET" section was updated. | 2-25 |
| | The "WCLK and RCLK" section was updated. | 2-25 |

# Datasheet Categories

### *Categories*

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "ProASIC3E Device Status" table on page II, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

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The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

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This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

### *Preliminary*

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### *Production*

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