



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	516096
Number of I/O	620
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3pe3000-2fgg896i

Temperature Grade Offerings

Package	A3PE600	A3PE1500	A3PE3000
Cortex-M1 Devices		M1A3PE1500	M1A3PE3000
PQ208	C, I	C, I	C, I
FG256	C, I	–	–
FG324	–	–	C, I
FG484	C, I	C, I	C, I
FG676	–	C, I	–
FG896	–	–	C, I

Note: C = Commercial temperature range: 0°C to 70°C ambient temperature
 I = Industrial temperature range: –40°C to 85°C ambient temperature

Speed Grade and Temperature Grade Matrix

Temperature Grade	Std.	–1	–2
C ¹	✓	✓	✓
I ²	✓	✓	✓

Notes:

1. C = Commercial temperature range: 0°C to 70°C ambient temperature
2. I = Industrial temperature range: –40°C to 85°C ambient temperature

References made to ProASIC3E devices also apply to ARM-enabled ProASIC3E devices. The ARM-enabled part numbers start with M1 (Cortex-M1).

Contact your local Microsemi SoC Products Group representative for device availability:
www.microsemi.com/index.php?option=com_content&id=135&lang=en&view=article.

VersaTiles

The ProASIC3E core consists of VersaTiles, which have been enhanced beyond the ProASIC^{PLUS}® core tiles. The ProASIC3E VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to [Figure 1-2](#) for VersaTile configurations.

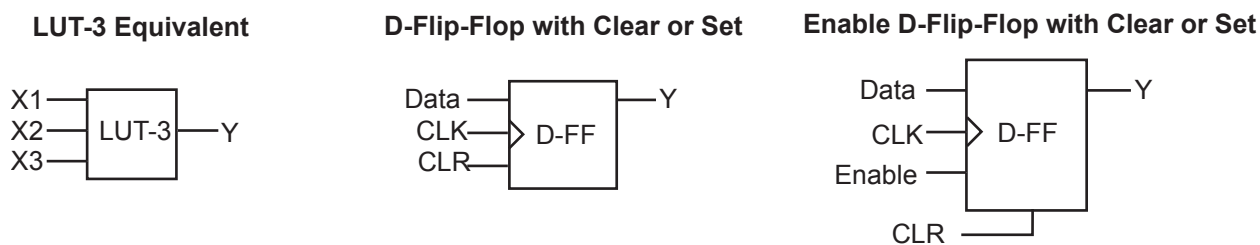


Figure 1-2 • VersaTile Configurations

User Nonvolatile FlashROM

ProASIC3E devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3E IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC3E development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

Table 2-4 • Overshoot and Undershoot Limits¹

VCCI and VMV	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle ²	Maximum Overshoot/Undershoot ²
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. Based on reliability requirements at 85°C.
2. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.
3. This table does not provide PCI overshoot/undershoot limits.

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC[®]3E device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in [Figure 2-1 on page 2-4](#).

There are five regions to consider during power-up.

ProASIC3E I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points ([Figure 2-1 on page 2-4](#)).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:

Ramping up: 0.6 V < trip_point_up < 1.2 V

Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC Trip Point:

Ramping up: 0.6 V < trip_point_up < 1.1 V

Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

Table 2-17 • Summary of I/O Timing Characteristics—Software Default Settings
–2 Speed Grade, Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = 3.0\text{ V}$

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option) ¹	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)
3.3 V LVTTTL / 3.3 V LVCMOS	12	12	High	35	–	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81
3.3 V LVCMOS Wide Range ²	100 μA	12	High	35	–	0.49	4.24	0.03	1.36	1.78	0.32	4.24	3.25	3.78	4.17	6.77	5.79
2.5 V LVCMOS	12	12	High	35	–	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28
1.8 V LVCMOS	12	12	High	35	–	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98
1.5 V LVCMOS	12	12	High	35	–	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37
3.3 V PCI	Per PCI spec	–	High	10	25 ³	0.49	2.09	0.03	0.78	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 ³	0.49	2.09	0.03	0.78	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16
3.3 V GTL	20 ⁴	–	High	10	25	0.45	1.55	0.03	2.19	–	0.32	1.52	1.55	–	–	3.19	3.22
2.5 V GTL	20 ⁴	–	High	10	25	0.45	1.59	0.03	1.83	–	0.32	1.61	1.59	–	–	3.28	3.26
3.3 V GTL+	35	–	High	10	25	0.45	1.53	0.03	1.19	–	0.32	1.56	1.53	–	–	3.23	3.20
2.5 V GTL+	33	–	High	10	25	0.45	1.65	0.03	1.13	–	0.32	1.68	1.57	–	–	3.35	3.24
HSTL (I)	8	–	High	20	50	0.49	2.37	0.03	1.59	–	0.32	2.42	2.35	–	–	4.09	4.02
HSTL (II)	15 ⁴	–	High	20	25	0.49	2.26	0.03	1.59	–	0.32	2.30	2.03	–	–	3.97	3.70
SSTL2 (I)	15	–	High	30	50	0.49	1.59	0.03	1.00	–	0.32	1.62	1.38	–	–	3.29	3.05
SSTL2 (II)	18	–	High	30	25	0.49	1.62	0.03	1.00	–	0.32	1.65	1.32	–	–	3.32	2.99
SSTL3 (I)	14	–	High	30	50	0.49	1.72	0.03	0.93	–	0.32	1.75	1.37	–	–	3.42	3.04
SSTL3 (II)	21	–	High	30	25	0.49	1.54	0.03	0.93	–	0.32	1.57	1.25	–	–	3.24	2.92
LVDS/B-LVDS/M-LVDS	24	–	High	–	–	0.49	1.40	0.03	1.36	–	–	–	–	–	–	–	–
LVPECL	24	–	High	–	–	0.49	1.36	0.03	1.22	–	–	–	–	–	–	–	–

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3V wide range as specified in the JESD8b specification.
3. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-11 on page 2-38](#) for connectivity. This resistor is not required during normal operation.
4. Output drive strength is below JEDEC specification.
5. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#).

Table 2-19 • I/O Output Buffer Maximum Resistances¹ (continued)

Standard	Drive Strength	R _{PULL-DOWN} (Ω) ²	R _{PULL-UP} (Ω) ³
3.3 V GTL+	35 mA	12	–
2.5 V GTL+	33 mA	15	–
HSTL (I)	8 mA	50	50
HSTL (II)	15 mA ⁴	25	25
SSTL2 (I)	15 mA	27	31
SSTL2 (II)	18 mA	13	15
SSTL3 (I)	14 mA	44	69
SSTL3 (II)	21 mA	18	32

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website at www.microsemi.com/index.php?option=com_content&id=1671&lang=en&view=article.
2. $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / IOL_{spec}$
3. $R_{(PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / IOH_{spec}$
4. Output drive strength is below JEDEC specification.

Table 2-20 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

VCCI	R _(WEAK PULL-UP) ¹ (Ω)		R _(WEAK PULL-DOWN) ² (Ω)	
	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
3.3 V (Wide Range I/Os)	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / I_{(WEAK PULL-UP-MIN)}$
2. $R_{(WEAK PULL-DOWN-MAX)} = (VOL_{spec}) / I_{(WEAK PULL-DOWN-MIN)}$

Table 2-22 • Duration of Short Circuit Event Before Failure (continued)

Temperature	Time before Failure
85°C	2 years
100°C	6 months

**Table 2-23 • Schmitt Trigger Input Hysteresis
Hysteresis Voltage Value (typ.) for Schmitt Mode Input Buffers**

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

Table 2-24 • I/O Input Rise Time, Fall Time, and Related I/O Reliability*

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns *	20 years (110°C)
LVTTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis.	20 years (110°C)
HSTL/SSTL/GTL	No requirement	10 ns *	10 years (100°C)
LVDS/B-LVDS/M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

Note: *For clock signals and similar edge-generating signals, refer to the "ProASIC3/E SSO and Pin Placement Guidelines" chapter of the [ProASIC3E FPGA Fabric User's Guide](#). The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

Voltage-Referenced I/O Characteristics

3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-48 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
20 mA ³	−0.3	VREF − 0.05	VREF + 0.05	3.6	0.4	−	20	20	181	268	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Output drive strength is below JEDEC specification.

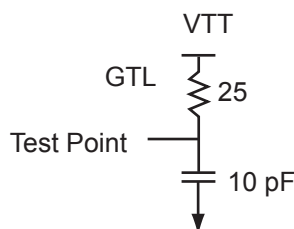


Figure 2-12 • AC Loading

Table 2-49 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF − 0.05	VREF + 0.05	0.8	0.8	1.2	10

Note: *Measuring point = V_{trip}. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-50 • 3.3 V GTL

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V VREF = 0.8 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.60	2.08	0.04	2.93	0.43	2.04	2.08			4.27	4.31	ns
−1	0.51	1.77	0.04	2.50	0.36	1.73	1.77			3.63	3.67	ns
−2	0.45	1.55	0.03	2.19	0.32	1.52	1.55			3.19	3.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-63 • Minimum and Maximum DC Input and Output Levels

HSTL Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
15 mA ³	−0.3	VREF − 0.1	VREF + 0.1	3.6	0.4	VCCI − 0.4	15	15	55	66	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Output drive strength is below JEDEC specification.

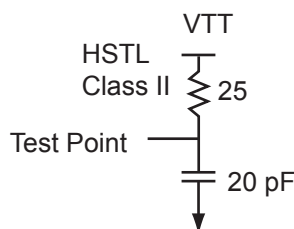


Figure 2-17 • AC Loading

Table 2-64 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF − 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: *Measuring point = Vtrip. See [Table 2-15 on page 2-18](#) for a complete table of trip points.

Timing Characteristics

Table 2-65 • HSTL Class II

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 1.4 V, VREF = 0.75 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.66	3.02	0.04	2.12	0.43	3.08	2.71			5.32	4.95	ns
−1	0.56	2.57	0.04	1.81	0.36	2.62	2.31			4.52	4.21	ns
−2	0.49	2.26	0.03	1.59	0.32	2.30	2.03			3.97	3.70	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL ¹	Output Lower Current	0.65	0.91	1.16	mA
IOH ¹	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
IIH ²	Input High Leakage Current			10	μA
IIL ²	Input Low Leakage Current			10	μA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage ²	100	350		mV

Notes:

1. IOL/IOH defined by VODIFF/(Resistor Network).
2. Currents are measured at 85°C junction temperature.

Table 2-79 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)
1.075	1.325	Cross point	–

Note: *Measuring point = Vtrip. See [Table 2-15 on page 2-18](#) for a complete table of trip points.

DDR Module Specifications

Input DDR Module

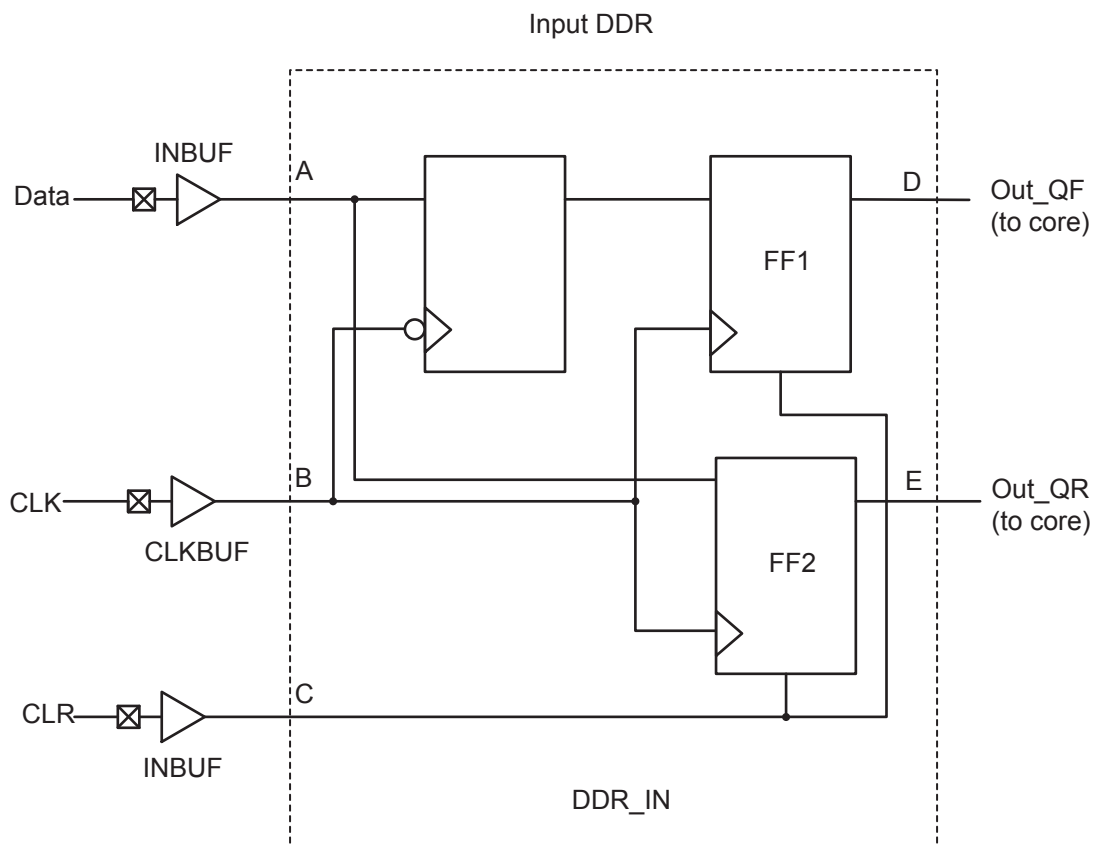


Figure 2-30 • Input DDR Timing Model

Table 2-89 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

VJTAG

JTAG Supply Voltage

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

VPUMP

Programming Supply Voltage

For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 μ F and 0.33 μ F capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

User-Defined Supply Pins

VREF

I/O Voltage Reference

Reference voltage for I/O minibanks. VREF pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, can be designated the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One VREF pin can support the number of I/Os available in its minibank.

User Pins

I/O

User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

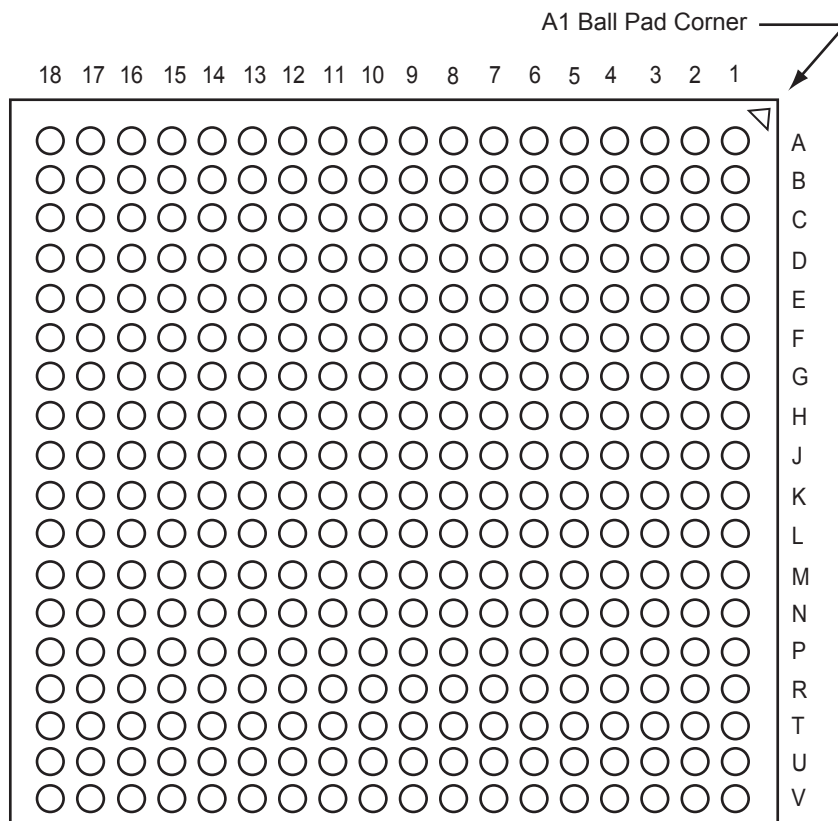
GL

Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *ProASIC3E FPGA Fabric User's Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

FG324

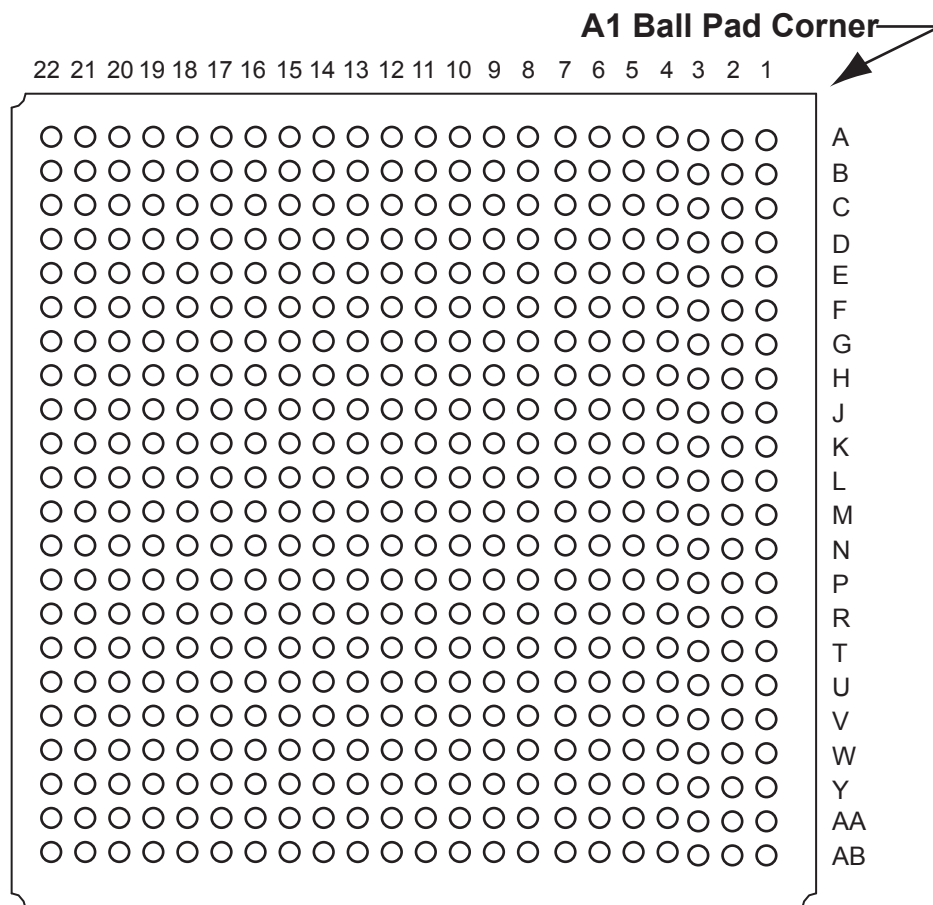


Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/products/fpga-soc/solutions>.

FG484



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/products/fpga-soc/solutions>.

FG484	
Pin Number	A3PE600 Function
N17	IO57NPB3V0
N18	IO55NPB3V0
N19	IO57PPB3V0
N20	NC
N21	IO56NDB3V0
N22	IO58PDB3V0
P1	NC
P2	IO111PDB6V1
P3	IO115NPB6V1
P4	IO113NPB6V1
P5	IO109PPB6V0
P6	IO108PDB6V0
P7	IO108NDB6V0
P8	VCCIB6
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB3
P16	GDB0/IO66NPB3V1
P17	IO60NDB3V1
P18	IO60PDB3V1
P19	IO61PDB3V1
P20	NC
P21	IO59PDB3V0
P22	IO58NDB3V0
R1	NC
R2	IO110PDB6V0
R3	VCC
R4	IO109NPB6V0
R5	IO106NDB6V0
R6	IO106PDB6V0
R7	GEC0/IO104NPB6V0
R8	VMV5

FG484	
Pin Number	A3PE600 Function
R9	VCCIB5
R10	VCCIB5
R11	IO84NDB5V0
R12	IO84PDB5V0
R13	VCCIB4
R14	VCCIB4
R15	VMV3
R16	VCCPLD
R17	GDB1/IO66PPB3V1
R18	GDC1/IO65PDB3V1
R19	IO61NDB3V1
R20	VCC
R21	IO59NDB3V0
R22	IO62PDB3V1
T1	NC
T2	IO110NDB6V0
T3	NC
T4	IO105PDB6V0
T5	IO105NDB6V0
T6	GEC1/IO104PPB6V0
T7	VCOMPLE
T8	GNDQ
T9	GEA2/IO101PPB5V2
T10	IO92NDB5V1
T11	IO90NDB5V1
T12	IO82NDB5V0
T13	IO74NDB4V1
T14	IO74PDB4V1
T15	GNDQ
T16	VCOMPLD
T17	VJTAG
T18	GDC0/IO65NDB3V1
T19	GDA1/IO67PDB3V1
T20	NC
T21	IO64PDB3V1
T22	IO62NDB3V1

FG484	
Pin Number	A3PE600 Function
U1	NC
U2	IO107PDB6V0
U3	IO107NDB6V0
U4	GEB1/IO103PDB6V0
U5	GEB0/IO103NDB6V0
U6	VMV6
U7	VCCPLE
U8	IO101NPB5V2
U9	IO95PPB5V1
U10	IO92PDB5V1
U11	IO90PDB5V1
U12	IO82PDB5V0
U13	IO76NDB4V1
U14	IO76PDB4V1
U15	VMV4
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO67NDB3V1
U20	NC
U21	IO64NDB3V1
U22	IO63PDB3V1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO102PDB6V0
V5	GEA0/IO102NDB6V0
V6	GNDQ
V7	GEC2/IO99PDB5V2
V8	IO95NPB5V1
V9	IO91NDB5V1
V10	IO91PDB5V1
V11	IO83NDB5V0
V12	IO83PDB5V0
V13	IO77NDB4V1
V14	IO77PDB4V1

FG484	
Pin Number	A3PE1500 Function
N17	IO91NPB3V0
N18	IO90NPB3V0
N19	IO91PPB3V0
N20	GNDQ
N21	IO93NDB3V0
N22	IO95PDB3V1
P1	NC
P2	IO183PDB6V2
P3	IO187NPB6V2
P4	IO184NPB6V2
P5	IO176PPB6V1
P6	IO182PDB6V1
P7	IO182NDB6V1
P8	VCCIB6
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB3
P16	GDB0/IO109NPB3V2
P17	IO97NDB3V1
P18	IO97PDB3V1
P19	IO99PDB3V1
P20	VMV3
P21	IO98PDB3V1
P22	IO95NDB3V1
R1	NC
R2	IO177PDB6V1
R3	VCC
R4	IO176NPB6V1
R5	IO174NDB6V0
R6	IO174PDB6V0
R7	GEC0/IO169NPB6V0
R8	VMV5

FG484	
Pin Number	A3PE1500 Function
R9	VCCIB5
R10	VCCIB5
R11	IO135NDB5V0
R12	IO135PDB5V0
R13	VCCIB4
R14	VCCIB4
R15	VMV3
R16	VCCPLD
R17	GDB1/IO109PPB3V2
R18	GDC1/IO108PDB3V2
R19	IO99NDB3V1
R20	VCC
R21	IO98NDB3V1
R22	IO101PDB3V1
T1	NC
T2	IO177NDB6V1
T3	NC
T4	IO171PDB6V0
T5	IO171NDB6V0
T6	GEC1/IO169PPB6V0
T7	VCOMPLE
T8	GNDQ
T9	GEA2/IO166PPB5V3
T10	IO145NDB5V1
T11	IO141NDB5V0
T12	IO139NDB5V0
T13	IO119NDB4V1
T14	IO119PDB4V1
T15	GNDQ
T16	VCOMPLD
T17	VJTAG
T18	GDC0/IO108NDB3V2
T19	GDA1/IO110PDB3V2
T20	NC
T21	IO103PDB3V2
T22	IO101NDB3V1

FG484	
Pin Number	A3PE1500 Function
U1	IO175PPB6V1
U2	IO173PDB6V0
U3	IO173NDB6V0
U4	GEB1/IO168PDB6V0
U5	GEB0/IO168NDB6V0
U6	VMV6
U7	VCCPLE
U8	IO166NPB5V3
U9	IO157PPB5V2
U10	IO145PDB5V1
U11	IO141PDB5V0
U12	IO139PDB5V0
U13	IO121NDB4V1
U14	IO121PDB4V1
U15	VMV4
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO110NDB3V2
U20	NC
U21	IO103NDB3V2
U22	IO105PDB3V2
V1	NC
V2	IO175NPB6V1
V3	GND
V4	GEA1/IO167PDB6V0
V5	GEA0/IO167NDB6V0
V6	GNDQ
V7	GEC2/IO164PDB5V3
V8	IO157NPB5V2
V9	IO151NDB5V2
V10	IO151PDB5V2
V11	IO137NDB5V0
V12	IO137PDB5V0
V13	IO123NDB4V1
V14	IO123PDB4V1

FG676	
Pin Number	A3PE1500 Function
L17	GND
L18	VCC
L19	VCCIB2
L20	IO67PDB2V1
L21	IO67NDB2V1
L22	IO71PDB2V2
L23	IO71NDB2V2
L24	GNDQ
L25	IO82PDB2V3
L26	IO84NDB2V3
M1	IO198NPB7V0
M2	IO202PDB7V1
M3	IO202NDB7V1
M4	IO206NDB7V1
M5	IO206PDB7V1
M6	IO204NDB7V1
M7	IO204PDB7V1
M8	VCCIB7
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	GND
M15	GND
M16	GND
M17	GND
M18	VCC
M19	VCCIB2
M20	IO73NDB2V2
M21	IO73PDB2V2
M22	IO81PPB2V3
M23	IO77PDB2V2
M24	IO77NDB2V2
M25	IO82NDB2V3
M26	IO83PDB2V3

FG676	
Pin Number	A3PE1500 Function
N1	GFB0/IO191NPB7V0
N2	VCOMPLF
N3	GFB1/IO191PPB7V0
N4	IO196PDB7V0
N5	GFA0/IO190NDB6V2
N6	IO200PDB7V1
N7	IO200NDB7V1
N8	VCCIB7
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	GND
N15	GND
N16	GND
N17	GND
N18	VCC
N19	VCCIB2
N20	IO79PDB2V3
N21	IO79NDB2V3
N22	GCA2/IO88PPB3V0
N23	IO81NPB2V3
N24	GCA0/IO87NDB3V0
N25	GCB0/IO86NPB2V3
N26	IO83NDB2V3
P1	GFA2/IO189PDB6V2
P2	VCCPLF
P3	IO193PPB7V0
P4	IO196NDB7V0
P5	GFA1/IO190PDB6V2
P6	IO194PDB7V0
P7	IO194NDB7V0
P8	VCCIB6
P9	VCC
P10	GND

FG676	
Pin Number	A3PE1500 Function
P11	GND
P12	GND
P13	GND
P14	GND
P15	GND
P16	GND
P17	GND
P18	VCC
P19	VCCIB3
P20	GCC0/IO85NDB2V3
P21	GCC1/IO85PDB2V3
P22	GCB1/IO86PPB2V3
P23	IO88NPB3V0
P24	GCA1/IO87PDB3V0
P25	VCCPLC
P26	VCOMPLC
R1	IO189NDB6V2
R2	IO185PDB6V2
R3	IO187NPB6V2
R4	IO193NPB7V0
R5	GFC2/IO187PPB6V2
R6	GFC1/IO192PDB7V0
R7	GFC0/IO192NDB7V0
R8	VCCIB6
R9	VCC
R10	GND
R11	GND
R12	GND
R13	GND
R14	GND
R15	GND
R16	GND
R17	GND
R18	VCC
R19	VCCIB3
R20	NC

FG896		FG896		FG896	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
AG9	IO225NPB5V3	AH15	IO195NDB5V0	AJ21	IO173PDB4V2
AG10	IO223NPB5V3	AH16	IO185NDB4V3	AJ22	IO163NDB4V1
AG11	IO221PDB5V3	AH17	IO185PDB4V3	AJ23	IO163PDB4V1
AG12	IO221NDB5V3	AH18	IO181PDB4V3	AJ24	IO167NPB4V1
AG13	IO205NPB5V1	AH19	IO177NDB4V2	AJ25	VCC
AG14	IO199NDB5V0	AH20	IO171NPB4V2	AJ26	IO156NPB4V0
AG15	IO199PDB5V0	AH21	IO165PPB4V1	AJ27	VCC
AG16	IO187NDB4V4	AH22	IO161PPB4V0	AJ28	TMS
AG17	IO187PDB4V4	AH23	IO157NDB4V0	AJ29	GND
AG18	IO181NDB4V3	AH24	IO157PDB4V0	AJ30	GND
AG19	IO171PPB4V2	AH25	IO155NDB4V0	AK2	GND
AG20	IO165NPB4V1	AH26	VCCIB4	AK3	GND
AG21	IO161NPB4V0	AH27	TDI	AK4	IO217PPB5V2
AG22	IO159NDB4V0	AH28	VCC	AK5	GND
AG23	IO159PDB4V0	AH29	VPUMP	AK6	IO215PPB5V2
AG24	IO158PPB4V0	AH30	GND	AK7	GND
AG25	GDB2/IO155PDB4V0	AJ1	GND	AK8	IO207NDB5V1
AG26	GDA2/IO154PPB4V0	AJ2	GND	AK9	IO207PDB5V1
AG27	GND	AJ3	GEA2/IO233PPB5V4	AK10	IO201NDB5V0
AG28	VJTAG	AJ4	VCC	AK11	IO201PDB5V0
AG29	VCC	AJ5	IO217NPB5V2	AK12	IO193NDB4V4
AG30	IO149NDB3V4	AJ6	VCC	AK13	IO193PDB4V4
AH1	GND	AJ7	IO215NPB5V2	AK14	IO197PDB5V0
AH2	IO233NPB5V4	AJ8	IO213NDB5V2	AK15	IO191NDB4V4
AH3	VCC	AJ9	IO213PDB5V2	AK16	IO191PDB4V4
AH4	GEB2/IO232PPB5V4	AJ10	IO209NDB5V1	AK17	IO189NDB4V4
AH5	VCCIB5	AJ11	IO209PDB5V1	AK18	IO189PDB4V4
AH6	IO219NDB5V3	AJ12	IO203NDB5V1	AK19	IO179PPB4V3
AH7	IO219PDB5V3	AJ13	IO203PDB5V1	AK20	IO175NDB4V2
AH8	IO227NDB5V4	AJ14	IO197NDB5V0	AK21	IO175PDB4V2
AH9	IO227PDB5V4	AJ15	IO195PDB5V0	AK22	IO169NDB4V1
AH10	IO225PPB5V3	AJ16	IO183NDB4V3	AK23	IO169PDB4V1
AH11	IO223PPB5V3	AJ17	IO183PDB4V3	AK24	GND
AH12	IO211NDB5V2	AJ18	IO179NPB4V3	AK25	IO167PPB4V1
AH13	IO211PDB5V2	AJ19	IO177PDB4V2	AK26	GND
AH14	IO205PPB5V1	AJ20	IO173NDB4V2	AK27	GDC2/IO156PPB4V0

FG896		FG896		FG896	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
E17	IO49PDB1V1	F23	IO72PDB1V3	G29	IO100PPB2V2
E18	IO50PDB1V1	F24	GNDQ	G30	GND
E19	IO58PDB1V2	F25	GND	H1	IO294PDB7V2
E20	IO60NDB1V2	F26	VMV2	H2	IO294NDB7V2
E21	IO77PDB1V4	F27	IO86PDB2V0	H3	IO300NDB7V3
E22	IO68NDB1V3	F28	IO92PDB2V1	H4	IO300PDB7V3
E23	IO68PDB1V3	F29	VCC	H5	IO295PDB7V2
E24	VCCIB1	F30	IO100NPB2V2	H6	IO299PDB7V3
E25	IO74PDB1V4	G1	GND	H7	VCOMPLA
E26	VCC	G2	IO296NPB7V2	H8	GND
E27	GBB1/IO80PPB1V4	G3	IO306NDB7V4	H9	IO08NDB0V0
E28	VCCIB2	G4	IO297NDB7V2	H10	IO08PDB0V0
E29	IO82NPB2V0	G5	VCCIB7	H11	IO18PDB0V2
E30	GND	G6	GNDQ	H12	IO26NPB0V3
F1	IO296PPB7V2	G7	VCC	H13	IO28NDB0V3
F2	VCC	G8	VMV0	H14	IO28PDB0V3
F3	IO306PDB7V4	G9	VCCIB0	H15	IO38PPB0V4
F4	IO297PDB7V2	G10	IO10NDB0V1	H16	IO42NDB1V0
F5	VMV7	G11	IO16NDB0V1	H17	IO52NDB1V1
F6	GND	G12	IO22PDB0V2	H18	IO52PDB1V1
F7	GNDQ	G13	IO26PPB0V3	H19	IO62NDB1V2
F8	IO12NDB0V1	G14	IO38NPB0V4	H20	IO62PDB1V2
F9	IO12PDB0V1	G15	IO36NDB0V4	H21	IO70NDB1V3
F10	IO10PDB0V1	G16	IO46NDB1V0	H22	IO70PDB1V3
F11	IO16PDB0V1	G17	IO46PDB1V0	H23	GND
F12	IO22NDB0V2	G18	IO56NDB1V1	H24	VCOMPLB
F13	IO30NDB0V3	G19	IO56PDB1V1	H25	GBC2/IO84PDB2V0
F14	IO30PDB0V3	G20	IO66NDB1V3	H26	IO84NDB2V0
F15	IO36PDB0V4	G21	IO66PDB1V3	H27	IO96PDB2V1
F16	IO48NDB1V0	G22	VCCIB1	H28	IO96NDB2V1
F17	IO48PDB1V0	G23	VMV1	H29	IO89PDB2V0
F18	IO50NDB1V1	G24	VCC	H30	IO89NDB2V0
F19	IO58NDB1V2	G25	GNDQ	J1	IO290NDB7V2
F20	IO60PDB1V2	G26	VCCIB2	J2	IO290PDB7V2
F21	IO77NDB1V4	G27	IO86NDB2V0	J3	IO302NDB7V3
F22	IO72NDB1V3	G28	IO92NDB2V1	J4	IO302PDB7V3

FG896		FG896		FG896	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
J5	IO295NDB7V2	K11	IO04PPB0V0	L17	VCC
J6	IO299NDB7V3	K12	VCCIB0	L18	VCC
J7	VCCIB7	K13	VCCIB0	L19	VCC
J8	VCCPLA	K14	VCCIB0	L20	VCC
J9	VCC	K15	VCCIB0	L21	IO78NPB1V4
J10	IO04NPB0V0	K16	VCCIB1	L22	IO104NPB2V2
J11	IO18NDB0V2	K17	VCCIB1	L23	IO98NDB2V2
J12	IO20NDB0V2	K18	VCCIB1	L24	IO98PDB2V2
J13	IO20PDB0V2	K19	VCCIB1	L25	IO87PDB2V0
J14	IO32NDB0V3	K20	IO76PPB1V4	L26	IO87NDB2V0
J15	IO32PDB0V3	K21	VCC	L27	IO97PDB2V1
J16	IO42PDB1V0	K22	IO78PPB1V4	L28	IO101PDB2V2
J17	IO44NDB1V0	K23	IO88NDB2V0	L29	IO103PDB2V2
J18	IO44PDB1V0	K24	IO88PDB2V0	L30	IO119NDB3V0
J19	IO54NDB1V1	K25	IO94PDB2V1	M1	IO282NDB7V1
J20	IO54PDB1V1	K26	IO94NDB2V1	M2	IO282PDB7V1
J21	IO76NPB1V4	K27	IO85PDB2V0	M3	IO292NDB7V2
J22	VCC	K28	IO85NDB2V0	M4	IO292PDB7V2
J23	VCCPLB	K29	IO93PDB2V1	M5	IO283NDB7V1
J24	VCCIB2	K30	IO93NDB2V1	M6	IO285PDB7V1
J25	IO90PDB2V1	L1	IO286NDB7V1	M7	IO287PDB7V1
J26	IO90NDB2V1	L2	IO286PDB7V1	M8	IO289PDB7V1
J27	GBB2/IO83PDB2V0	L3	IO298NDB7V3	M9	IO289NDB7V1
J28	IO83NDB2V0	L4	IO298PDB7V3	M10	VCCIB7
J29	IO91PDB2V1	L5	IO283PDB7V1	M11	VCC
J30	IO91NDB2V1	L6	IO291NDB7V2	M12	GND
K1	IO288NDB7V1	L7	IO291PDB7V2	M13	GND
K2	IO288PDB7V1	L8	IO293PDB7V2	M14	GND
K3	IO304NDB7V3	L9	IO293NDB7V2	M15	GND
K4	IO304PDB7V3	L10	IO307NPB7V4	M16	GND
K5	GAB2/IO308PDB7V4	L11	VCC	M17	GND
K6	IO308NDB7V4	L12	VCC	M18	GND
K7	IO301PDB7V3	L13	VCC	M19	GND
K8	IO301NDB7V3	L14	VCC	M20	VCC
K9	GAC2/IO307PPB7V4	L15	VCC	M21	VCCIB2
K10	VCC	L16	VCC	M22	NC

Revision	Changes	Page
Revision 11 (August 2012)	Added a Note stating "VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information." to Table 2-1 • Absolute Maximum Ratings and Table 2-2 • Recommended Operating Conditions ¹ (SAR 38322).	2-1 3-1 2-1
	The drive strength, IOL, and IOH value for 3.3 V GTL and 2.5 V GTL was changed from 25 mA to 20 mA in the following tables (SAR 31924): "Summary of Maximum and Minimum DC Input and Output Levels" table "Summary of I/O Timing Characteristics—Software Default Settings" table "I/O Output Buffer Maximum Resistances ¹ " table "Minimum and Maximum DC Input and Output Levels" table "Minimum and Maximum DC Input and Output Levels" table Also added note stating "Output drive strength is below JEDEC specification" for Tables 2-17 and 2-19. Additionally, the IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected from 51 to 35 (for 3.3 V GTL+) and from 40 to 33 (for 2.5 V GTL+) in table Table 2-13 (SAR 39714).	2-16 2-19 2-20 2-39 2-40
	"Duration of Short Circuit Event Before Failure" table was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 37934).	2-22
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34796): "It uses a 5 V–tolerant input buffer and push-pull output buffer." This change was made in revision 10 and omitted from the change table in error.	2-30
	Figure 2-11 was updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34889).	2-38
Revision 11 (continued)	In Table 2-81 VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 37222).	2-52
	Figure 2-47 and Figure 2-48 are new (SAR 34848).	2-79
	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions and Packaging" chapter: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38322). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1