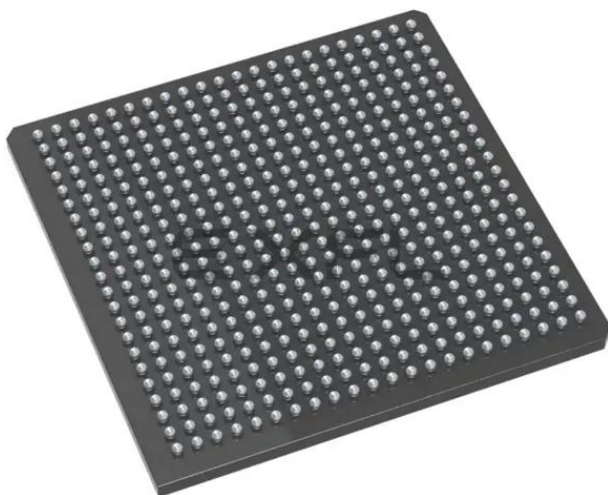




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	516096
Number of I/O	341
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3pe3000-fg484

I/Os Per Package¹

ProASIC3E Devices	A3PE600		A3PE1500 ³		A3PE3000 ³		
Cortex-M1 Devices ²			M1A3PE1500		M1A3PE3000		
Package	I/O Types						
	Single-Ended I/O ¹	Differential I/O Pairs	Single-Ended I/O ¹	Differential I/O Pairs	Single-Ended I/O ¹	Differential I/O Pairs	
	PQ208	147	65	147	65	147	65
	FG256	165	79	–	–	–	–
	FG324	–	–	–	–	221	110
	FG484	270	135	280	139	341	168
	FG676	–	–	444	222	–	–
	FG896	–	–	–	–	620	310

Notes:

- When considering migrating your design to a lower- or higher-density device, refer to the [ProASIC3E FPGA Fabric User's Guide](#) to ensure compliance with design and board migration requirements.
- Each used differential I/O pair reduces the number of single-ended I/Os available by two.
- For A3PE1500 and A3PE3000 devices, the usage of certain I/O standards is limited as follows:
 - SSTL3(I) and (II): up to 40 I/Os per north or south bank
 - LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank
 - SSTL2(I) and (II) / GTL+ 2.5 V / GTL 2.5 V: up to 72 I/Os per north or south bank
- FG256 and FG484 are footprint-compatible packages.
- When using voltage-referenced I/O standards, one I/O pin should be assigned as a voltage-referenced pin (VREF) per minibank (group of I/Os).
- "G" indicates RoHS-compliant packages. Refer to the ["ProASIC3E Ordering Information"](#) on page III for the location of the "G" in the part number.

Table 1-2 • ProASIC3E FPGAs Package Sizes Dimensions

Package	PQ208	FG256	FG324	FG484	FG676	FG896
Length × Width (mm\mm)	28 × 28	17 × 17	19 × 19	23 × 23	27 × 27	31 × 31
Nominal Area (mm ²)	784	289	361	529	729	961
Pitch (mm)	0.5	1.0	1.0	1.0	1.0	1.0
Height (mm)	3.40	1.60	1.63	2.23	2.23	2.23

ProASIC3E Device Status

ProASIC3E Devices	Status	M1 ProASIC3E Devices	Status
A3PE600	Production		
A3PE1500	Production	M1A3PE1500	Production
A3PE3000	Production	M1A3PE3000	Production

Table 2-32 • 3.3 V LVCMOS Wide Range Low Slew
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	4 mA	Std.	0.66	17.02	0.04	1.83	2.38	0.43	17.02	13.74	4.16	3.78	20.42	17.14	ns
		–1	0.56	14.48	0.04	1.55	2.02	0.36	14.48	11.69	3.54	3.21	17.37	14.58	ns
		–2	0.49	12.71	0.03	1.36	1.78	0.32	12.71	10.26	3.11	2.82	15.25	12.80	ns
100 μA	8 mA	Std.	0.66	12.16	0.04	1.83	2.38	0.43	12.16	9.78	4.70	4.74	15.55	13.17	ns
		–1	0.56	10.34	0.04	1.55	2.02	0.36	10.34	8.32	4.00	4.03	13.23	11.20	ns
		–2	0.49	9.08	0.03	1.36	1.78	0.32	9.08	7.30	3.51	3.54	11.61	9.84	ns
100 μA	12 mA	Std.	0.66	9.32	0.04	1.83	2.38	0.43	9.32	7.62	5.06	5.36	12.71	11.02	ns
		–1	0.56	7.93	0.04	1.55	2.02	0.36	7.93	6.48	4.31	4.56	10.81	9.37	ns
		–2	0.49	6.96	0.03	1.36	1.78	0.32	6.96	5.69	3.78	4.00	9.49	8.23	ns
100 μA	16 mA	Std.	0.66	8.69	0.04	1.83	2.38	0.43	8.69	7.17	5.14	5.53	12.08	10.57	ns
		–1	0.56	7.39	0.04	1.55	2.02	0.36	7.39	6.10	4.37	4.71	10.28	8.99	ns
		–2	0.49	6.49	0.03	1.36	1.78	0.32	6.49	5.36	3.83	4.13	9.02	7.89	ns
100 μA	24 mA	Std.	0.66	8.11	0.04	1.83	2.38	0.43	8.11	7.13	5.23	6.13	11.50	10.52	ns
		–1	0.56	6.90	0.04	1.55	2.02	0.36	6.90	6.06	4.45	5.21	9.78	8.95	ns
		–2	0.49	6.05	0.03	1.36	1.78	0.32	6.05	5.32	3.91	4.57	8.59	7.86	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. Software default selection highlighted in gray.
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

Table 2-40 • 1.8 V LVCMOS Low Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.7\text{ V}$

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	15.84	0.04	1.45	1.91	0.43	15.65	15.84	2.78	1.58	17.89	18.07	ns
	–1	0.56	13.47	0.04	1.23	1.62	0.36	13.31	13.47	2.37	1.35	15.22	15.37	ns
	–2	0.49	11.83	0.03	1.08	1.42	0.32	11.69	11.83	2.08	1.18	13.36	13.50	ns
4 mA	Std.	0.66	11.39	0.04	1.45	1.91	0.43	11.60	10.76	3.26	2.77	13.84	12.99	ns
	–1	0.56	9.69	0.04	1.23	1.62	0.36	9.87	9.15	2.77	2.36	11.77	11.05	ns
	–2	0.49	8.51	0.03	1.08	1.42	0.32	8.66	8.03	2.43	2.07	10.33	9.70	ns
6 mA	Std.	0.66	8.97	0.04	1.45	1.91	0.43	9.14	8.10	3.57	3.36	11.37	10.33	ns
	–1	0.56	7.63	0.04	1.23	1.62	0.36	7.77	6.89	3.04	2.86	9.67	8.79	ns
	–2	0.49	6.70	0.03	1.08	1.42	0.32	6.82	6.05	2.66	2.51	8.49	7.72	ns
8 mA	Std.	0.66	8.35	0.04	1.45	1.91	0.43	8.50	7.59	3.64	3.52	10.74	9.82	ns
	–1	0.56	7.10	0.04	1.23	1.62	0.36	7.23	6.45	3.10	3.00	9.14	8.35	ns
	–2	0.49	6.24	0.03	1.08	1.42	0.32	6.35	5.66	2.72	2.63	8.02	7.33	ns
12 mA	Std.	0.66	7.94	0.04	1.45	1.91	0.43	8.09	7.56	3.74	4.11	10.32	9.80	ns
	–1	0.56	6.75	0.04	1.23	1.62	0.36	6.88	6.43	3.18	3.49	8.78	8.33	ns
	–2	0.49	5.93	0.03	1.08	1.42	0.32	6.04	5.65	2.79	3.07	7.71	7.32	ns
16 mA	Std.	0.66	7.94	0.04	1.45	1.91	0.43	8.09	7.56	3.74	4.11	10.32	9.80	ns
	–1	0.56	6.75	0.04	1.23	1.62	0.36	6.88	6.43	3.18	3.49	8.78	8.33	ns
	–2	0.49	5.93	0.03	1.08	1.42	0.32	6.04	5.65	2.79	3.07	7.71	7.32	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-51 • Minimum and Maximum DC Input and Output Levels

2.5 GTL	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min., V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
20 mA ³	−0.3	VREF − 0.05	VREF + 0.05	3.6	0.4	−	20	20	124	169	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Output drive strength is below JEDEC specification.

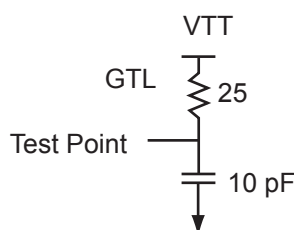


Figure 2-13 • AC Loading

Table 2-52 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF − 0.05	VREF + 0.05	0.8	0.8	1.2	10

Note: *Measuring point = Vtrip. See [Table 2-15 on page 2-18](#) for a complete table of trip points.

Timing Characteristics

Table 2-53 • 2.5 V GTL

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V VREF = 0.8 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.60	2.13	0.04	2.46	0.43	2.16	2.13			4.40	4.36	ns
−1	0.51	1.81	0.04	2.09	0.36	1.84	1.81			3.74	3.71	ns
−2	0.45	1.59	0.03	1.83	0.32	1.61	1.59			3.28	3.26	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL ¹	Output Lower Current	0.65	0.91	1.16	mA
IOH ¹	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
IIH ²	Input High Leakage Current			10	μA
IIL ²	Input Low Leakage Current			10	μA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage ²	100	350		mV

Notes:

1. IOL/IOH defined by VODIFF/(Resistor Network).
2. Currents are measured at 85°C junction temperature.

Table 2-79 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)
1.075	1.325	Cross point	–

Note: *Measuring point = Vtrip. See [Table 2-15 on page 2-18](#) for a complete table of trip points.

Timing Characteristics

Table 2-93 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Combinatorial Cell	Equation	Parameter	-2	-1	Std.	Units
INV	$Y = !A$	t_{PD}	0.40	0.46	0.54	ns
AND2	$Y = A \cdot B$	t_{PD}	0.47	0.54	0.63	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.47	0.54	0.63	ns
OR2	$Y = A + B$	t_{PD}	0.49	0.55	0.65	ns
NOR2	$Y = !(A + B)$	t_{PD}	0.49	0.55	0.65	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.74	0.84	0.99	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	0.70	0.79	0.93	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	0.87	1.00	1.17	ns
MUX2	$Y = A \text{ IS } + B \text{ S}$	t_{PD}	0.51	0.58	0.68	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.56	0.64	0.75	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-5](#) for derating values.

VersaTile Specifications as a Sequential Module

The ProASIC3E library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the [Fusion](#), [IGLOO/e](#), and [ProASIC3/E Macro Library Guide](#).

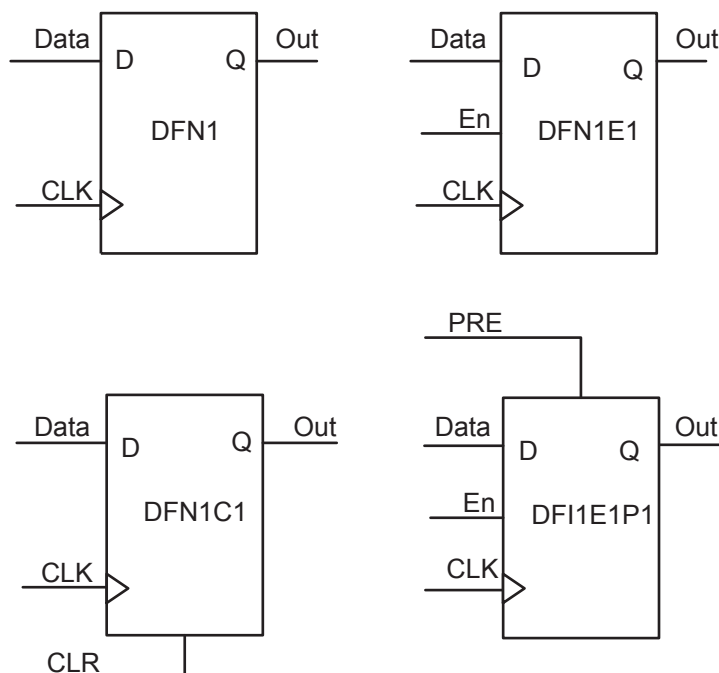


Figure 2-36 • Sample of Sequential Cells

Global Resource Characteristics

A3PE600 Clock Tree Topology

Clock delays are device-specific. Figure 2-38 is an example of a global tree used for clock routing. The global tree presented in Figure 2-38 is driven by a CCC located on the west side of the A3PE600 device. It is used to drive all D-flip-flops in the device.

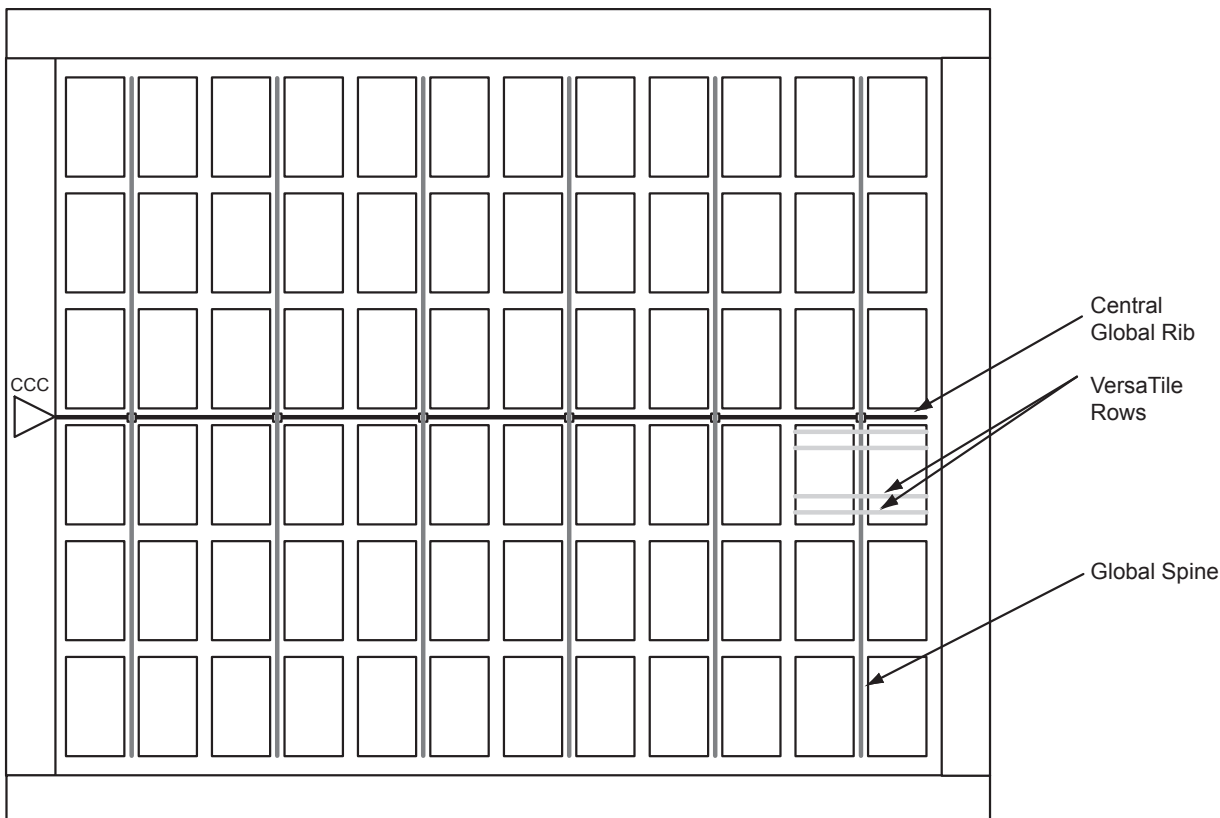


Figure 2-38 • Example of Global Tree Use in an A3PE600 Device for Clock Routing

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-70. Table 2-95 on page 2-69, Table 2-96 on page 2-69, and Table 2-97 on page 2-69 present minimum and maximum global clock delays within the device. Minimum and maximum delays are measured with minimum and maximum loading.

FIFO

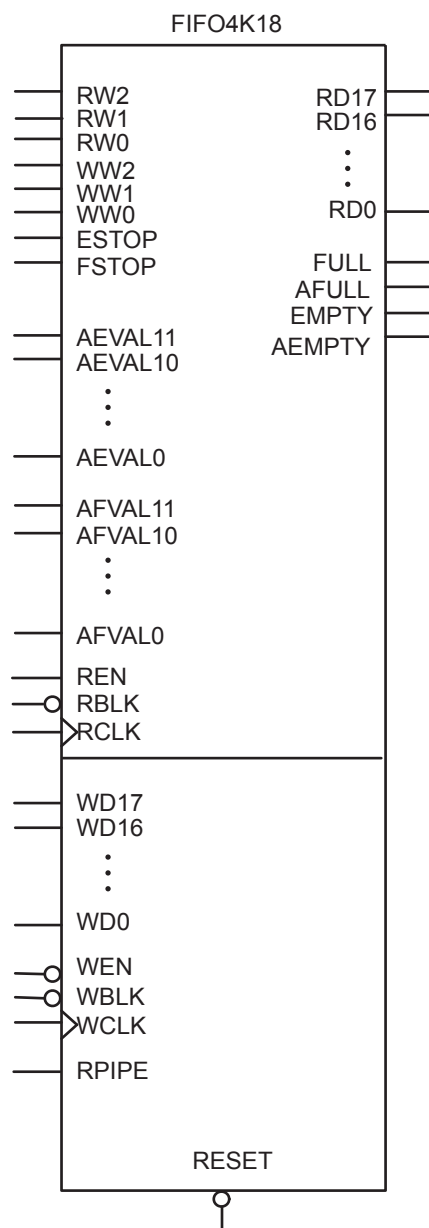


Figure 2-46 • FIFO Model

Refer to the I/O Structure section of the [ProASIC3E FPGA Fabric User's Guide](#) for an explanation of the naming of global pins.

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK

Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements. Refer to [Table 3-1](#) for more information.

Table 3-1 • Recommended Tie-Off Values for the TCK and TRST Pins

VJTAG	Tie-Off Resistance
VJTAG at 3.3 V	200 Ω to 1 k Ω
VJTAG at 2.5 V	200 Ω to 1 k Ω
VJTAG at 1.8 V	500 Ω to 1 k Ω
VJTAG at 1.5 V	500 Ω to 1 k Ω

Notes:

1. Equivalent parallel resistance if more than one device is on the JTAG chain
2. The TCK pin can be pulled up/down.
3. The TRST pin is pulled down.

TDI

Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO

Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS

Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST

Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from [Table 3-1](#) and must satisfy the parallel resistance value requirement. The values in [Table 3-1](#) correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements.

Special Function Pins

NC

No Connect

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC

Do Not Connect

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Packaging

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

Microsemi consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Microsemi IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Microsemi offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

Related Documents

User's Guides

ProASIC3E FPGA Fabric User's Guide

http://www.microsemi.com/document-portal/doc_download/130883-proasic3e-fpga-fabric-user-s-guide

Packaging

The following documents provide packaging information and device selection for low power flash devices.

Product Catalog

http://www.microsemi.com/soc/documents/ProdCat_PIB.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

Package Mechanical Drawings

http://www.microsemi.com/document-portal/doc_download/131095-package-mechanical-drawings

This document contains the package mechanical drawings for all packages currently or previously supplied by Microsemi. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials: <http://www.microsemi.com/products/fpga-soc/solutions>.

PQ208	
Pin Number	A3PE1500 Function
109	TRST
110	VJTAG
111	VMV3
112	GDA0/IO110NPB3V2
113	GDB0/IO109NPB3V2
114	GDA1/IO110PPB3V2
115	GDB1/IO109PPB3V2
116	GDC0/IO108NDB3V2
117	GDC1/IO108PDB3V2
118	IO105NDB3V2
119	IO105PDB3V2
120	IO101NDB3V1
121	IO101PDB3V1
122	GND
123	VCCIB3
124	GCC2/IO90PSB3V0
125	GCB2/IO89PSB3V0
126	NC
127	IO88NDB3V0
128	GCA2/IO88PDB3V0
129	GCA1/IO87PPB3V0
130	GND
131	VCCPLC
132	GCA0/IO87NPB3V0
133	VCOMPLC
134	GCB0/IO86NDB2V3
135	GCB1/IO86PDB2V3
136	GCC1/IO85PSB2V3
137	IO83NDB2V3
138	IO83PDB2V3
139	IO81PSB2V3
140	VCCIB2
141	GND
142	VCC
143	IO73NDB2V2
144	IO73PDB2V2

PQ208	
Pin Number	A3PE1500 Function
145	IO71NDB2V2
146	IO71PDB2V2
147	IO67NDB2V1
148	IO67PDB2V1
149	IO65NDB2V1
150	IO65PDB2V1
151	GBC2/IO60PSB2V0
152	GBA2/IO58PSB2V0
153	GBB2/IO59PSB2V0
154	VMV2
155	GNDQ
156	GND
157	VMV1
158	GNDQ
159	GBA1/IO57PDB1V3
160	GBA0/IO57NDB1V3
161	GBB1/IO56PDB1V3
162	GND
163	GBB0/IO56NDB1V3
164	GBC1/IO55PDB1V3
165	GBC0/IO55NDB1V3
166	IO51PDB1V2
167	IO51NDB1V2
168	IO47PDB1V1
169	IO47NDB1V1
170	VCCIB1
171	VCC
172	IO43PSB1V1
173	IO41PDB1V1
174	IO41NDB1V1
175	IO35PDB1V0
176	IO35NDB1V0
177	IO31PDB0V3
178	GND
179	IO31NDB0V3
180	IO29PDB0V3

PQ208	
Pin Number	A3PE1500 Function
181	IO29NDB0V3
182	IO27PDB0V3
183	IO27NDB0V3
184	IO23PDB0V2
185	IO23NDB0V2
186	VCCIB0
187	VCC
188	IO18PDB0V2
189	IO18NDB0V2
190	IO15PDB0V1
191	IO15NDB0V1
192	IO12PSB0V1
193	IO11PDB0V1
194	IO11NDB0V1
195	GND
196	IO08PDB0V1
197	IO08NDB0V1
198	IO05PDB0V0
199	IO05NDB0V0
200	VCCIB0
201	GAC1/IO02PDB0V0
202	GAC0/IO02NDB0V0
203	GAB1/IO01PDB0V0
204	GAB0/IO01NDB0V0
205	GAA1/IO00PDB0V0
206	GAA0/IO00NDB0V0
207	GNDQ
208	VMV0

FG256	
Pin Number	A3PE600 Function
G13	GCC1/IO50PPB2V1
G14	IO44NDB2V1
G15	IO44PDB2V1
G16	IO49NSB2V1
H1	GFB0/IO119NPB7V0
H2	GFA0/IO118NDB6V1
H3	GFB1/IO119PPB7V0
H4	VCOMPLF
H5	GFC0/IO120NPB7V0
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO50NPB2V1
H13	GCB1/IO51PPB2V1
H14	GCA0/IO52NPB3V0
H15	VCOMPLC
H16	GCB0/IO51NPB2V1
J1	GFA2/IO117PSB6V1
J2	GFA1/IO118PDB6V1
J3	VCCPLF
J4	IO116NDB6V1
J5	GFB2/IO116PDB6V1
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO54PPB3V0
J13	GCA1/IO52PPB3V0
J14	GCC2/IO55PPB3V0
J15	VCCPLC
J16	GCA2/IO53PSB3V0

FG256	
Pin Number	A3PE600 Function
K1	GFC2/IO115PSB6V1
K2	IO113PPB6V1
K3	IO112PDB6V1
K4	IO112NDB6V1
K5	VCCIB6
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB3
K13	IO54NPB3V0
K14	IO57NPB3V0
K15	IO55NPB3V0
K16	IO57PPB3V0
L1	IO113NPB6V1
L2	IO109PPB6V0
L3	IO108PDB6V0
L4	IO108NDB6V0
L5	VCCIB6
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB3
L13	GDB0/IO66NPB3V1
L14	IO60NDB3V1
L15	IO60PDB3V1
L16	IO61PDB3V1
M1	IO109NPB6V0
M2	IO106NDB6V0
M3	IO106PDB6V0
M4	GEC0/IO104NPB6V0

FG256	
Pin Number	A3PE600 Function
M5	VMV5
M6	VCCIB5
M7	VCCIB5
M8	IO84NDB5V0
M9	IO84PDB5V0
M10	VCCIB4
M11	VCCIB4
M12	VMV3
M13	VCCPLD
M14	GDB1/IO66PPB3V1
M15	GDC1/IO65PDB3V1
M16	IO61NDB3V1
N1	IO105PDB6V0
N2	IO105NDB6V0
N3	GEC1/IO104PPB6V0
N4	VCOMPLE
N5	GNDQ
N6	GEA2/IO101PPB5V2
N7	IO92NDB5V1
N8	IO90NDB5V1
N9	IO82NDB5V0
N10	IO74NDB4V1
N11	IO74PDB4V1
N12	GNDQ
N13	VCOMPLD
N14	VJTAG
N15	GDC0/IO65NDB3V1
N16	GDA1/IO67PDB3V1
P1	GEB1/IO103PDB6V0
P2	GEB0/IO103NDB6V0
P3	VMV6
P4	VCCPLE
P5	IO101NPB5V2
P6	IO95PPB5V1
P7	IO92PDB5V1
P8	IO90PDB5V1

FG256	
Pin Number	A3PE600 Function
P9	IO82PDB5V0
P10	IO76NDB4V1
P11	IO76PDB4V1
P12	VMV4
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO67NDB3V1
R1	GEA1/IO102PDB6V0
R2	GEA0/IO102NDB6V0
R3	GNDQ
R4	GEC2/IO99PDB5V2
R5	IO95NPB5V1
R6	IO91NDB5V1
R7	IO91PDB5V1
R8	IO83NDB5V0
R9	IO83PDB5V0
R10	IO77NDB4V1
R11	IO77PDB4V1
R12	IO69NDB4V0
R13	GDB2/IO69PDB4V0
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO100NDB5V2
T3	GEB2/IO100PDB5V2
T4	IO99NDB5V2
T5	IO88NDB5V0
T6	IO88PDB5V0
T7	IO89NSB5V0
T8	IO80NSB4V1
T9	IO81NDB4V1
T10	IO81PDB4V1
T11	IO70NDB4V0
T12	GDC2/IO70PDB4V0

FG256	
Pin Number	A3PE600 Function
T13	IO68NDB4V0
T14	GDA2/IO68PDB4V0
T15	TMS
T16	GND

FG484		FG484		FG484	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
A1	GND	AA15	IO170PDB4V2	B7	IO14PDB0V1
A2	GND	AA16	IO166NDB4V1	B8	IO18NDB0V2
A3	VCCIB0	AA17	IO166PDB4V1	B9	IO24NDB0V2
A4	IO10NDB0V1	AA18	IO160NDB4V0	B10	IO34PDB0V4
A5	IO10PDB0V1	AA19	IO160PDB4V0	B11	IO40PDB0V4
A6	IO16NDB0V1	AA20	IO158NPB4V0	B12	IO46NDB1V0
A7	IO16PDB0V1	AA21	VCCIB3	B13	IO54NDB1V1
A8	IO18PDB0V2	AA22	GND	B14	IO62NDB1V2
A9	IO24PDB0V2	AB1	GND	B15	IO62PDB1V2
A10	IO28NDB0V3	AB2	GND	B16	IO68NDB1V3
A11	IO28PDB0V3	AB3	VCCIB5	B17	IO68PDB1V3
A12	IO46PDB1V0	AB4	IO216NDB5V2	B18	IO72PDB1V3
A13	IO54PDB1V1	AB5	IO216PDB5V2	B19	IO74PDB1V4
A14	IO56NDB1V1	AB6	IO210NDB5V2	B20	IO76NPB1V4
A15	IO56PDB1V1	AB7	IO210PDB5V2	B21	VCCIB2
A16	IO64NDB1V2	AB8	IO208NDB5V1	B22	GND
A17	IO64PDB1V2	AB9	IO208PDB5V1	C1	VCCIB7
A18	IO72NDB1V3	AB10	IO197NDB5V0	C2	IO303PDB7V3
A19	IO74NDB1V4	AB11	IO197PDB5V0	C3	IO305PDB7V3
A20	VCCIB1	AB12	IO174NDB4V2	C4	IO06NPB0V0
A21	GND	AB13	IO174PDB4V2	C5	GND
A22	GND	AB14	IO172NDB4V2	C6	IO12NDB0V1
AA1	GND	AB15	IO172PDB4V2	C7	IO12PDB0V1
AA2	VCCIB6	AB16	IO168NDB4V1	C8	VCC
AA3	IO228PDB5V4	AB17	IO168PDB4V1	C9	VCC
AA4	IO224PDB5V3	AB18	IO162NDB4V1	C10	IO34NDB0V4
AA5	IO218NDB5V3	AB19	IO162PDB4V1	C11	IO40NDB0V4
AA6	IO218PDB5V3	AB20	VCCIB4	C12	IO48NDB1V0
AA7	IO212NDB5V2	AB21	GND	C13	IO48PDB1V0
AA8	IO212PDB5V2	AB22	GND	C14	VCC
AA9	IO198PDB5V0	B1	GND	C15	VCC
AA10	IO198NDB5V0	B2	VCCIB7	C16	IO70NDB1V3
AA11	IO188PPB4V4	B3	IO06PPB0V0	C17	IO70PDB1V3
AA12	IO180NDB4V3	B4	IO08NDB0V0	C18	GND
AA13	IO180PDB4V3	B5	IO08PDB0V0	C19	IO76PPB1V4
AA14	IO170NDB4V2	B6	IO14NDB0V1	C20	IO88NDB2V0

FG676	
Pin Number	A3PE1500 Function
A1	GND
A2	GND
A3	GAA0/IO00NDB0V0
A4	GAA1/IO00PDB0V0
A5	IO06NDB0V0
A6	IO09NDB0V1
A7	IO09PDB0V1
A8	IO14NDB0V1
A9	IO14PDB0V1
A10	IO22NDB0V2
A11	IO22PDB0V2
A12	IO26NDB0V3
A13	IO26PDB0V3
A14	IO30NDB0V3
A15	IO30PDB0V3
A16	IO34NDB1V0
A17	IO34PDB1V0
A18	IO38NDB1V0
A19	IO38PDB1V0
A20	IO41PDB1V1
A21	IO44PDB1V1
A22	IO49PDB1V2
A23	IO50PDB1V2
A24	GBC1/IO55PDB1V3
A25	GND
A26	GND
AA1	IO174PDB6V0
AA2	IO171PDB6V0
AA3	GEA1/IO167PPB6V0
AA4	GEC0/IO169NPB6V0
AA5	VCOMPLE
AA6	GND
AA7	IO165NDB5V3
AA8	GEB2/IO165PDB5V3
AA9	IO163PDB5V3
AA10	IO159NDB5V3

FG676	
Pin Number	A3PE1500 Function
AA11	IO153NDB5V2
AA12	IO147NDB5V1
AA13	IO139NDB5V0
AA14	IO137NDB5V0
AA15	IO123NDB4V1
AA16	IO123PDB4V1
AA17	IO117NDB4V0
AA18	IO117PDB4V0
AA19	GDB2/IO112PDB4V0
AA20	GNDQ
AA21	TDO
AA22	GND
AA23	GND
AA24	IO102NDB3V1
AA25	IO102PDB3V1
AA26	IO98NDB3V1
AB1	IO174NDB6V0
AB2	IO171NDB6V0
AB3	GEB1/IO168PPB6V0
AB4	GEA0/IO167NPB6V0
AB5	VCCPLE
AB6	GND
AB7	GND
AB8	IO156NDB5V2
AB9	IO156PDB5V2
AB10	IO150PDB5V1
AB11	IO155PDB5V2
AB12	IO142PDB5V0
AB13	IO135NDB5V0
AB14	IO135PDB5V0
AB15	IO132PDB4V2
AB16	IO129PDB4V2
AB17	IO121PDB4V1
AB18	IO119NDB4V1
AB19	IO112NDB4V0
AB20	VMV4

FG676	
Pin Number	A3PE1500 Function
AB21	TCK
AB22	TRST
AB23	GDC0/IO108NDB3V2
AB24	GDC1/IO108PDB3V2
AB25	IO104NDB3V2
AB26	IO104PDB3V2
AC1	IO170PDB6V0
AC2	GEB0/IO168NPB6V0
AC3	IO166NPB5V3
AC4	GNDQ
AC5	GND
AC6	IO160PDB5V3
AC7	IO161PDB5V3
AC8	IO154PDB5V2
AC9	GND
AC10	IO150NDB5V1
AC11	IO155NDB5V2
AC12	IO142NDB5V0
AC13	IO138NDB5V0
AC14	IO138PDB5V0
AC15	IO132NDB4V2
AC16	IO129NDB4V2
AC17	IO121NDB4V1
AC18	IO119PDB4V1
AC19	IO118NDB4V0
AC20	IO118PDB4V0
AC21	IO114PPB4V0
AC22	TMS
AC23	VJTAG
AC24	VMV3
AC25	IO106NDB3V2
AC26	IO106PDB3V2
AD1	IO170NDB6V0
AD2	GEA2/IO166PPB5V3
AD3	VMV5
AD4	GEC2/IO164PDB5V3

FG676	
Pin Number	A3PE1500 Function
G13	IO21NDB0V2
G14	IO27PDB0V3
G15	IO35NDB1V0
G16	IO39PDB1V0
G17	IO51NDB1V2
G18	IO53NDB1V2
G19	VCCIB1
G20	GBA2/IO58PPB2V0
G21	GNDQ
G22	IO64NDB2V1
G23	IO64PDB2V1
G24	IO72PDB2V2
G25	IO72NDB2V2
G26	IO78PDB2V2
H1	IO208NDB7V2
H2	IO208PDB7V2
H3	IO209NDB7V2
H4	IO209PDB7V2
H5	IO219NDB7V3
H6	GAC2/IO219PDB7V3
H7	VCCIB7
H8	VCC
H9	VCCIB0
H10	VCCIB0
H11	VCCIB0
H12	VCCIB0
H13	VCCIB0
H14	VCCIB1
H15	VCCIB1
H16	VCCIB1
H17	VCCIB1
H18	VCCIB1
H19	VCC
H20	VCC
H21	IO58NPB2V0
H22	IO70PDB2V1

FG676	
Pin Number	A3PE1500 Function
H23	IO69PDB2V1
H24	IO76PDB2V2
H25	IO76NDB2V2
H26	IO78NDB2V2
J1	IO197NDB7V0
J2	IO197PDB7V0
J3	VMV7
J4	IO215NDB7V3
J5	IO215PDB7V3
J6	IO214PDB7V3
J7	IO214NDB7V3
J8	VCCIB7
J9	VCC
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	VCC
J15	VCC
J16	VCC
J17	VCC
J18	VCC
J19	VCCIB2
J20	IO62PDB2V0
J21	IO62NDB2V0
J22	IO70NDB2V1
J23	IO69NDB2V1
J24	VMV2
J25	IO80PDB2V3
J26	IO80NDB2V3
K1	IO195PDB7V0
K2	IO199NDB7V1
K3	IO199PDB7V1
K4	IO205NDB7V1
K5	IO205PDB7V1
K6	IO217PDB7V3

FG676	
Pin Number	A3PE1500 Function
K7	IO217NDB7V3
K8	VCCIB7
K9	VCC
K10	GND
K11	GND
K12	GND
K13	GND
K14	GND
K15	GND
K16	GND
K17	GND
K18	VCC
K19	VCCIB2
K20	IO65PDB2V1
K21	IO65NDB2V1
K22	IO74PDB2V2
K23	IO74NDB2V2
K24	IO75PDB2V2
K25	IO75NDB2V2
K26	IO84PDB2V3
L1	IO195NDB7V0
L2	IO198PPB7V0
L3	GNDQ
L4	IO201PDB7V1
L5	IO201NDB7V1
L6	IO210NDB7V2
L7	IO210PDB7V2
L8	VCCIB7
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	GND
L15	GND
L16	GND

FG676	
Pin Number	A3PE1500 Function
W25	IO96PDB3V1
W26	IO94NDB3V0
Y1	IO175NDB6V1
Y2	IO175PDB6V1
Y3	IO173NDB6V0
Y4	IO173PDB6V0
Y5	GEC1/IO169PPB6V0
Y6	GNDQ
Y7	VMV6
Y8	VCCIB5
Y9	IO163NDB5V3
Y10	IO159PDB5V3
Y11	IO153PDB5V2
Y12	IO147PDB5V1
Y13	IO139PDB5V0
Y14	IO137PDB5V0
Y15	IO125NDB4V1
Y16	IO125PDB4V1
Y17	IO115NDB4V0
Y18	IO115PDB4V0
Y19	VCC
Y20	VPUMP
Y21	VCOMPLD
Y22	VCCPLD
Y23	IO100NDB3V1
Y24	IO100PDB3V1
Y25	IO96NDB3V1
Y26	IO98PDB3V1

FG896	
Pin Number	A3PE3000 Function
E17	IO49PDB1V1
E18	IO50PDB1V1
E19	IO58PDB1V2
E20	IO60NDB1V2
E21	IO77PDB1V4
E22	IO68NDB1V3
E23	IO68PDB1V3
E24	VCCIB1
E25	IO74PDB1V4
E26	VCC
E27	GBB1/IO80PPB1V4
E28	VCCIB2
E29	IO82NPB2V0
E30	GND
F1	IO296PPB7V2
F2	VCC
F3	IO306PDB7V4
F4	IO297PDB7V2
F5	VMV7
F6	GND
F7	GNDQ
F8	IO12NDB0V1
F9	IO12PDB0V1
F10	IO10PDB0V1
F11	IO16PDB0V1
F12	IO22NDB0V2
F13	IO30NDB0V3
F14	IO30PDB0V3
F15	IO36PDB0V4
F16	IO48NDB1V0
F17	IO48PDB1V0
F18	IO50NDB1V1
F19	IO58NDB1V2
F20	IO60PDB1V2
F21	IO77NDB1V4
F22	IO72NDB1V3

FG896	
Pin Number	A3PE3000 Function
F23	IO72PDB1V3
F24	GNDQ
F25	GND
F26	VMV2
F27	IO86PDB2V0
F28	IO92PDB2V1
F29	VCC
F30	IO100NPB2V2
G1	GND
G2	IO296NPB7V2
G3	IO306NDB7V4
G4	IO297NDB7V2
G5	VCCIB7
G6	GNDQ
G7	VCC
G8	VMV0
G9	VCCIB0
G10	IO10NDB0V1
G11	IO16NDB0V1
G12	IO22PDB0V2
G13	IO26PPB0V3
G14	IO38NPB0V4
G15	IO36NDB0V4
G16	IO46NDB1V0
G17	IO46PDB1V0
G18	IO56NDB1V1
G19	IO56PDB1V1
G20	IO66NDB1V3
G21	IO66PDB1V3
G22	VCCIB1
G23	VMV1
G24	VCC
G25	GNDQ
G26	VCCIB2
G27	IO86NDB2V0
G28	IO92NDB2V1

FG896	
Pin Number	A3PE3000 Function
G29	IO100PPB2V2
G30	GND
H1	IO294PDB7V2
H2	IO294NDB7V2
H3	IO300NDB7V3
H4	IO300PDB7V3
H5	IO295PDB7V2
H6	IO299PDB7V3
H7	VCOMPLA
H8	GND
H9	IO08NDB0V0
H10	IO08PDB0V0
H11	IO18PDB0V2
H12	IO26NPB0V3
H13	IO28NDB0V3
H14	IO28PDB0V3
H15	IO38PPB0V4
H16	IO42NDB1V0
H17	IO52NDB1V1
H18	IO52PDB1V1
H19	IO62NDB1V2
H20	IO62PDB1V2
H21	IO70NDB1V3
H22	IO70PDB1V3
H23	GND
H24	VCOMPLB
H25	GBC2/IO84PDB2V0
H26	IO84NDB2V0
H27	IO96PDB2V1
H28	IO96NDB2V1
H29	IO89PDB2V0
H30	IO89NDB2V0
J1	IO290NDB7V2
J2	IO290PDB7V2
J3	IO302NDB7V3
J4	IO302PDB7V3

Revision	Changes	Page
Advance v0.5 (continued)	The "I/O User Input/Output" pin description was updated to include information on what happens when the pin is unused.	2-50
	The "JTAG Pins" section was updated to include information on what happens when the pin is unused.	2-51
	The "Programming" section was updated to include information concerning serialization.	2-53
	The "JTAG 1532" section was updated to include SAMPLE/PRELOAD information.	2-54
	The "DC and Switching Characteristics" chapter was updated with new information.	Starting on page 3-1
	Table 3-6 was updated.	3-5
	In Table 3-10, PAC4 was updated.	3-8
	Table 3-19 was updated.	3-20
	The note in Table 3-24 was updated.	3-23
	All Timing Characteristics tables were updated from LVTTTL to Register Delays	3-26 to 3-64
	The Timing Characteristics for RAM4K9, RAM512X18, and FIFO were updated.	3-74 to 3-79
	F _{TCKMAX} was updated in Table 3-98.	3-80
Advance v0.4 (October 2005)	The "Packaging Tables" table was updated.	ii
Advance v0.3	Figure 2-11 was updated.	2-9
	The "Clock Resources (VersaNets)" section was updated.	2-9
	The "VersaNet Global Networks and Spine Access" section was updated.	2-9
	The "PLL Macro" section was updated.	2-15
	Figure 2-27 was updated.	2-28
	Figure 2-20 was updated.	2-19
	Table 2-5 was updated.	2-25
	Table 2-6 was updated.	2-25
	The "FIFO Flag Usage Considerations" section was updated.	2-27
	Table 2-33 was updated.	2-51
	Figure 2-24 was updated.	2-31
	The "Cold-Sparing Support" section is new.	2-34
	Table 2-45 was updated.	2-64
	Table 2-48 was updated.	2-81
	Pin descriptions in the "JTAG Pins" section were updated.	2-51
	The "Pin Descriptions" section was updated.	2-50
	Table 3-7 was updated.	3-6

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "[ProASIC3E Device Status](#)" table on page II, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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