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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	516096
Number of I/O	620
Number of Gates	300000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3pe3000-fg896

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

static Microsemi.

ProASIC3E Flash Family FPGAs

I/Os Per Package¹

ProASIC3E Devices	A3P	E600	A3PE	1500 ³	A3PE3000 ³		
Cortex-M1 Devices ²			M1A3F	PE1500	M1A3PE3000		
			I/O T	ypes			
Package	Single-Ended I/O ¹	Differential I/O Pairs	Single-Ended I/O ¹ Differential I/O Pairs		Single-Ended I/O ¹	Differential I/O Pairs	
PQ208	147	65	147	65	147	65	
FG256	165	79	-	_	-	-	
FG324	-	-	-	-	221	110	
FG484	270	135	280	139	341	168	
FG676	_	_	444	222	_	_	
FG896	-	-	-	-	620	310	

Notes:

1. When considering migrating your design to a lower- or higher-density device, refer to the ProASIC3E FPGA Fabric User's Guide to ensure compliance with design and board migration requirements.

- 2. Each used differential I/O pair reduces the number of single-ended I/Os available by two.
- 3. For A3PE1500 and A3PE3000 devices, the usage of certain I/O standards is limited as follows:
 - SSTL3(I) and (II): up to 40 I/Os per north or south bank
 - LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank
 - SSTL2(I) and (II) / GTL+ 2.5 V/ GTL 2.5 V: up to 72 I/Os per north or south bank
- 4. FG256 and FG484 are footprint-compatible packages.
- 5. When using voltage-referenced I/O standards, one I/O pin should be assigned as a voltage-referenced pin (VREF) per minibank (group of I/Os).
- 6. "G" indicates RoHS-compliant packages. Refer to the "ProASIC3E Ordering Information" on page III for the location of the "G" in the part number.

Package	PQ208	FG256	FG324	FG484	FG676	FG896
Length × Width (mm\mm)	28 × 28	17 × 17	19 × 19	23 × 23	27 × 27	31 × 31
Nominal Area (mm ²)	784	289	361	529	729	961
Pitch (mm)	0.5	1.0	1.0	1.0	1.0	1.0
Height (mm)	3.40	1.60	1.63	2.23	2.23	2.23

Table 1-2 • ProASIC3E FPGAs Package Sizes Dimensions

ProASIC3E Device Status

ProASIC3E Devices	Status	M1 ProASIC3E Devices	Status
A3PE600	Production		
A3PE1500	Production	M1A3PE1500	Production
A3PE3000	Production	M1A3PE3000	Production



ProASIC3E Device Family Overview

Pro I/Os with Advanced I/O Standards

The ProASIC3E family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). ProASIC3E FPGAs support 19 different I/O standards, including single-ended, differential, and voltage-referenced. The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported. Each I/O bank is subdivided into VREF minibanks, which are used by voltage-referenced I/Os. VREF minibanks contain 8 to 18 I/Os. All the I/Os in a given minibank share a common VREF line. Therefore, if any I/O in a given VREF minibank is configured as a VREF pin, the remaining I/Os in that minibank will be able to use that reference voltage.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications (e.g., PCI 66 MHz, bidirectional SSTL 2 and 3, Class I and II)
- Double-Data-Rate applications (e.g., DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications, and DDR 200 MHz SRAM using bidirectional HSTL Class II)

ProASIC3E banks support M-LVDS with 20 multi-drop points.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

- Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.
 - 1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
 - From the FlashPro GUI, click PDB Configuration. A FlashPoint Programming File Generator window appears.
 - 3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
 - 4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-3 on page 1-7).
 - Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

1 - I/O is set to drive out logic High

0 - I/O is set to drive out logic Low

Last Known State - I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

Z -Tri-State: I/O is tristated



ProASIC3E DC and Switching Characteristics

Combinatorial Cells Contribution—P_{C-CELL}

 $P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

 α_{1} is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-11 on page 2-11.

 $\mathsf{F}_{\mathsf{CLK}}$ is the global clock signal frequency.

Routing Net Contribution—P_{NET}

 $P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

 $N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

 α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-11 on page 2-11.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—PINPUTS

 $P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

 α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-11 on page 2-11.

 F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—POUTPUTS

 $P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$

 $N_{\mbox{OUTPUTS}}$ is the number of I/O output buffers used in the design.

 α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-11 on page 2-11.

 β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-12 on page 2-11.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

 $\mathsf{P}_{\mathsf{MEMORY}} = \mathsf{PAC11} * \mathsf{N}_{\mathsf{BLOCKS}} * \mathsf{F}_{\mathsf{READ-CLOCK}} * \beta_2 + \mathsf{PAC12} * \mathsf{N}_{\mathsf{BLOCK}} * \mathsf{F}_{\mathsf{WRITE-CLOCK}} * \beta_3$

 $N_{\mbox{\scriptsize BLOCKS}}$ is the number of RAM blocks used in the design.

F_{READ-CLOCK} is the memory read clock frequency.

 β_2 is the RAM enable rate for read operations—guidelines are provided in Table 2-12 on page 2-11.

F_{WRITE-CLOCK} is the memory write clock frequency.

 β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-12 on page 2-11.

PLL Contribution—P_{PLL}

P_{PLL} = PAC13 + PAC14 * F_{CLKOUT}

F_{CLKOUT} is the output clock frequency.¹

The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution (PAC14 * F_{CLKOUT} product) to the total PLL contribution.

Table 2-22	 Duration o 	f Short Ci	cuit Event	Before	Failure	(continued)
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Temperature	Time before Failure
85°C	2 years
100°C	6 months

Table 2-23 • Schmitt Trigger Input Hysteresis

Hysteresis Voltage Value (typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

Table 2-24 • I/O Input Rise Time, Fall Time, and Related I/O Reliability*

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns *	20 years (110°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis.	20 years (110°C)
HSTL/SSTL/GTL	No requirement	10 ns *	10 years (100°C)
LVDS/B-LVDS/M-LVDS/ LVPECL	No requirement	10 ns *	10 years (100°C)

Note: *For clock signals and similar edge-generating signals, refer to the "ProASIC3/E SSO and Pin Placement Guidelines" chapter of the ProASIC3E FPGA Fabric User's Guide. The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

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ProASIC3E DC and Switching Characteristics

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{zLS}	t _{zHS}	Units
12 mA	Std.	0.66	6.03	0.04	1.20	1.57	0.43	6.14	5.02	3.28	3.47	8.37	7.26	ns
	-1	0.56	5.13	0.04	1.02	1.33	0.36	5.22	4.27	2.79	2.95	7.12	6.17	ns
	-2	0.49	4.50	0.03	0.90	1.17	0.32	4.58	3.75	2.45	2.59	6.25	5.42	ns
16 mA	Std.	0.66	5.62	0.04	1.20	1.57	0.43	5.72	4.72	3.32	3.58	7.96	6.96	ns
	-1	0.56	4.78	0.04	1.02	1.33	0.36	4.87	4.02	2.83	3.04	6.77	5.92	ns
	-2	0.49	4.20	0.03	0.90	1.17	0.32	4.27	3.53	2.48	2.67	5.94	5.20	ns
24 mA	Std.	0.66	5.24	0.04	1.20	1.57	0.43	5.34	4.69	3.39	3.96	7.58	6.93	ns
	-1	0.56	4.46	0.04	1.02	1.33	0.36	4.54	3.99	2.88	3.37	6.44	5.89	ns
	-2	0.49	3.92	0.03	0.90	1.17	0.32	3.99	3.50	2.53	2.96	5.66	5.17	ns

Table 2-28 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

ProASIC3E DC and Switching Characteristics

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

2.5 V LVCMOS	v	ΊL	VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max., V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
4 mA	-0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
8 mA	-0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	-0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	-0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	-0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10

Table 2-33 • Minimum and Maximum DC Input and Output Levels

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.

Test Point
Datapath
$$\xrightarrow{1}{1}$$
 35 pF
 $R = 1 k$
Test Point
Enable Path $\xrightarrow{1}{1}$ R to VCCI for $t_{LZ} / t_{ZL} / t_{ZLS}$
R to GND for $t_{HZ} / t_{ZH} / t_{ZHS}$
 $35 pF$ for $t_{ZH} / t_{ZHS} / t_{ZL} / t_{ZLS}$
 $35 pF$ for $t_{HZ} / t_{ZH} / t_{ZLS}$

Figure 2-8 • AC Loading

Table 2-34 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)	
0	2.5	1.2	_	35	

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

ProASIC3E DC and Switching Characteristics

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-51 • Minimum and Maximum DC Input and Output Levels

2.5 GTL		VIL	VIH		VOL	VOH	IOL	ЮН	IOSL	IOSH	IIL	IIH
Drive Strength	Min., V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA²	μA²
20 mA ³	-0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	_	20	20	124	169	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

2. Currents are measured at 85°C junction temperature.

3. Output drive strength is below JEDEC specification.



Figure 2-13 • AC Loading

Table 2-52 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.05	VREF + 0.05	0.8	0.8	1.2	10

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-53 • 2.5 V GTL

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V VREF = 0.8 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.60	2.13	0.04	2.46	0.43	2.16	2.13			4.40	4.36	ns
-1	0.51	1.81	0.04	2.09	0.36	1.84	1.81			3.74	3.71	ns
-2	0.45	1.59	0.03	1.83	0.32	1.61	1.59			3.28	3.26	ns

ProASIC3E DC and Switching Characteristics

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

HSTL Class II	VIL		VIH		VOL	VOH	IOL	ЮН	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max., V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA²	μA²
15 mA ³	-0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15	55	66	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

2. Currents are measured at 85°C junction temperature.

3. Output drive strength is below JEDEC specification.



Figure 2-17 • AC Loading

Table 2-64 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-65 • HSTL Class II

Commercial-Case Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V, VREF = 0.75 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.66	3.02	0.04	2.12	0.43	3.08	2.71			5.32	4.95	ns
–1	0.56	2.57	0.04	1.81	0.36	2.62	2.31			4.52	4.21	ns
-2	0.49	2.26	0.03	1.59	0.32	2.30	2.03			3.97	3.70	ns

SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-72 • Minimum and Maximum	DC Input and Output Levels
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SSTL3 Class I		VIL	VIH		VOL	VOH	IOL	ЮН	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA²	μA²
14 mA	-0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14	54	51	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

2. Currents are measured at 85°C junction temperature.



Figure 2-20 • AC Loading

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-74 • SSTL3 Class I

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Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.5 V
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Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.66	2.31	0.04	1.25	0.43	2.35	1.84			4.59	4.07	ns
-1	0.56	1.96	0.04	1.06	0.36	2.00	1.56			3.90	3.46	ns
-2	0.49	1.72	0.03	0.93	0.32	1.75	1.37			3.42	3.04	ns

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by the Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and DDR. However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-22. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3E also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).



Figure 2-22 • LVDS Circuit Diagram and Board-Level Implementation

Timing Characteristics

Table 2-80 • LVDS

Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Speed Grade	t _{DOUT} t _{DP}		t _{DIN}	t _{PY}	Units
Std.	0.66	1.87	0.04	1.82	ns
-1	0.56	1.59	0.04	1.55	ns
-2	0.49	1.40	0.03	1.36	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-23. The input and output buffer delays are available in the LVDS section in Table 2-80.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: $R_S = 60 \Omega$ and $R_T = 70 \Omega$, given $Z_0 = 50 \Omega$ (2") and $Z_{stub} = 50 \Omega$ (~1.5").



Figure 2-23 • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers





Figure 2-29 • Output Enable Register Timing Diagram

Timing Characteristics

Table 2-88 • Output Enable Register Propagation DelaysCommercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{OECLKQ}	Clock-to-Q of the Output Enable Register	0.59	0.67	0.79	ns
t _{OESUD}	Data Setup Time for the Output Enable Register	0.31	0.36	0.42	ns
t _{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	0.00	ns
t _{OESUE}	Enable Setup Time for the Output Enable Register	0.44	0.50	0.58	ns
t _{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	0.00	ns
t _{OECLR2Q}	Asynchronous Clear-to-Q of the Output Enable Register	0.67	0.76	0.89	ns
t _{OEPRE2Q}	Asynchronous Preset-to-Q of the Output Enable Register	0.67	0.76	0.89	ns
t _{OEREMCLR}	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
t _{OERECCLR}	Asynchronous Clear Recovery Time for the Output Enable Register	0.22	0.25	0.30	ns
t _{OEREMPRE}	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
t _{OERECPRE}	Asynchronous Preset Recovery Time for the Output Enable Register	0.22	0.25	0.30	ns
t _{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
t _{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
t _{OECKMPWH}	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.41	0.48	ns
t _{OECKMPWL}	Clock Minimum Pulse Width Low for the Output Enable Register	0.32	0.37	0.43	ns





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riyure	2-33 -	Output	DDK	rinning	Diagram

Timing Characteristics

Table 2-92 • Output DDR Propagation DelaysCommercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{DDROCLKQ}	Clock-to-Out of DDR for Output DDR	0.70	0.80	0.94	ns
t _{DDROSUD1}	Data_F Data Setup for Output DDR	0.38	0.43	0.51	ns
t _{DDROSUD2}	Data_R Data Setup for Output DDR	0.38	0.43	0.51	ns
t _{DDROHD1}	Data_F Data Hold for Output DDR	0.00	0.00	0.00	ns
t _{DDROHD2}	Data_R Data Hold for Output DDR	0.00	0.00	0.00	ns
t _{DDROCLR2Q}	Asynchronous Clear-to-Out for Output DDR	0.80	0.91	1.07	ns
t _{DDROREMCLR}	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	0.00	ns
t _{DDRORECCLR}	Asynchronous Clear Recovery Time for Output DDR	0.22	0.25	0.30	ns
t _{DDROWCLR1}	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	0.25	0.30	ns
t _{DDROCKMPWH}	Clock Minimum Pulse Width High for the Output DDR	0.36	0.41	0.48	ns
t _{DDROCKMPWL}	Clock Minimum Pulse Width Low for the Output DDR	0.32	0.37	0.43	ns
F _{DDOMAX}	Maximum Frequency for the Output DDR	1404	1232	1048	MHz



ProASIC3E DC and Switching Characteristics

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-98 • ProASIC3E CCC/PLL Specification

Parameter	Minimum	Typical	Maximum	Units	
Clock Conditioning Circuitry Input Frequency fIN_CCC	1.5		350	MHz	
Clock Conditioning Circuitry Output Frequency f _{OUT_CCC}	0.75		350	MHz	
Delay Increments in Programmable Delay Blocks ^{1, 2}		160 ³		ps	
Serial Clock (SCLK) for Dynamic PLL ⁴			125	MHz	
Number of Programmable Values in Each Programmable Delay Block			32		
Input Period Jitter			1.5	ns	
CCC Output Peak-to-Peak Period Jitter F _{CCC_OUT}	_OUT Max Peak-to-Peak Period Jitter				
	1 Global Network Used		3 Global Networks Used		
0.75 MHz to 24 MHz	0.50%		0.70%		
24 MHz to 100 MHz	1.00%		1.20%		
100 MHz to 250 MHz	1.75%		2.00%		
250 MHz to 350 MHz	2.50%		5.60%		
Acquisition Time LockControl = 0			300	μs	
LockControl = 1			6.0	ms	
Tracking Jitter ⁵ LockControl = 0			1.6	ns	
LockControl = 1			0.8	ns	
Output Duty Cycle	Outy Cycle 48.5 51.5		51.5	%	
Delay Range in Block: Programmable Delay 1 ^{1, 2}	0.6		5.56 n:		
Delay Range in Block: Programmable Delay 2 ^{1,2}	Delay Range in Block: Programmable Delay 2 ^{1,2} 0.025 5.56		5.56	ns	
Delay Range in Block: Fixed Delay ^{1,4}		2.2		ns	

Notes:

1. This delay is a function of voltage and temperature. See Table 2-6 on page 2-5 for deratings

2. $T_J = 25^{\circ}C$, VCC = 1.5 V.

3. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help for more information.

4. Maximum value obtained for a -2 speed-grade device in worst-case commercial conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

5. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.

ProASIC3E DC and Switching Characteristics

Timing Characteristics

Table 2-99 • RAM4K9

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{AS}	Address setup time	0.25	0.28	0.33	ns
t _{AH}	Address hold time	0.00	0.00	0.00	ns
t _{ENS}	REN, WEN setup time	0.14	0.16	0.19	ns
t _{ENH}	REN, WEN hold time	0.10	0.11	0.13	ns
t _{BKS}	BLK setup time	0.23	0.27	0.31	ns
t _{BKH}	BLK hold time	0.02	0.02	0.02	ns
t _{DS}	Input data (DIN) setup time	0.18	0.21	0.25	ns
t _{DH}	Input data (DIN) hold time	0.00	0.00	0.00	ns
t _{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	1.79	2.03	2.39	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.36	2.68	3.15	ns
t _{CKQ2}	Clock High to new data valid on DOUT (pipelined)	0.89	1.02	1.20	ns
t _{C2CWWL} 1	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Closing Edge	0.33	0.28	0.25	ns
t _{C2CWWH} 1	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge	0.30	0.26	0.23	ns
t _{C2CRWH} 1	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.45	0.38	0.34	ns
t _{C2CWRH} 1	Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge		0.42	0.37	ns
t _{RSTBQ}	RESET Low to data out Low on DO (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on DO (pipelined)	0.92	1.05	1.23	ns
t _{REMRSTB}	RESET removal	0.29	0.33	0.38	ns
t _{RECRSTB}	RESET recovery	1.50	1.71	2.01	ns
t _{MPWRSTB}	RESET minimum pulse width	0.21	0.24	0.29	ns
t _{CYC}	Clock cycle time	3.23	3.68	4.32	ns
F _{MAX}	Maximum frequency	310	272	231	MHz

Notes:

1. For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.

Package Pin Assignments

	FG484		FG484	FG484	
Pin Number	A3PE600 Function	Pin Number	A3PE600 Function	Pin Number	A3PE600 Function
C21	NC	E13	IO24NDB1V0	G5	IO129PDB7V1
C22	VCCIB2	E14	IO24PDB1V0	G6	GAC2/IO132PDB7V1
D1	NC	E15	GBC1/IO33PDB1V1	G7	VCOMPLA
D2	NC	E16	GBB0/IO34NDB1V1	G8	GNDQ
D3	NC	E17	GNDQ	G9	IO09NDB0V1
D4	GND	E18	GBA2/IO36PDB2V0	G10	IO09PDB0V1
D5	GAA0/IO00NDB0V0	E19	IO42NDB2V0	G11	IO13PDB0V2
D6	GAA1/IO00PDB0V0	E20	GND	G12	IO21PDB1V0
D7	GAB0/IO01NDB0V0	E21	NC	G13	IO25PDB1V0
D8	IO05PDB0V0	E22	NC	G14	IO27NDB1V0
D9	IO10PDB0V1	F1	NC	G15	GNDQ
D10	IO12PDB0V2	F2	IO131NDB7V1	G16	VCOMPLB
D11	IO16NDB0V2	F3	IO131PDB7V1	G17	GBB2/IO37PDB2V0
D12	IO23NDB1V0	F4	IO133NDB7V1	G18	IO39PDB2V0
D13	IO23PDB1V0	F5	IO134NDB7V1	G19	IO39NDB2V0
D14	IO28NDB1V1	F6	VMV7	G20	IO43PDB2V0
D15	IO28PDB1V1	F7	VCCPLA	G21	IO43NDB2V0
D16	GBB1/IO34PDB1V1	F8	GAC0/IO02NDB0V0	G22	NC
D17	GBA0/IO35NDB1V1	F9	GAC1/IO02PDB0V0	H1	NC
D18	GBA1/IO35PDB1V1	F10	IO15NDB0V2	H2	NC
D19	GND	F11	IO15PDB0V2	H3	VCC
D20	NC	F12	IO20PDB1V0	H4	IO128NDB7V1
D21	NC	F13	IO25NDB1V0	H5	IO129NDB7V1
D22	NC	F14	IO27PDB1V0	H6	IO132NDB7V1
E1	NC	F15	GBC0/IO33NDB1V1	H7	IO130PDB7V1
E2	NC	F16	VCCPLB	H8	VMV0
E3	GND	F17	VMV2	H9	VCCIB0
E4	GAB2/IO133PDB7V1	F18	IO36NDB2V0	H10	VCCIB0
E5	GAA2/IO134PDB7V1	F19	IO42PDB2V0	H11	IO13NDB0V2
E6	GNDQ	F20	NC	H12	IO21NDB1V0
E7	GAB1/IO01PDB0V0	F21	NC	H13	VCCIB1
E8	IO05NDB0V0	F22	NC	H14	VCCIB1
E9	IO10NDB0V1	G1	IO127NDB7V1	H15	VMV1
E10	IO12NDB0V2	G2	IO127PDB7V1	H16	GBC2/IO38PDB2V0
E11	IO16PDB0V2	G3	NC	H17	IO37NDB2V0
E12	IO20NDB1V0	G4	IO128PDB7V1	H18	IO41NDB2V0



FG676



Note

For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/products/fpga-soc/solutions*.

	FG676	
Pin Number	A3PE1500 Function	Pin N
A1	GND	AA
A2	GND	AA
A3	GAA0/IO00NDB0V0	AA
A4	GAA1/IO00PDB0V0	AA
A5	IO06NDB0V0	AA
A6	IO09NDB0V1	AA
A7	IO09PDB0V1	AA
A8	IO14NDB0V1	AA
A9	IO14PDB0V1	AA
A10	IO22NDB0V2	AA
A11	IO22PDB0V2	AA
A12	IO26NDB0V3	AA
A13	IO26PDB0V3	AA
A14	IO30NDB0V3	AA
A15	IO30PDB0V3	AA
A16	IO34NDB1V0	AA
A17	IO34PDB1V0	A
A18	IO38NDB1V0	A
A19	IO38PDB1V0	A
A20	IO41PDB1V1	A
A21	IO44PDB1V1	A
A22	IO49PDB1V2	A
A23	IO50PDB1V2	A
A24	GBC1/IO55PDB1V3	A
A25	GND	A
A26	GND	AE
AA1	IO174PDB6V0	A
AA2	IO171PDB6V0	AE
AA3	GEA1/IO167PPB6V0	AE
AA4	GEC0/IO169NPB6V0	AE
AA5	VCOMPLE	AE
AA6	GND	AE
AA7	IO165NDB5V3	AE
AA8	GEB2/IO165PDB5V3	AE
AA9	IO163PDB5V3	AE
AA10	IO159NDB5V3	AE

FG676				
Pin Number	A3PE1500 Function			
AA11	IO153NDB5V2			
AA12	IO147NDB5V1			
AA13	IO139NDB5V0			
AA14	IO137NDB5V0			
AA15	IO123NDB4V1			
AA16	IO123PDB4V1			
AA17	IO117NDB4V0			
AA18	IO117PDB4V0			
AA19	GDB2/IO112PDB4V0			
AA20	GNDQ			
AA21	TDO			
AA22	GND			
AA23	GND			
AA24	IO102NDB3V1			
AA25	IO102PDB3V1			
AA26	IO98NDB3V1			
AB1	IO174NDB6V0			
AB2	IO171NDB6V0			
AB3	GEB1/IO168PPB6V0			
AB4	GEA0/IO167NPB6V0			
AB5	VCCPLE			
AB6	GND			
AB7	GND			
AB8	IO156NDB5V2			
AB9	IO156PDB5V2			
AB10	IO150PDB5V1			
AB11	IO155PDB5V2			
AB12	IO142PDB5V0			
AB13	IO135NDB5V0			
AB14	IO135PDB5V0			
AB15	IO132PDB4V2			
AB16	IO129PDB4V2			
AB17	IO121PDB4V1			
AB18	IO119NDB4V1			
AB19	IO112NDB4V0			
AB20	VMV4			

FG676				
Pin Number	A3PE1500 Function			
AB21	TCK			
AB22	TRST			
AB23	GDC0/IO108NDB3V2			
AB24	GDC1/IO108PDB3V2			
AB25	IO104NDB3V2			
AB26	IO104PDB3V2			
AC1	IO170PDB6V0			
AC2	GEB0/IO168NPB6V0			
AC3	IO166NPB5V3			
AC4	GNDQ			
AC5	GND			
AC6	IO160PDB5V3			
AC7	IO161PDB5V3			
AC8	IO154PDB5V2			
AC9	GND			
AC10	IO150NDB5V1			
AC11	IO155NDB5V2			
AC12	IO142NDB5V0			
AC13	IO138NDB5V0			
AC14	IO138PDB5V0			
AC15	IO132NDB4V2			
AC16	IO129NDB4V2			
AC17	IO121NDB4V1			
AC18	IO119PDB4V1			
AC19	IO118NDB4V0			
AC20	IO118PDB4V0			
AC21	IO114PPB4V0			
AC22	TMS			
AC23	VJTAG			
AC24	VMV3			
AC25	IO106NDB3V2			
AC26	IO106PDB3V2			
AD1	IO170NDB6V0			
AD2	GEA2/IO166PPB5V3			
AD3	VMV5			
AD4	GEC2/IO164PDB5V3			



Datasheet Information

Revision	Changes	Page
Revision 10 (continued)	"TBD" for 3.3 V LVCMOS Wide Range in Table 2-19 • I/O Output Buffer Maximum Resistances ¹ and Table 2-21 • I/O Short Currents IOSH/IOSL was replaced by "Same as regular 3.3 V LVCMOS" (SAR 33853).	2-20, 2-27
	3.3 V LVCMOS Wide Range information was separated from regular 3.3 V LVCMOS and placed into its own new section, "3.3 V LVCMOS Wide Range". Values of IOSH and IOSL were added in Table 2-29 • Minimum and Maximum DC Input and Output Levels (SAR 33853).	
	The formulas in the table notes for Table 2-20 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 34755).	2-21
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34889).	2-24
	The titles and subtitles for Table 2-31 • 3.3 V LVCMOS Wide Range High Slew and Table 2-32 • 3.3 V LVCMOS Wide Range Low Slew were corrected (SAR 37227).	2-28, 2-29
	The following notes were removed from Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels (SAR 34812): ±5%	2-50
	Differential input voltage = ±350 mV	
	Minimum pulse width High and Low values were added to the tables in the "Global Tree Timing Characteristics" section. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 36957).	2-68
	A note was added to Table 2-98 • ProASIC3E CCC/PLL Specification indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34824).	2-70
	The following figures were deleted. Reference was made to a new application note, <i>Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs</i> , which covers these cases in detail (SAR 34872).	2-74, 2-75, 2-79,
	Figure 2-44 • Write Access after Write onto Same Address	2-82
	Figure 2-45 • Read Access after Write onto Same Address	
	Figure 2-46 • Write Access after Read onto Same Address	
	Characteristics" tables, Figure 2-49 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35750).	
	The "Pin Descriptions and Packaging" chapter is new (SAR 34771).	3-1
	Package names used in the "Package Pin Assignments" section were revised to match standards given in <i>Package Mechanical Drawings</i> (SAR 34771).	4-1
	Pin E6 for the FG256 package was corrected from VvB0 to VCCIB0 (SARs 30364, 31597, 26243).	4-9
July 2010	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "ProASIC3E Device Status" table on page II indicates the status for each device in the device family.	N/A



Datasheet Information

Revision	Changes	Page
v2.0 (continued)	Table 3-6 • Temperature and Voltage Derating Factors for Timing Delays wasupdated.	3-5
	Table 3-5 • Package Thermal Resistivities was updated.	3-5
	Table 3-10 • Different Components Contributing to the Dynamic PowerConsumption in ProASIC3E Devices was updated.	3-8
	t_{WRO} and t_{CCKH} were added to Table 3-94 \bullet RAM4K9 and Table 3-95 \bullet RAM512X18.	3-74 to 3-74
	The note in Table 3-24 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was updated.	3-23
	Figure 3-43 • Write Access After Write onto Same Address, Figure 3-44 • Read Access After Write onto Same Address, and Figure 3-45 • Write Access After Read onto Same Address are new.	3-71 to 3- 73
	Figure 3-53 • Timing Diagram was updated.	3-80
	Notes were added to the package diagrams identifying if they were top or bottom view.	N/A
	The A3PE1500 "208-Pin PQFP" table is new.	4-4
	The A3PE1500 "484-Pin FBGA" table is new.	4-18
	The A3PE1500 "A3PE1500 Function" table is new.	4-24
Advance v0.6 (January 2007)	In the "Packaging Tables" table, the number of I/Os for the A3PE1500 was changed for the FG484 and FG676 packages.	ii
Advance v0.5 (April 2006)	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	Figure 2-8 • Very-Long-Line Resources was updated.	2-8
	The footnotes in Figure 2-27 • CCC/PLL Macro were updated.	2-28
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options.	2-24
	The "SRAM and FIFO" section was updated.	2-21
	The "RESET" section was updated.	2-25
	The "WCLK and RCLK" section was updated.	2-25
	The "RESET" section was updated.	2-25
	The "RESET" section was updated.	2-27
	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	Figure 2-8 • Very-Long-Line Resources was updated.	2-8
	The footnotes in Figure 2-27 • CCC/PLL Macro were updated.	2-28
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options.	2-24
	The "SRAM and FIFO" section was updated.	2-21
	The "RESET" section was updated.	2-25
	The "WCLK and RCLK" section was updated.	2-25