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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	
Total RAM Bits	516096
Number of I/O	620
Number of Gates	300000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3pe3000-fgg896

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Thermal Characteristics

Introduction

The temperature variable in Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

 T_J = Junction Temperature = $\Delta T + T_A$

where:

T_A = Ambient Temperature

 ΔT = Temperature gradient between junction (silicon) and ambient ΔT = θ_{ia} * P

 θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja} . The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 110°C. EQ 2 shows a sample calculation of the absolute maximum power dissipation allowed for an 896-pin FBGA package at commercial temperature and in still air.

Maximum Power Allowed =
$$\frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(°C/W)} = \frac{110°C - 70°C}{13.6°C/W} = 5.88 \text{ W}$$

Package Type	Pin Count	θ_{jc}	Still Air	200 ft./min.	500 ft./min.	Units
Plastic Quad Flat Package (PQFP)	208	8.0	26.1	22.5	20.8	C/W
Plastic Quad Flat Package (PQFP) with embedded heat spreader in A3PE3000	208	3.8	16.2	13.3	11.9	C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.9	22.8	21.5	C/W
	484	3.2	20.5	17.0	15.9	C/W
	676	3.2	16.4	13.0	12.0	C/W
	896	2.4	13.6	10.4	9.4	C/W

Table 2-5 • Package Thermal Resistivities

Temperature and Voltage Derating Factors

Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays
(normalized to $T_J = 70^{\circ}$ C, VCC = 1.425 V)

Array Voltage VCC (V)	Junction Temperature (°C)									
	–40°C	0°C	25°C	70°C	85°C	100°C				
1.425	0.87	0.92	0.95	1.00	1.02	1.04				
1.500	0.83	0.88	0.90	0.95	0.97	0.98				
1.575	0.80	0.85	0.87	0.92	0.93	0.95				

EQ 1

EQ 2

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- · The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-11 on page 2-11.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-12 on page 2-11.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-12 on page 2-11. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—PTOTAL

 $P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

P_{STAT} = PDC1 + N_{INPUTS} * PDC2 + N_{OUTPUTS} * PDC3

N_{INPUTS} is the number of I/O input buffers used in the design.

N_{OUTPUTS} is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption—P_{DYN}

P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}

Global Clock Contribution—P_{CLOCK}

P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S-CELL} * PAC4) * F_{CLK}

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3E FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3E FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

Sequential Cells Contribution—P_{S-CELL}

 P_{S-CELL} = N_{S-CELL} * (PAC5 + α_1 / 2 * PAC6) * F_{CLK}

 $N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

 α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-11 on page 2-11.

F_{CLK} is the global clock signal frequency.

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ProASIC3E DC and Switching Characteristics

User I/O Characteristics

Timing Model



Figure 2-2 • Timing Model Operating Conditions: –2 Speed, Commercial Temperature Range (T_J = 70°C), Worst-Case VCC = 1.425 V



ProASIC3E DC and Switching Characteristics

Table 2-21 • I/O Short Currents IOSH/IOSL

	Drive Strength	IOSH (mA)*	IOSL (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55

Notes:

- 1. $T_J = 100^{\circ}C$
- 2. Applicable to 3.3 V LVCMOS Wide Range. IOSL/IOSH dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-22 • Duration of Short Circuit Event Before Failure

Temperature	Time before Failure
-40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years

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ProASIC3E DC and Switching Characteristics

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTL support.

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VОН	IOL	юн	IOSL	IOSH	IIL¹	IIH ²
Drive Strength	Min. V	Max. V	Min., V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	-0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	-0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	-0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Table 2-25 • Minimum and Maximum DC Input and Output Levels

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V< VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN< VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.



Figure 2-6 • AC Loading

Table 2-26 • 3.3 V LVTTL / 3.3 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	3.3	1.4	-	35

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

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ProASIC3E DC and Switching Characteristics

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for generalpurpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	-0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10
6 mA	-0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	6	6	39	32	10	10
8 mA	-0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	8	8	55	66	10	10
12 mA	-0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12	55	66	10	10

Table 2-41 • Minimum and Maximum DC Input and Output Levels

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V< VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.

Test Point
Datapath
$$\downarrow$$
 35 pF
$$R = 1 k$$
Test Point
Enable Path \downarrow

$$R to VCCI for t_{LZ} / t_{ZL} / t_{ZLS}$$

$$R to GND for t_{HZ} / t_{ZH} / t_{ZHS} / t_{ZL} / t_{ZLS}$$

$$35 pF for t_{ZH} / t_{ZHS} / t_{ZL} / t_{ZLS}$$

Figure 2-10 • AC Loading

Table 2-42 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	1.5	0.75	_	35

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

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ProASIC3E DC and Switching Characteristics

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-57 • Minimum and Maximum DC Input and Output Levels

2.5 V GTL+	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA²	μA²
33 mA	-0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	_	33	33	124	169	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

2. Currents are measured at 85°C junction temperature.



Figure 2-15 • AC Loading

Table 2-58 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-59 • 2.5 V GTL+

```
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.0 V
```

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.60	2.21	0.04	1.51	0.43	2.25	2.10			4.48	4.34	ns
-1	0.51	1.88	0.04	1.29	0.36	1.91	1.79			3.81	3.69	ns
-2	0.45	1.65	0.03	1.13	0.32	1.68	1.57			3.35	3.24	ns

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

|--|

HSTL Class I V		VIL	VIH		VOL	VOH	IOL	ЮН	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA²	μA²
8 mA	-0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI - 0.4	8	8	39	32	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

2. Currents are measured at 85°C junction temperature.



Figure 2-16 • AC Loading

Table 2-61 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: **Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-62 • HSTL Class I

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = .4 V, VREF = 0.75 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.66	3.18	0.04	2.12	0.43	3.24	3.14			5.47	5.38	ns
-1	0.56	2.70	0.04	1.81	0.36	2.75	2.67			4.66	4.58	ns
-2	0.49	2.37	0.03	1.59	0.32	2.42	2.35			4.09	4.02	ns

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ProASIC3E DC and Switching Characteristics

Output Register





Timing Characteristics

Table 2-87 • Output Data Register Propagation DelaysCommercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{OCLKQ}	Clock-to-Q of the Output Data Register	0.59	0.67	0.79	ns
t _{OSUD}	Data Setup Time for the Output Data Register	0.31	0.36	0.42	ns
t _{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t _{OSUE}	Enable Setup Time for the Output Data Register	0.44	0.50	0.59	ns
t _{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t _{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.80	0.91	1.07	ns
t _{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.80	0.91	1.07	ns
t _{OREMCLR}	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	0.00	ns
t _{ORECCLR}	Asynchronous Clear Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
t _{OREMPRE}	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	0.00	ns
t _{ORECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
t _{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
t _{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
t _{OCKMPWH}	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.41	0.48	ns
t _{OCKMPWL}	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.37	0.43	ns





Eiguro	2 22 .	Autout	סחח	Timina	Diagram
Iguie	2-33 -	Output	אטט	rinning	Diagram

Timing Characteristics

Table 2-92 • Output DDR Propagation DelaysCommercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{DDROCLKQ}	Clock-to-Out of DDR for Output DDR	0.70	0.80	0.94	ns
t _{DDROSUD1}	Data_F Data Setup for Output DDR	0.38	0.43	0.51	ns
t _{DDROSUD2}	Data_R Data Setup for Output DDR	0.38	0.43	0.51	ns
t _{DDROHD1}	Data_F Data Hold for Output DDR	0.00	0.00	0.00	ns
t _{DDROHD2}	Data_R Data Hold for Output DDR	0.00	0.00	0.00	ns
t _{DDROCLR2Q}	Asynchronous Clear-to-Out for Output DDR	0.80	0.91	1.07	ns
t _{DDROREMCLR}	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	0.00	ns
t _{DDRORECCLR}	Asynchronous Clear Recovery Time for Output DDR	0.22	0.25	0.30	ns
t _{DDROWCLR1}	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	0.25	0.30	ns
t _{DDROCKMPWH}	Clock Minimum Pulse Width High for the Output DDR	0.36	0.41	0.48	ns
t _{DDROCKMPWL}	Clock Minimum Pulse Width Low for the Output DDR	0.32	0.37	0.43	ns
F _{DDOMAX}	Maximum Frequency for the Output DDR	1404	1232	1048	MHz



Figure 2-35 • Timing Model and Waveforms



Figure 2-50 • FIFO EMPTY Flag and AEMPTY Flag Assertion



4 – Package Pin Assignments

PQ208



Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *http://www.microsemi.com/products/fpga-soc/solutions*.



FG484					
Pin Number	A3PE600 Function				
V15	IO69NDB4V0				
V16	GDB2/IO69PDB4V0				
V17	TDI				
V18	GNDQ				
V19	TDO				
V20	GND				
V21	NC				
V22	IO63NDB3V1				
W1	NC				
W2	NC				
W3	NC				
W4	GND				
W5	IO100NDB5V2				
W6	GEB2/IO100PDB5V2				
W7	IO99NDB5V2				
W8	IO88NDB5V0				
W9	IO88PDB5V0				
W10	IO89NDB5V0				
W11	IO80NDB4V1				
W12	IO81NDB4V1				
W13	IO81PDB4V1				
W14	IO70NDB4V0				
W15	GDC2/IO70PDB4V0				
W16	IO68NDB4V0				
W17	GDA2/IO68PDB4V0				
W18	TMS				
W19	GND				
W20	NC				
W21	NC				
W22	NC				
Y1	VCCIB6				
Y2	NC				
Y3	NC				
Y4	IO98NDB5V2				
Y5	GND				
Y6	IO94NDB5V1				

FG484					
A3PE600 Function					
IO94PDB5V1					
VCC					
VCC					
IO89PDB5V0					
IO80PDB4V1					
IO78NPB4V1					
NC					
VCC					
VCC					
NC					
NC					
GND					
NC					
NC					
NC					
VCCIB3					

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Package Pin Assignments

	FG676		FG676	FG676	
Pin Number	A3PE1500 Function	Pin Number	A3PE1500 Function	Pin Number	A3PE1500 Function
G13	IO21NDB0V2	H23	IO69PDB2V1	K7	IO217NDB7V3
G14	IO27PDB0V3	H24	IO76PDB2V2	K8	VCCIB7
G15	IO35NDB1V0	H25	IO76NDB2V2	K9	VCC
G16	IO39PDB1V0	H26	IO78NDB2V2	K10	GND
G17	IO51NDB1V2	J1	IO197NDB7V0	K11	GND
G18	IO53NDB1V2	J2	IO197PDB7V0	K12	GND
G19	VCCIB1	J3	VMV7	K13	GND
G20	GBA2/IO58PPB2V0	J4	IO215NDB7V3	K14	GND
G21	GNDQ	J5	IO215PDB7V3	K15	GND
G22	IO64NDB2V1	J6	IO214PDB7V3	K16	GND
G23	IO64PDB2V1	J7	IO214NDB7V3	K17	GND
G24	IO72PDB2V2	J8	VCCIB7	K18	VCC
G25	IO72NDB2V2	J9	VCC	K19	VCCIB2
G26	IO78PDB2V2	J10	VCC	K20	IO65PDB2V1
H1	IO208NDB7V2	J11	VCC	K21	IO65NDB2V1
H2	IO208PDB7V2	J12	VCC	K22	IO74PDB2V2
H3	IO209NDB7V2	J13	VCC	K23	IO74NDB2V2
H4	IO209PDB7V2	J14	VCC	K24	IO75PDB2V2
H5	IO219NDB7V3	J15	VCC	K25	IO75NDB2V2
H6	GAC2/IO219PDB7V3	J16	VCC	K26	IO84PDB2V3
H7	VCCIB7	J17	VCC	L1	IO195NDB7V0
H8	VCC	J18	VCC	L2	IO198PPB7V0
H9	VCCIB0	J19	VCCIB2	L3	GNDQ
H10	VCCIB0	J20	IO62PDB2V0	L4	IO201PDB7V1
H11	VCCIB0	J21	IO62NDB2V0	L5	IO201NDB7V1
H12	VCCIB0	J22	IO70NDB2V1	L6	IO210NDB7V2
H13	VCCIB0	J23	IO69NDB2V1	L7	IO210PDB7V2
H14	VCCIB1	J24	VMV2	L8	VCCIB7
H15	VCCIB1	J25	IO80PDB2V3	L9	VCC
H16	VCCIB1	J26	IO80NDB2V3	L10	GND
H17	VCCIB1	K1	IO195PDB7V0	L11	GND
H18	VCCIB1	K2	IO199NDB7V1	L12	GND
H19	VCC	K3	IO199PDB7V1	L13	GND
H20	VCC	K4	IO205NDB7V1	L14	GND
H21	IO58NPB2V0	K5	IO205PDB7V1	L15	GND
H22	IO70PDB2V1	K6	IO217PDB7V3	L16	GND



FG676					
Pin Number	A3PE1500 Function				
W25	IO96PDB3V1				
W26	IO94NDB3V0				
Y1	IO175NDB6V1				
Y2	IO175PDB6V1				
Y3	IO173NDB6V0				
Y4	IO173PDB6V0				
Y5	GEC1/IO169PPB6V0				
Y6	GNDQ				
Y7	VMV6				
Y8	VCCIB5				
Y9	IO163NDB5V3				
Y10	IO159PDB5V3				
Y11	IO153PDB5V2				
Y12	IO147PDB5V1				
Y13	IO139PDB5V0				
Y14	IO137PDB5V0				
Y15	IO125NDB4V1				
Y16	IO125PDB4V1				
Y17	IO115NDB4V0				
Y18	IO115PDB4V0				
Y19	VCC				
Y20	VPUMP				
Y21	VCOMPLD				
Y22	VCCPLD				
Y23	IO100NDB3V1				
Y24	IO100PDB3V1				
Y25	IO96NDB3V1				
Y26	IO98PDB3V1				



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Revision	Changes	Page
Revision 10 (continued)	"TBD" for 3.3 V LVCMOS Wide Range in Table 2-19 • I/O Output Buffer Maximum Resistances ¹ and Table 2-21 • I/O Short Currents IOSH/IOSL was replaced by "Same as regular 3.3 V LVCMOS" (SAR 33853).	2-20, 2-27
	3.3 V LVCMOS Wide Range information was separated from regular 3.3 V LVCMOS and placed into its own new section, "3.3 V LVCMOS Wide Range". Values of IOSH and IOSL were added in Table 2-29 • Minimum and Maximum DC Input and Output Levels (SAR 33853).	
	The formulas in the table notes for Table 2-20 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 34755).	2-21
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34889).	2-24
	The titles and subtitles for Table 2-31 • 3.3 V LVCMOS Wide Range High Slew and Table 2-32 • 3.3 V LVCMOS Wide Range Low Slew were corrected (SAR 37227).	2-28, 2-29
	The following notes were removed from Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels (SAR 34812): ±5%	2-50
	Differential input voltage = ±350 mV	
	Minimum pulse width High and Low values were added to the tables in the "Global Tree Timing Characteristics" section. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 36957).	2-68
	A note was added to Table 2-98 • ProASIC3E CCC/PLL Specification indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34824).	2-70
	The following figures were deleted. Reference was made to a new application note, <i>Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs</i> , which covers these cases in detail (SAR 34872).	2-74, 2-75, 2-79,
	Figure 2-44 • Write Access after Write onto Same Address	2-82
	Figure 2-45 • Read Access after Write onto Same Address	
	Figure 2-46 • Write Access after Read onto Same Address	
	Characteristics" tables, Figure 2-49 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35750).	
	The "Pin Descriptions and Packaging" chapter is new (SAR 34771).	3-1
	Package names used in the "Package Pin Assignments" section were revised to match standards given in <i>Package Mechanical Drawings</i> (SAR 34771).	4-1
	Pin E6 for the FG256 package was corrected from VvB0 to VCCIB0 (SARs 30364, 31597, 26243).	4-9
July 2010	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "ProASIC3E Device Status" table on page II indicates the status for each device in the device family.	N/A



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Revision	Changes	Page
Revision 3 (Apr 2008) Packaging v1.2	The following pins had duplicates and the extra pins were deleted from the "PQ208" A3PE3000 table:	4-2
	36, 62, 171	
	Note: There were no pin function changes in this update.	
	The following pins had duplicates and the extra pins were deleted from the "FG324" table:	4-12
	E2, E3, E16, E17, P2, P3, T16, U17	
	Note: There were no pin function changes in this update.	
	The "FG256" pin table was updated for the A3PE600 device because the old PAT were based on the IFX die, and this is the final UMC die version.	4-9
	The "FG484" was updated for the A3PE600 device because the old PAT were based on the IFX die, and this is the final UMC die version.	4-22
	The following pins had duplicates and the extra pins were deleted from the "FG896" table:	4-41
	AD6, AE5, AE28, AF29, F5, F26, G6, G25	
	Note: There were no pin function changes in this update.	
Revision 2 (Mar 2008) Product Brief rev. 1	The FG324 package was added to the "ProASIC3E Product Family" table, the "I/Os Per Package1" table, and the "Temperature Grade Offerings" table for A3PE3000.	I, II, IV
Revision 1 (Feb 2008) DC and Switching Characteristics v1.1	In Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature 1, Maximum Operating Junction Temperature was changed from 110°C to 100°C for both commercial and industrial grades.	2
	The "PLL Behavior at Brownout Condition" section is new.	2-4
	In the "PLL Contribution—PPLL" section, the following was deleted: FCLKIN is the input clock frequency.	2-10
	In Table 2-14 • Summary of Maximum and Minimum DC Input Levels, the note was incorrect. It previously said T_J and it was corrected and changed to T_A .	2-17
	In Table 2-98 • ProASIC3E CCC/PLL Specification, the SCLK parameter and note 1 are new.	2-70
	Table 2-103 • JTAG 1532 was populated with the parameter data, which was not in the previous version of the document.	2-83
Revision 1 (cont'd) Packaging v1.1	The "PQ208" pin table for A3PE3000 was updated.	4-2
	The "FG324" pin table for A3PE3000 is new.	4-13
	The "FG484" pin table for A3PE3000 is new.	4-17
	The "FG896" pin table for A3PE3000 is new.	4-41
Revision 0 (Jan 2008)	This document was previously in datasheet v2.1. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is 51700098-001-0.	N/A
v2.1 (July 2007)	CoreMP7 information was removed from the "Features and Benefits" section.	1-1
	The M1 device part numbers have been updated in ProASIC3E Product Family, "Packaging Tables", "Temperature Grade Offerings", "Speed Grade and Temperature Grade Matrix", and "Speed Grade and Temperature Grade Matrix".	1-1



Datasheet Information

Revision	Changes	Page
v2.0 (continued)	Table 3-6 • Temperature and Voltage Derating Factors for Timing Delays wasupdated.	3-5
	Table 3-5 • Package Thermal Resistivities was updated.	3-5
	Table 3-10 • Different Components Contributing to the Dynamic PowerConsumption in ProASIC3E Devices was updated.	3-8
	$t_{\rm WRO}$ and $t_{\rm CCKH}$ were added to Table 3-94 \bullet RAM4K9 and Table 3-95 \bullet RAM512X18.	3-74 to 3-74
	The note in Table 3-24 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was updated.	3-23
	Figure 3-43 • Write Access After Write onto Same Address, Figure 3-44 • Read Access After Write onto Same Address, and Figure 3-45 • Write Access After Read onto Same Address are new.	3-71 to 3- 73
	Figure 3-53 • Timing Diagram was updated.	3-80
	Notes were added to the package diagrams identifying if they were top or bottom view.	N/A
	The A3PE1500 "208-Pin PQFP" table is new.	4-4
	The A3PE1500 "484-Pin FBGA" table is new.	4-18
	The A3PE1500 "A3PE1500 Function" table is new.	4-24
Advance v0.6 (January 2007)	In the "Packaging Tables" table, the number of I/Os for the A3PE1500 was changed for the FG484 and FG676 packages.	ii
Advance v0.5 (April 2006)	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	Figure 2-8 • Very-Long-Line Resources was updated.	2-8
	The footnotes in Figure 2-27 • CCC/PLL Macro were updated.	2-28
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options.	2-24
	The "SRAM and FIFO" section was updated.	2-21
	The "RESET" section was updated.	2-25
	The "WCLK and RCLK" section was updated.	2-25
	The "RESET" section was updated.	2-25
	The "RESET" section was updated.	2-27
	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	Figure 2-8 • Very-Long-Line Resources was updated.	2-8
	The footnotes in Figure 2-27 • CCC/PLL Macro were updated.	2-28
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options.	2-24
	The "SRAM and FIFO" section was updated.	2-21
	The "RESET" section was updated.	2-25
	The "WCLK and RCLK" section was updated.	2-25



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