Microchip Technology - M1A3PE3000-PQ208 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	516096
Number of I/O	147
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3pe3000-pq208

Advanced Architecture

The proprietary ProASIC3E architecture provides granularity comparable to standard-cell ASICs. The ProASIC3E device consists of five distinct and programmable architectural features (Figure 1-1 on page 3):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- Pro I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the ProASIC3E core tile as either a three-input lookup table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC family of third-generation architecture Flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

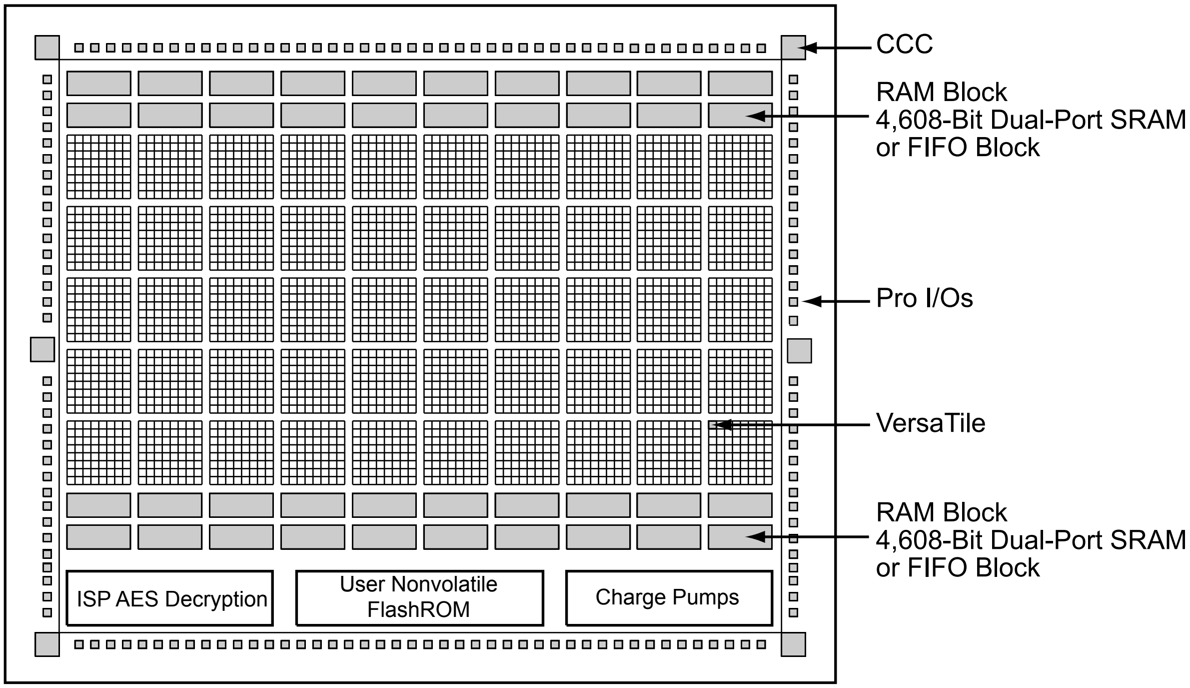


Figure 1-1 • **ProASIC3E Device Architecture Overview**

VersaTiles

The ProASIC3E core consists of VersaTiles, which have been enhanced beyond the ProASIC$^{\underline{PLUS}®}$ core tiles. The ProASIC3E VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-2 for VersaTile configurations.

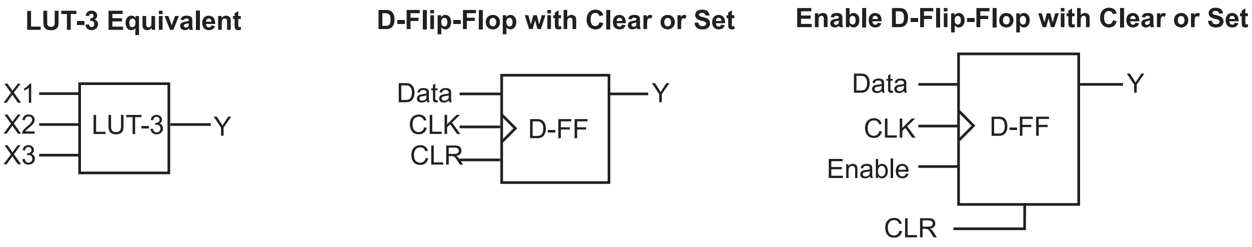


Figure 1-2 • **VersaTile Configurations**

User Nonvolatile FlashROM

ProASIC3E devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3E IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC3E development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

Table 2-4 • **Overshoot and Undershoot Limits** [1]

VCCI and VMV	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
3. *This table does not provide PCI overshoot/undershoot limits.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC®3E device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4.

There are five regions to consider during power-up.

ProASIC3E I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 on page 2-4).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI **Trip Point:**
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC **Trip Point:**
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLXL exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-1 on page 2-4 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *ProASIC3E FPGA Fabric User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

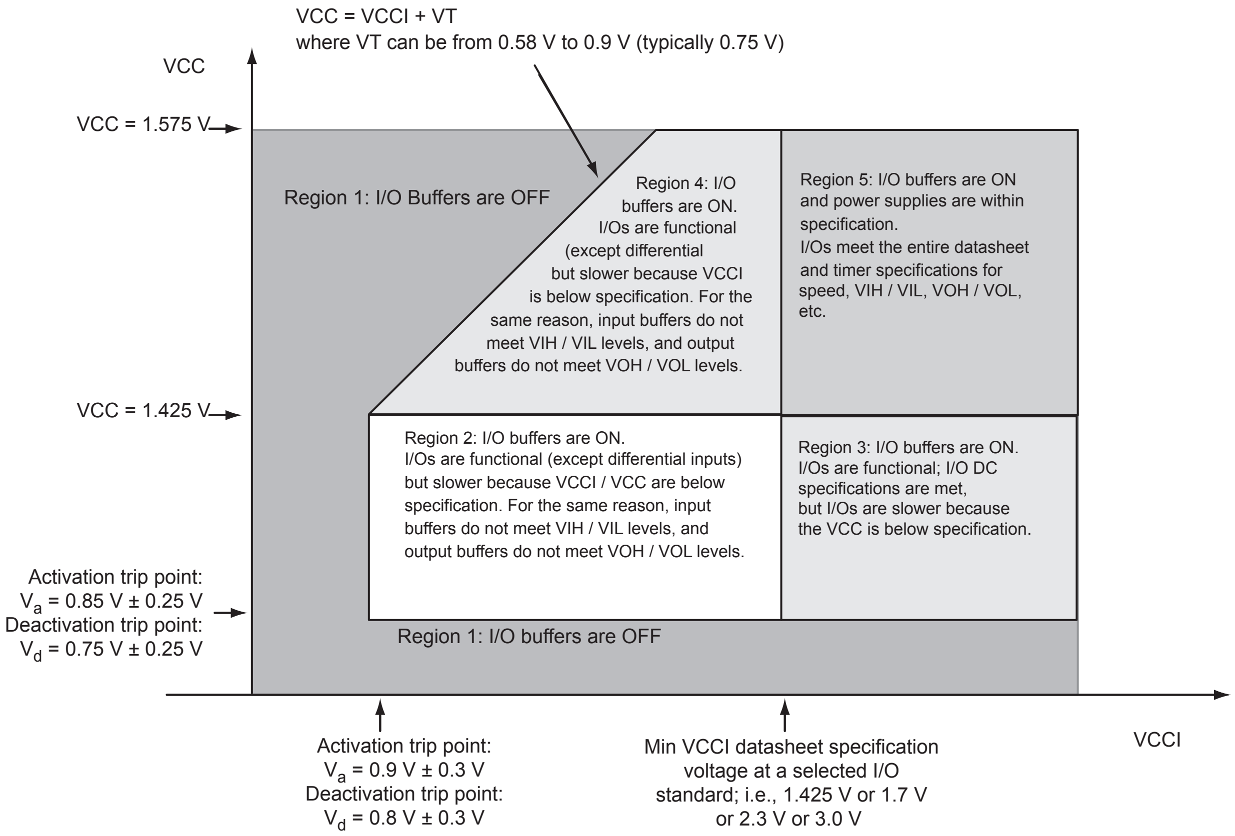


Figure 2-1 • **I/O State as a Function of VCCI and VCC Voltage Levels**

Table 2-9 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings (continued) (continued)[1]

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
SSTL3 (I)	30	3.3	26.02	114.87
SSTL3 (II)	30	3.3	42.21	131.76
Differential				
LVDS/B-LVDS/M-LVDS	–	2.5	7.70	89.62
LVPECL	–	3.3	19.42	168.02

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PDC3 is the static power (where applicable) measured on VCCI.*
3. *PAC10 is the total dynamic power measured on VCC and VCCI.*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

Power Consumption of Various Internal Resources

Table 2-10 • Different Components Contributing to the Dynamic Power Consumption in ProASIC3E Devices

Parameter	Definition	Device-Specific Dynamic Contributions (µW/MHz)		
		A3PE600	A3PE1500	A3PE3000
PAC1	Clock contribution of a Global Rib	12.77	16.21	19.7
PAC2	Clock contribution of a Global Spine	1.85	3.06	4.16
PAC3	Clock contribution of a VersaTile row	0.88		
PAC4	Clock contribution of a VersaTile used as a sequential module	0.12		
PAC5	First contribution of a VersaTile used as a sequential module	0.07		
PAC6	Second contribution of a VersaTile used as a sequential module	0.29		
PAC7	Contribution of a VersaTile used as a combinatorial module	0.29		
PAC8	Average contribution of a routing net	0.70		
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-8 on page 2-6.		
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-9 on page 2-7		
PAC11	Average contribution of a RAM block during a read operation	25.00		
PAC12	Average contribution of a RAM block during a write operation	30.00		
PAC13	Static PLL contribution	2.55 mW		
PAC14	Dynamic contribution for PLL	2.60		

Note: For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power calculator or SmartPower in Libero SoC.

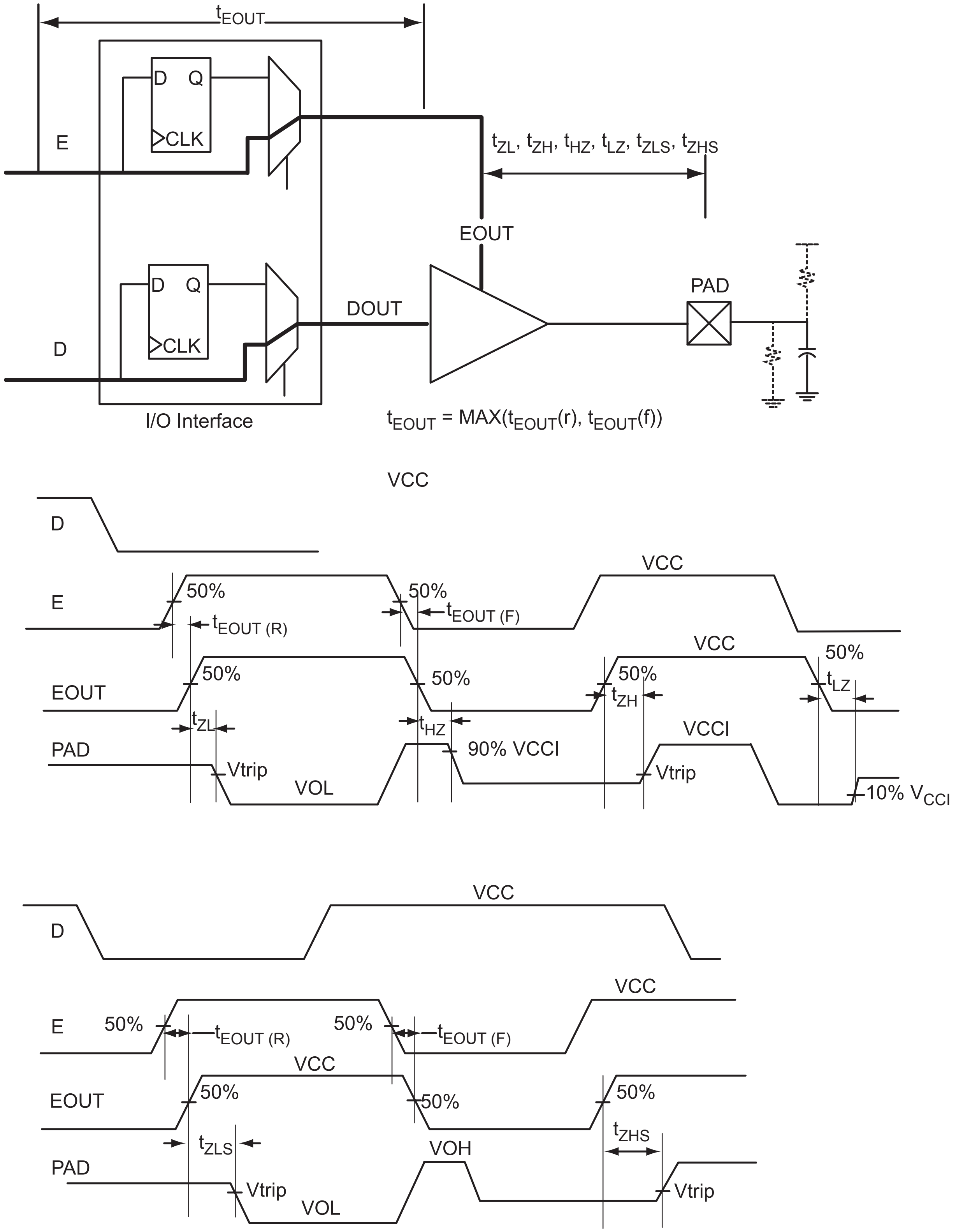


Figure 2-5 • **Tristate Output Buffer Timing Model and Delays (example)**

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-13 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions**

				VIL		VIH		VOL	VOH	IOL[3]	IOH[3]
I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[1]	Slew Rate	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range	100 µA	12 mA	High	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI Specification										
3.3 V PCI-X	Per PCI-X Specification										
3.3 V GTL	20 mA[2]	20 mA[2]	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
2.5 V GTL	20 mA[2]	20 mA[2]	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
3.3 V GTL+	35 mA	35 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35
2.5 V GTL+	33 mA	33 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33
HSTL (I)	8 mA	8 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8
HSTL (II)	15 mA[2]	15 mA[2]	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15
SSTL2 (I)	15 mA	15 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15
SSTL2 (II)	18 mA	18 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18
SSTL3 (I)	14 mA	14 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14
SSTL3 (II)	21 mA	21 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *Output drive strength is below JEDEC specification.*
3. *Currents are measured at 85°C junction temperature.*
4. *Output Slew Rates can be extracted from IBIS Models, located at http://www.microsemi.com/index.php?option=com_content&id=1671&lang=en&view=article.*

3.3 V LVCMOS Wide Range

Table 2-29 • **Minimum and Maximum DC Input and Output Levels**

3.3 V LVCMOS Wide Range	Equivalent Software Default Drive	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	**Strength Option[1]**	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**µA**	**µA**	**Max. mA[4]**	**Max. mA[4]**	**µA[5]**	**µA[5]**
100 µA	2 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	27	25	10	10
100 µA	4 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	27	25	10	10
100 µA	6 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	54	51	10	10
100 µA	8 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	54	51	10	10
100 µA	12 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	109	103	10	10
100 µA	16 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	127	132	10	10
100 µA	24 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	181	268	10	10

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN< VCCI. Input current is larger when operating outside recommended ranges.*
4. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

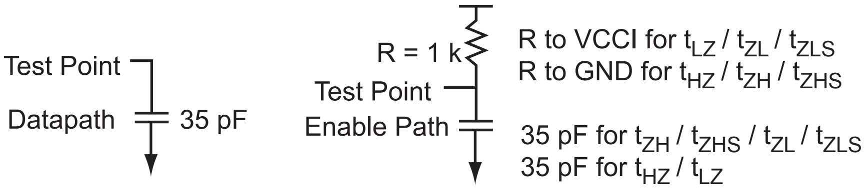


Figure 2-7 • **AC Loading**

Table 2-30 • **3.3 V LVCMOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	35

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

***Table 2-36* • 2.5 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	12.00	0.04	1.51	1.66	0.43	12.23	11.61	2.72	2.20	14.46	13.85	ns
	–1	0.56	10.21	0.04	1.29	1.41	0.36	10.40	9.88	2.31	1.87	12.30	11.78	ns
	–2	0.49	8.96	0.03	1.13	1.24	0.32	9.13	8.67	2.03	1.64	10.80	10.34	ns
8 mA	Std.	0.66	8.73	0.04	1.51	1.66	0.43	8.89	8.01	3.10	2.93	11.13	10.25	ns
	–1	0.56	7.43	0.04	1.29	1.41	0.36	7.57	6.82	2.64	2.49	9.47	8.72	ns
	–2	0.49	6.52	0.03	1.13	1.24	0.32	6.64	5.98	2.32	2.19	8.31	7.65	ns
12 mA	Std.	0.66	6.77	0.04	1.51	1.66	0.43	6.90	6.11	3.37	3.39	9.14	8.34	ns
	–1	0.56	5.76	0.04	1.29	1.41	0.36	5.87	5.20	2.86	2.89	7.77	7.10	ns
	–2	0.49	5.06	0.03	1.13	1.24	0.32	5.15	4.56	2.51	2.53	6.82	6.23	ns
16 mA	Std.	0.66	6.31	0.04	1.51	1.66	0.43	6.42	5.73	3.42	3.52	8.66	7.96	ns
	–1	0.56	5.37	0.04	1.29	1.41	0.36	5.46	4.87	2.91	3.00	7.37	6.77	ns
	–2	0.49	4.71	0.03	1.13	1.24	0.32	4.80	4.28	2.56	2.63	6.47	5.95	ns
24 mA	Std.	0.66	5.93	0.04	1.51	1.66	0.43	6.04	5.70	3.49	4.00	8.28	7.94	ns
	–1	0.56	5.05	0.04	1.29	1.41	0.36	5.14	4.85	2.97	3.40	7.04	6.75	ns
	–2	0.49	4.43	0.03	1.13	1.24	0.32	4.51	4.26	2.61	2.99	6.18	5.93	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Timing Characteristics

Table 2-43 • **1.5 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	8.53	0.04	1.70	2.14	0.43	7.26	8.53	3.39	2.79	9.50	10.77	ns
	–1	0.56	7.26	0.04	1.44	1.82	0.36	6.18	7.26	2.89	2.37	8.08	9.16	ns
	–2	0.49	6.37	0.03	1.27	1.60	0.32	5.42	6.37	2.53	2.08	7.09	8.04	ns
4 mA	Std.	0.66	5.41	0.04	1.70	2.14	0.43	5.22	5.41	3.75	3.48	7.45	7.65	ns
	–1	0.56	4.60	0.04	1.44	1.82	0.36	4.44	4.60	3.19	2.96	6.34	6.50	ns
	–2	0.49	4.04	0.03	1.27	1.60	0.32	3.89	4.04	2.80	2.60	5.56	5.71	ns
6 mA	Std.	0.66	4.80	0.04	1.70	2.14	0.43	4.89	4.75	3.83	3.67	7.13	6.98	ns
	–1	0.56	4.09	0.04	1.44	1.82	0.36	4.16	4.04	3.26	3.12	6.06	5.94	ns
	–2	0.49	3.59	0.03	1.27	1.60	0.32	3.65	3.54	2.86	2.74	5.32	5.21	ns
8 mA	Std.	0.66	4.42	0.04	1.70	2.14	0.43	4.50	3.62	3.96	4.37	6.74	5.86	ns
	–1	0.56	3.76	0.04	1.44	1.82	0.36	3.83	3.08	3.37	3.72	5.73	4.98	ns
	–2	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns
12 mA	Std.	0.66	4.42	0.04	1.70	2.14	0.43	4.50	3.62	3.96	4.37	6.74	5.86	ns
	–1	0.56	3.76	0.04	1.44	1.82	0.36	3.83	3.08	3.37	3.72	5.73	4.98	ns
	–2	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

Table 2-44 • **1.5 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	14.11	0.04	1.70	2.14	0.43	14.37	13.14	3.40	2.68	16.61	15.37	ns
	–1	0.56	12.00	0.04	1.44	1.82	0.36	12.22	11.17	2.90	2.28	14.13	13.08	ns
	–2	0.49	10.54	0.03	1.27	1.60	0.32	10.73	9.81	2.54	2.00	12.40	11.48	ns
4 mA	Std.	0.66	11.23	0.04	1.70	2.14	0.43	11.44	9.87	3.77	3.36	13.68	12.10	ns
	–1	0.56	9.55	0.04	1.44	1.82	0.36	9.73	8.39	3.21	2.86	11.63	10.29	ns
	–2	0.49	8.39	0.03	1.27	1.60	0.32	8.54	7.37	2.81	2.51	10.21	9.04	ns
6 mA	Std.	0.66	10.45	0.04	1.70	2.14	0.43	10.65	9.24	3.84	3.55	12.88	11.48	ns
	–1	0.56	8.89	0.04	1.44	1.82	0.36	9.06	7.86	3.27	3.02	10.96	9.76	ns
	–2	0.49	7.81	0.03	1.27	1.60	0.32	7.95	6.90	2.87	2.65	9.62	8.57	ns
8 mA	Std.	0.66	10.02	0.04	1.70	2.14	0.43	10.20	9.23	3.97	4.22	12.44	11.47	ns
	–1	0.56	8.52	0.04	1.44	1.82	0.36	8.68	7.85	3.38	3.59	10.58	9.75	ns
	–2	0.49	7.48	0.03	1.27	1.60	0.32	7.62	6.89	2.97	3.15	9.29	8.56	ns
12 mA	Std.	0.66	10.02	0.04	1.70	2.14	0.43	10.20	9.23	3.97	4.22	12.44	11.47	ns
	–1	0.56	8.52	0.04	1.44	1.82	0.36	8.68	7.85	3.38	3.59	10.58	9.75	ns
	–2	0.49	7.48	0.03	1.27	1.60	0.32	7.62	6.89	2.97	3.15	9.29	8.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-63 • Minimum and Maximum DC Input and Output Levels

HSTL Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max., V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	μA[2]	μA[2]
15 mA[3]	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15	55	66	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Output drive strength is below JEDEC specification.

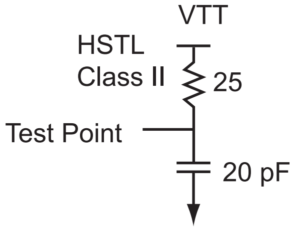


Figure 2-17 • AC Loading

Table 2-64 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

**Table 2-65 • HSTL Class II
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 1.4 V, VREF = 0.75 V**

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	3.02	0.04	2.12	0.43	3.08	2.71			5.32	4.95	ns
–1	0.56	2.57	0.04	1.81	0.36	2.62	2.31			4.52	4.21	ns
–2	0.49	2.26	0.03	1.59	0.32	2.30	2.03			3.97	3.70	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

***Table 2-75* • Minimum and Maximum DC Input and Output Levels**

SSTL3 Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	μA[2]	μA[2]
21 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21	109	103	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

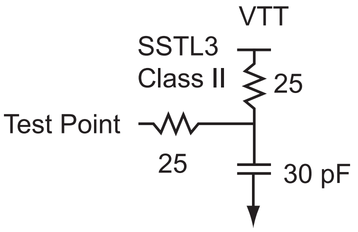


***Figure 2-21* • AC Loading**

***Table 2-76* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

*Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

***Table 2-77* • SSTL3 Class II**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V, VREF = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.07	0.04	1.25	0.43	2.10	1.67			4.34	3.91	ns
–1	0.56	1.76	0.04	1.06	0.36	1.79	1.42			3.69	3.32	ns
–2	0.49	1.54	0.03	0.93	0.32	1.57	1.25			3.24	2.92	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by the Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and DDR. However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-22. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3E also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

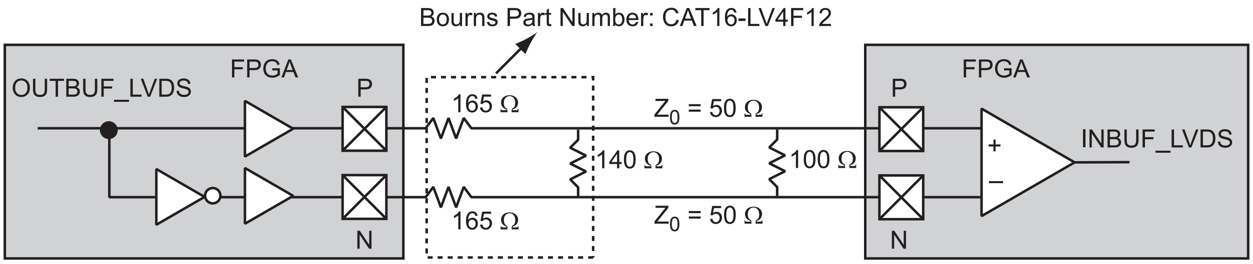


***Figure 2-22* • LVDS Circuit Diagram and Board-Level Implementation**

Table 2-78 • LVDS Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL[1]	Output Lower Current	0.65	0.91	1.16	mA
IOH[1]	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
IIH[2]	Input High Leakage Current			10	µA
IIL[2]	Input Low Leakage Current			10	µA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage [2]	100	350		mV

Notes:

1. *IOL/IOH defined by VODIFF/(Resistor Network).*
2. *Currents are measured at 85°C junction temperature.*

Table 2-79 • AC Waveforms, Measuring Points, and Capacitive Loads

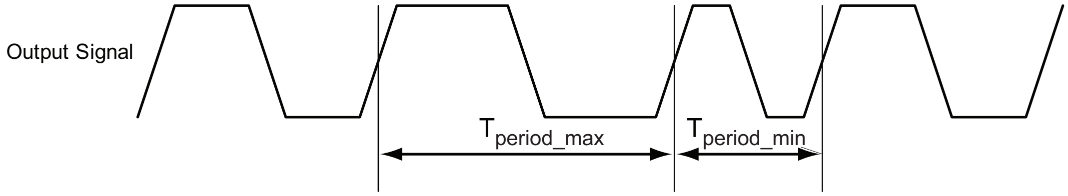
Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)
1.075	1.325	Cross point	–

Note: *Measuring point = Vtrip. See Table 2-15 on page 2-18 for a complete table of trip points.

Table 2-85 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

Note: *See Figure 2-26 on page 2-55 for more information.



Note: *Peak-to-peak jitter measurements are defined by* $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.

***Figure 2-39* • Peak-to-Peak Jitter Definition**

PQ208	
Pin Number	A3PE600 Function
108	TDO
109	TRST
110	VJTAG
111	VMV3
112	GDA0/IO67NPB3V1
113	GDB0/IO66NPB3V1
114	GDA1/IO67PPB3V1
115	GDB1/IO66PPB3V1
116	GDC0/IO65NDB3V1
117	GDC1/IO65PDB3V1
118	IO62NDB3V1
119	IO62PDB3V1
120	IO58NDB3V0
121	IO58PDB3V0
122	GND
123	VCCIB3
124	GCC2/IO55PSB3V0
125	GCB2/IO54PSB3V0
126	NC
127	IO53NDB3V0
128	GCA2/IO53PDB3V0
129	GCA1/IO52PPB3V0
130	GND
131	VCCPLC
132	GCA0/IO52NPB3V0
133	VCOMPLC
134	GCB0/IO51NDB2V1
135	GCB1/IO51PDB2V1
136	GCC1/IO50PSB2V1
137	IO49NDB2V1
138	IO49PDB2V1
139	IO48PSB2V1
140	VCCIB2
141	GND
142	VCC
143	IO47NDB2V1
144	IO47PDB2V1
145	IO44NDB2V1
146	IO44PDB2V1
147	IO43NDB2V0
148	IO43PDB2V0
149	IO40NDB2V0
150	IO40PDB2V0
151	GBC2/IO38PSB2V0
152	GBA2/IO36PSB2V0
153	GBB2/IO37PSB2V0
154	VMV2
155	GNDQ
156	GND
157	VMV1
158	GNDQ
159	GBA1/IO35PDB1V1
160	GBA0/IO35NDB1V1
161	GBB1/IO34PDB1V1
162	GND
163	GBB0/IO34NDB1V1
164	GBC1/IO33PDB1V1
165	GBC0/IO33NDB1V1
166	IO31PDB1V1
167	IO31NDB1V1
168	IO27PDB1V0
169	IO27NDB1V0
170	VCCIB1
171	VCC
172	IO23PPB1V0
173	IO22PSB1V0
174	IO23NPB1V0
175	IO21PDB1V0
176	IO21NDB1V0
177	IO19PPB0V2
178	GND
179	IO18PPB0V2
180	IO19NPB0V2
181	IO18NPB0V2
182	IO17PPB0V2
183	IO16PPB0V2
184	IO17NPB0V2
185	IO16NPB0V2
186	VCCIB0
187	VCC
188	IO15PDB0V2
189	IO15NDB0V2
190	IO13PDB0V2
191	IO13NDB0V2
192	IO11PSB0V1
193	IO09PDB0V1
194	IO09NDB0V1
195	GND
196	IO07PDB0V1
197	IO07NDB0V1
198	IO05PDB0V0
199	IO05NDB0V0
200	VCCIB0
201	GAC1/IO02PDB0V0
202	GAC0/IO02NDB0V0
203	GAB1/IO01PDB0V0
204	GAB0/IO01NDB0V0
205	GAA1/IO00PDB0V0
206	GAA0/IO00NDB0V0
207	GNDQ
208	VMV0

FG324	
Pin Number	**A3PE3000 FBGA**
N1	IO247NDB6V1
N2	IO247PDB6V1
N3	IO251NPB6V2
N4	GEC0/IO236NDB6V0
N5	VCOMPLE
N6	IO212NDB5V2
N7	IO212PDB5V2
N8	IO192NPB4V4
N9	IO174PDB4V2
N10	IO170PDB4V2
N11	GDA2/IO154PPB4V0
N12	GDB2/IO155PPB4V0
N13	GDA1/IO153PPB3V4
N14	VCOMPLD
N15	GDB0/IO152NDB3V4
N16	GDB1/IO152PDB3V4
N17	IO138NDB3V3
N18	IO138PDB3V3
P1	IO245PDB6V1
P2	GNDQ
P3	VMV6
P4	GEC1/IO236PDB6V0
P5	VCCPLE
P6	IO214PDB5V2
P7	VCCIB5
P8	GND
P9	IO174NDB4V2
P10	IO170NDB4V2
P11	GND
P12	VCCIB4
P13	IO155NPB4V0
P14	VCCPLD
P15	VJTAG
P16	GDC0/IO151NDB3V4
P17	GDC1/IO151PDB3V4
P18	IO142PDB3V3
R1	IO245NDB6V1
R2	VCCIB6
R3	GEA1/IO234PPB6V0
R4	IO232NDB5V4
R5	GEB2/IO232PDB5V4
R6	IO214NDB5V2
R7	IO202PDB5V1
R8	IO194PDB5V0
R9	IO186PDB4V4
R10	IO178PDB4V3
R11	IO168NSB4V1
R12	IO164PDB4V1
R13	GDC2/IO156PDB4V0
R14	TCK
R15	VPUMP
R16	TRST
R17	VCCIB3
R18	IO142NDB3V3
T1	IO241PDB6V0
T2	GEA0/IO234NPB6V0
T3	IO233NPB5V4
T4	IO231NPB5V4
T5	VMV5
T6	IO208NDB5V1
T7	IO202NDB5V1
T8	IO194NDB5V0
T9	IO186NDB4V4
T10	IO178NDB4V3
T11	IO166NPB4V1
T12	IO164NDB4V1
T13	IO156NDB4V0
T14	VMV4
T15	TDI
T16	GNDQ
T17	TDO
T18	IO146PDB3V4
U1	IO241NDB6V0
U2	GEA2/IO233PPB5V4
U3	GEC2/IO231PPB5V4
U4	VCCIB5
U5	GNDQ
U6	IO208PDB5V1
U7	IO198PPB5V0
U8	VCCIB5
U9	IO182NPB4V3
U10	IO180NPB4V3
U11	VCCIB4
U12	IO166PPB4V1
U13	IO162PDB4V1
U14	GNDQ
U15	VCCIB4
U16	TMS
U17	VMV3
U18	IO146NDB3V4
V1	GND
V2	IO218NDB5V3
V3	IO218PDB5V3
V4	IO206NDB5V1
V5	IO206PDB5V1
V6	IO198NPB5V0
V7	GND
V8	IO190NDB4V4
V9	IO190PDB4V4
V10	IO182PPB4V3
V11	IO180PPB4V3
V12	GND
V13	IO162NDB4V1
V14	IO160NDB4V0
V15	IO160PDB4V0
V16	IO158NDB4V0
V17	IO158PDB4V0
V18	GND

Revision	Changes	Page
v2.1 (continued)	The words "ambient temperature" were added to the temperature range in the "Temperature Grade Offerings", "Speed Grade and Temperature Grade Matrix", and "Speed Grade and Temperature Grade Matrix" sections.	1-I
	The "Clock Conditioning Circuit (CCC) and PLL" section was updated.	1-I
	The caption "Main (chip)" in Figure 2-9 • Overview of Automotive ProASIC3 VersaNet Global Network was changed to "Chip (main)."	2-9
	The T_J parameter in Table 3-2 • Recommended Operating Conditions was changed to T_A, ambient temperature, and table notes 4–6 were added.	3-2
	The "PLL Macro" section was updated to add information on the VCO and PLL outputs during power-up.	2-15
v2.0 (April 2007)	In the "Temperature Grade Offerings" section, Ambient was deleted.	iii
	Ambient was deleted from "Temperature Grade Offerings".	iii
	Ambient was deleted from the "Speed Grade and Temperature Grade Matrix".	iv
	The "PLL Macro" section was updated to include power-up information.	2-15
	Table 2-13 • ProASIC3E CCC/PLL Specification was updated.	2-30
	Figure 2-19 • Peak-to-Peak Jitter Definition is new.	2-18
	The "SRAM and FIFO" section was updated with operation and timing requirement information.	2-21
	The "RESET" section was updated with read and write information.	2-25
	The "RESET" section was updated with read and write information.	2-25
	The "Introduction" in the "Advanced I/Os" section was updated to include information on input and output buffers being disabled.	2-28
	In the Table 2-15 • Levels of Hot-Swap Support, the ProASIC3 compliance descriptions were updated for levels 3 and 4.	2-34
	Table 2-45 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3E Devices was updated.	2-64
	Notes 3, 4, and 5 were added to Table 2-17 • Comparison Table for 5 V–Compliant Receiver Scheme. 5 x 52.72 was changed to 52.7 and the Maximum current was updated from 4 x 52.7 to 5 x 52.7.	2-40
	The "VCCPLF PLL Supply Voltage" section was updated.	2-50
	The "VPUMP Programming Supply Voltage" section was updated.	2-50
	The "GL Globals" section was updated to include information about direct input into quadrant clocks.	2-51
	VJTAG was deleted from the "TCK Test Clock" section.	2-51
	In Table 2-22 • Recommended Tie-Off Values for the TCK and TRST Pins, TSK was changed to TCK in note 2. Note 3 was also updated.	2-51
	Ambient was deleted from Table 3-2 • Recommended Operating Conditions. VPUMP programming mode was changed from "3.0 to 3.6" to "3.15 to 3.45".	3-2
	Note 3 is new in Table 3-4 • Overshoot and Undershoot Limits (as measured on quiet I/Os).	3-2
	In EQ 3-2, 150 was changed to 110 and the result changed to 5.88.	3-5

Revision	Changes	Page
Advance v0.5 (continued)	The "I/O User Input/Output" pin description was updated to include information on what happens when the pin is unused.	2-50
	The "JTAG Pins" section was updated to include information on what happens when the pin is unused.	2-51
	The "Programming" section was updated to include information concerning serialization.	2-53
	The "JTAG 1532" section was updated to include SAMPLE/PRELOAD information.	2-54
	The "DC and Switching Characteristics" chapter was updated with new information.	Starting on page 3-1
	Table 3-6 was updated.	3-5
	In Table 3-10, PAC4 was updated.	3-8
	Table 3-19 was updated.	3-20
	The note in Table 3-24 was updated.	3-23
	All Timing Characteristics tables were updated from LVTTL to Register Delays	3-26 to 3-64
	The Timing Characteristics for RAM4K9, RAM512X18, and FIFO were updated.	3-74 to 3-79
	F_{TCKMAX} was updated in Table 3-98.	3-80
Advance v0.4 (October 2005)	The "Packaging Tables" table was updated.	ii
Advance v0.3	Figure 2-11 was updated.	2-9
	The "Clock Resources (VersaNets)" section was updated.	2-9
	The "VersaNet Global Networks and Spine Access" section was updated.	2-9
	The "PLL Macro" section was updated.	2-15
	Figure 2-27 was updated.	2-28
	Figure 2-20 was updated.	2-19
	Table 2-5 was updated.	2-25
	Table 2-6 was updated.	2-25
	The "FIFO Flag Usage Considerations" section was updated.	2-27
	Table 2-33 was updated.	2-51
	Figure 2-24 was updated.	2-31
	The "Cold-Sparing Support" section is new.	2-34
	Table 2-45 was updated.	2-64
	Table 2-48 was updated.	2-81
	Pin descriptions in the "JTAG Pins" section were updated.	2-51
	The "Pin Descriptions" section was updated.	2-50
	Table 3-7 was updated.	3-6