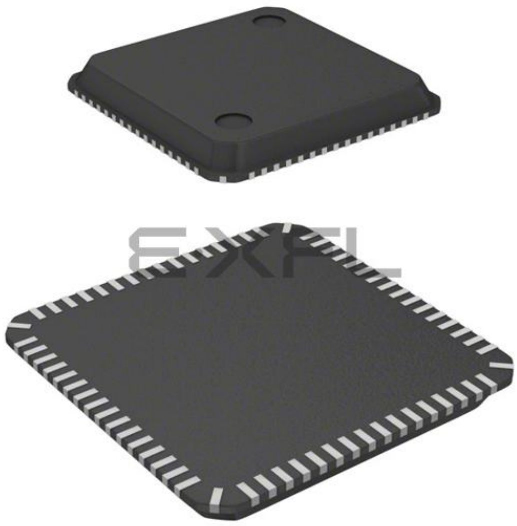
Renesas Electronics America Inc - DF2210CUNP24V Datasheet



Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	24MHz
Connectivity	SCI, SmartCard, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN
Supplier Device Package	64-VQFN (8.2x8.2)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2210cunp24v

2.2 CPU Operating Modes

The H8S/2000 CPU has two operating modes: normal and advanced. Normal mode supports a maximum 64-kbyte address space. Advanced mode supports a maximum 16-Mbyte total address space. The mode is selected by the mode pins.

2.2.1 Normal Mode

The exception vector table and stack have the same structure as in the H8/300 CPU.

- Address Space

  A maximum address space of 64 kbytes can be accessed.

- Extended Registers (En)

  The extended registers (E0 to E7) can be used as 16-bit registers, or as the upper 16-bit segments of 32-bit registers. When En is used as a 16-bit register it can contain any value, even when the corresponding general register (Rn) is used as an address register. If the general register is referenced in the register indirect addressing mode with pre-decrement (@–Rn) or post-increment (@Rn+) and a carry or borrow occurs, however, the value in the corresponding extended register (En) will be affected.

- Instruction Set

  All instructions and addressing modes can be used. Only the lower 16 bits of effective addresses (EA) are valid.

- Exception Vector Table and Memory Indirect Branch Addresses

  In normal mode the top area starting at H'0000 is allocated to the exception vector table. One branch address is stored per 16 bits. The exception vector table in normal mode is shown in figure 2.1. For details of the exception vector table, see section 4, Exception Handling.

  The memory indirect addressing mode (@@aa:8) employed in the JMP and JSR instructions uses an 8-bit absolute address included in the instruction code to specify a memory operand that contains a branch address. In normal mode the operand is a 16-bit (word) operand, providing a 16-bit branch address. Branch addresses can be stored in the top area from H'0000 to H'00FF. Note that this area is also used for the exception vector table.

- Stack Structure

  When the program counter (PC) is pushed onto the stack in a subroutine call, and the PC, condition-code register (CCR), and extended control register (EXR) are pushed onto the stack in exception handling, they are stored as shown in figure 2.2. EXR is not pushed onto the stack in interrupt control mode 0. For details, see section 4, Exception Handling.

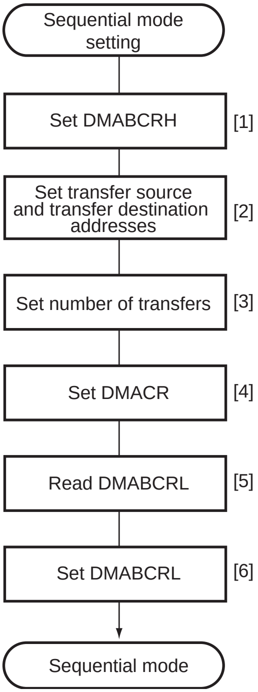
Note: Normal mode is not available in this LSI.

Table 2.10 Block Data Transfer Instruction

Instruction	Size	Function

EEPMOV.B	–	if R4L ≠ 0 then
		        Repeat @ER5+ → @ER6+
		            R4L–1 → R4L
		        Until R4L = 0
		else next;

EEPMOV.W	–	if R4 ≠ 0 then
		        Repeat @ER5+ → @ER6+
		            R4–1 → R4
		        Until R4 = 0
		else next;
		Transfer a data block. Starting from the address set in ER5, transfers data for the number of bytes set in R4L or R4 to the address location set in ER6.
		Execution of the next instruction begins as soon as the transfer is completed.



[1] Set each bit in DMABCRH.
- Clear the FAE bit to 0 to select short address mode.
- Specify enabling or disabling of internal interrupt clearing with the DTA bit.

[2] Set the transfer source address and transfer destination address in MAR and IOAR.

[3] Set the number of transfers in ETCR.

[4] Set each bit in DMACR.
- Set the transfer data size with the DTSZ bit.
- Specify whether MAR is to be incremented or decremented with the DTID bit.
- Clear the RPE bit to 0 to select sequential mode.
- Specify the transfer direction with the DTDIR bit.
- Select the activation source with bits DTF3 to DTF0.

[5] Read the DTE bit in DMABCRL as 0.

[6] Set each bit in DMABCRL.
- Specify enabling or disabling of transfer andinterrupts with the DTIE bit.
- Set the DTE bit to 1 to enable transfer.

Figure 7.3 Example of Sequential Mode Setting Procedure

Table 8.75 PE4 Pin Function

PE4DDR	0	1
Pin Function	PE4 input pin	PE4 output pin

Table 8.76 PE3 Pin Function

PE3DDR	0	1
Pin Function	PE3 input pin	PE3 output pin

Table 8.77 PE2 Pin Function

PE2DDR	0	1
Pin Function	PE2 input pin	PE2 output pin

Table 8.78 PE1 Pin Function

PE1DDR	0	1
Pin Function	PE1 input pin	PE1 output pin

Table 8.79 PE0 Pin Function

PE0DDR	0	1
Pin Function	PE0 input pin	PE0 output pin

8.10.6 Port E Input Pull-Up MOS States

The port E has an on-chip input pull-up MOS function that can be controlled by software. The input pull-up MOS can be used in modes 4 to 6 and in 8-bit bus mode, or in mode 7, and can be specified as the on or off state for individual bits.

Table 8.80 summarizes the input pull-up MOS states.

8.12.1 Port G Data Direction Register (PGDDR)

PGDDR specifies input or output for the pins of the port G.

Since PGDDR is a write-only register, the bit manipulation instructions must not be used to write PGDDR. For details, see section 2.9.4, Accessing Registers Containing Write-Only Bits.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	Undefined	—	Reserved These bits are undefined and cannot be modified.
4	PG4DDR*[2]	0/1*[1]	W	(H8S/2218 Group) Modes 4 to 6: Setting a PGDDR bit to 1 makes the PG4 to PG1 pins bus control signal output pins, while clearing the bit to 0 makes the pins input ports. Mode 7: Setting a PGDDR bit to 1 makes the corresponding port G pin an output port, while clearing the bit to 0 makes the pin an input port. (H8S/2212 Group) Setting a PG1DDR bit to 1 makes the corresponding port G pin an output port, while clearing the bit to 0 makes the pin an input port.
3	PG3DDR*[2]	0	W	
2	PG2DDR*[2]	0	W	
1	PG1DDR	0	W	
0	PG0DDR*[3]	0	W	(H8S/2212 Group) When EMLE = 1: Pin PG0 function as the H-UDI (TDI) pin. When EMLE = 0: If a PG0DDR bit is set to 1, pin PG0 function as output ports. If a PG0DDR bit is cleared to 0, pin PG0 function as input ports.

Notes: 1. The initial value becomes 1 in modes 4 and 5 and 0 in modes 6 and 7.

2. Reserved in the H8S/2212 Group. If this bit is read, an undefined value will be read. This bit cannot be modified.

3. Reserved in the H8S/2218 Group. If this bit is read, an undefined value will be read. This bit cannot be modified.

Table 9.13 TIOR_1 (channel 1)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOB3	IOB2	IOB1	IOB0	TGRB_1 Function	TIOCB1 Pin Function
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 output 0 output at compare match
		1	0		Initial output is 0 output 1 output at compare match
			1		Initial output is 0 output Toggle output at compare match
	1	0	0		Output disabled
			1		Initial output is 1 output 0 output at compare match
		1	0		Initial output is 1 output 1 output at compare match
			1		Initial output is 1 output Toggle output at compare match
1	0	0	0	Input capture register	Capture input source is TIOCB1 pin Input capture at rising edge
			1		Capture input source is TIOCB1 pin Input capture at falling edge
		1	×		Capture input source is TIOCB1 pin Input capture at both edges
	1	×	×		Setting prohibited

Legend:

×: Don’t care

Bit	Bit Name	Initial value	R/W	Description
4	TCFV	0	R/(W)*	Overflow Flag Status flag that indicates that TCNT overflow has occurred. The write value should always be 0 to clear this flag. [Setting condition] When the TCNT value overflows (change from H'FFFF to H'0000) [Clearing condition] When 0 is written to TCFV after reading TCFV = 1
3	TGFD	0	R/(W)*	Input Capture/Output Compare Flag D Status flag that indicates the occurrence of TGRD input capture or compare match in channel 0. The write value should always be 0 to clear this flag. In channels 1 and 2, bit 3 is reserved. It is always read as 0 and cannot be modified. [Setting conditions] • When TCNT = TGRD while TGRD is functioning as output compare register • When TCNT value is transferred to TGRD by input capture signal while TGRD is functioning as input capture register [Clearing condition] When 0 is written to TGFD after reading TGFD = 1
2	TGFC	0	R/(W)*	Input Capture/Output Compare Flag C Status flag that indicates the occurrence of TGRC input capture or compare match in channel 0. The write value should always be 0 to clear this flag. In channels 1 and 2, bit 2 is reserved. It is always read as 0 and cannot be modified. [Setting conditions] • When TCNT = TGRC while TGRC is functioning as output compare register • When TCNT value is transferred to TGRC by input capture signal while TGRC is functioning as input capture register [Clearing condition] When 0 is written to TGFC after reading TGFC = 1

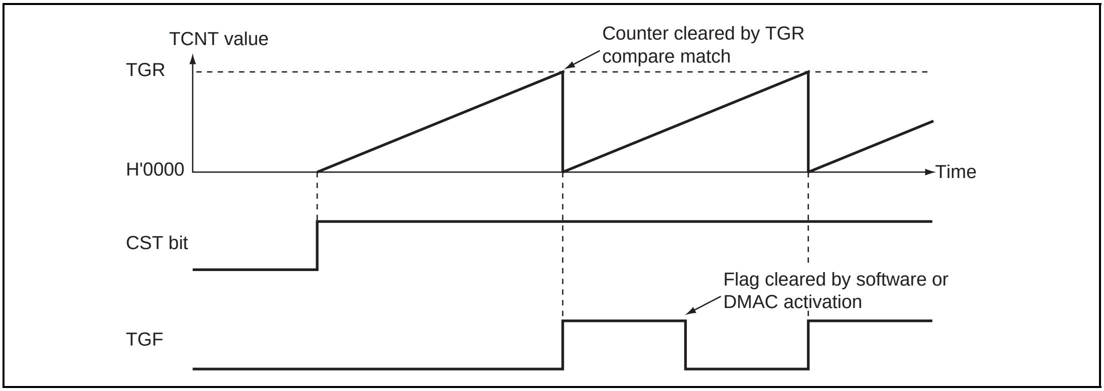
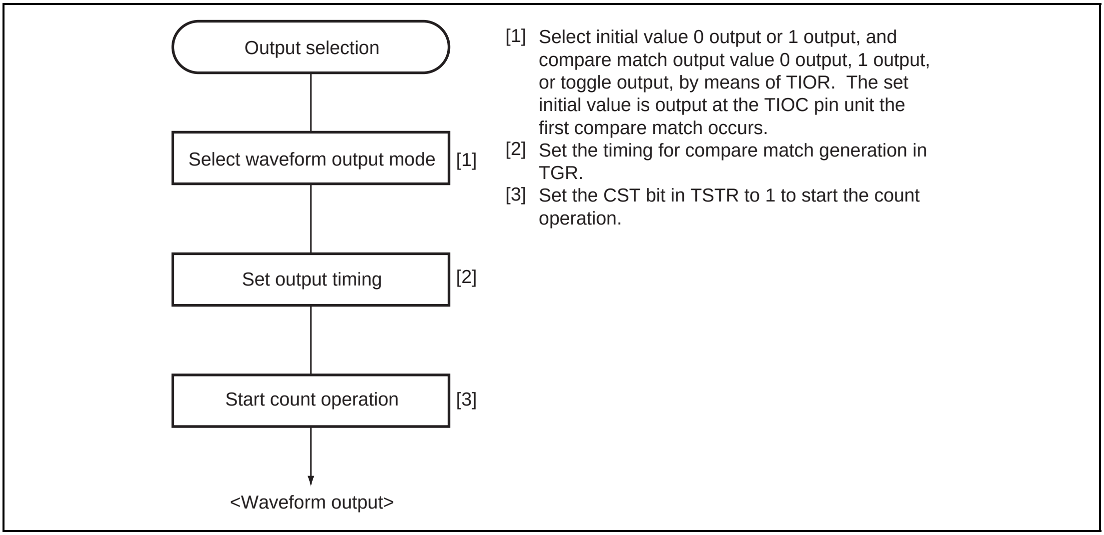


Figure 9.8 Periodic Counter Operation

Waveform Output by Compare Match: The TPU can perform 0, 1, or toggle output from the corresponding output pin using compare match.

1. Example of setting procedure for waveform output by compare match

   Figure 9.9 shows an example of the setting procedure for waveform output by compare match.



[1] Select initial value 0 output or 1 output, and compare match output value 0 output, 1 output, or toggle output, by means of TIOR. The set initial value is output at the TIOC pin unit the first compare match occurs.

[2] Set the timing for compare match generation in TGR.

[3] Set the CST bit in TSTR to 1 to start the count operation.

Figure 9.9 Example of Setting Procedure for Waveform Output by Compare Match

Timing for Counter Clearing by Compare Match/Input Capture: Figure 9.34 shows the timing when counter clearing by compare match occurrence is specified, and figure 9.35 shows the timing when counter clearing by input capture occurrence is specified.

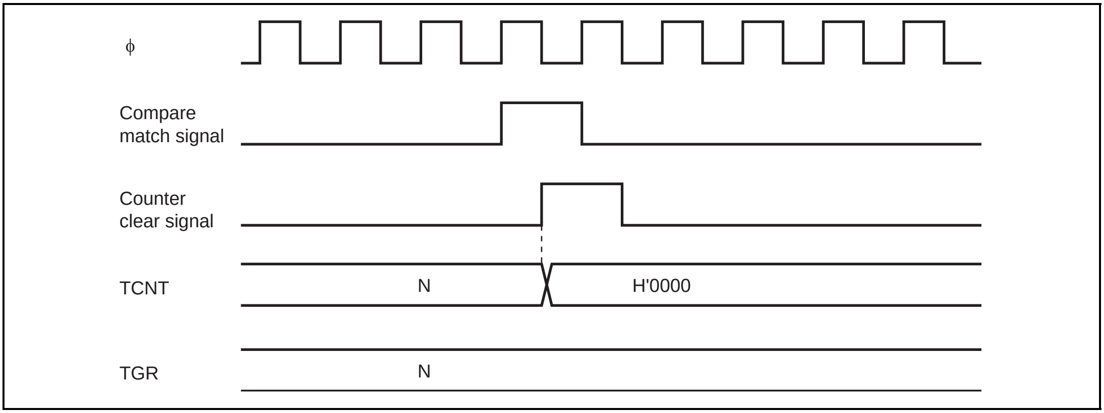


Figure 9.34 Counter Clear Timing (Compare Match)

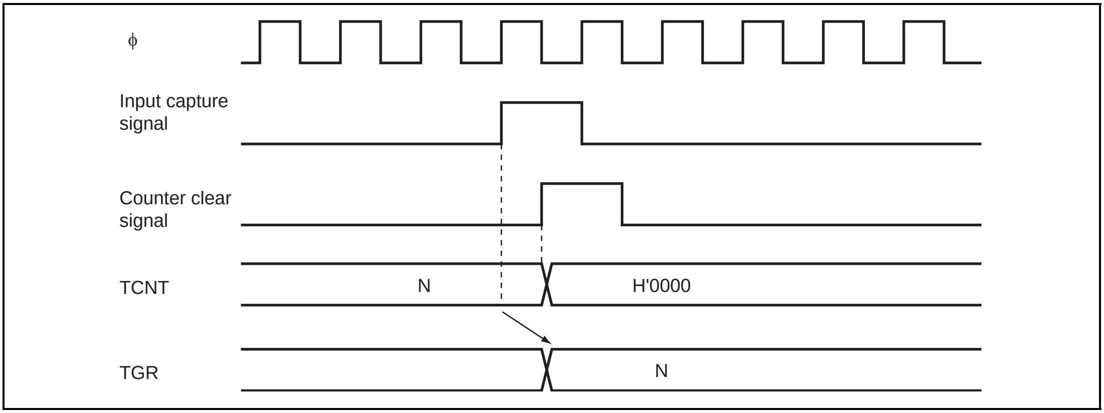


Figure 9.35 Counter Clear Timing (Input Capture)

11.3.7 Clock Source Select Register (RTCCSR)

RTCCSR selects clock source. This register is initialized to H'08 by a $\overline{\text{STBY}}$ input or $\overline{\text{RES}}$ input. A free running counter controls start/stop of counter operation by the RUN bit in RTCCR1. When a clock other than 32.768 MHz is selected, the RTC is disabled and operates as an 8-bit free running counter. An interrupt can be generated by setting 1 to the FOIE bit in RTCCR2 and enabling an overflow interrupt of the free running counter. A clock in which the system clock is divided by 32, 16, 8, or 4 is output in high-speed mode, medium-speed mode, sleep mode, subactive mode, or subsleep mode.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved This bit is always read as 0.
6	RCS6	0	R/W	Clock Output Selection
5	RCS5	0	R/W	Selects a clock output from the TMOW pin when the TMOWE bit in UCTLR is set to 1. 00: φ/4 01: φ/8 10: φ/16 11: φ/32
4	—	0	—	Reserved This bit is always read as 0.
3	RCS3	1	R/W	Clock Source Selection
2	RCS2	0	R/W	0000: φ/8·················· Free running counter operation
1	RCS1	0	R/W	0001: φ/32················ Free running counter operation
0	RCS0	0	R/W	0010: φ/128·············· Free running counter operation 0011: φ/256·············· Free running counter operation 0100: φ/512·············· Free running counter operation 0101: φ/2048············ Free running counter operation 0110: φ/4096············ Free running counter operation 0111: φ/8192············ Free running counter operation 1000: 32.768 kHz·····RTC operation

Bit	Bit Name	Initial Value	R/W	Description
7	ACS3	0	R/W	Asynchronous Clock Source Select Selects the clock source in asynchronous mode depending on the combination with the ACS2 to ACS0 (bits 2 to 0 in SEMRA_0). For details, see section 12.3.9, Serial Extended Mode Register A_0 (SEMRA_0).
6 to 4	—	Undefined	—	Reserved The write value should always be 0.
3	TIOCA2E	1	R/W	TIOCA2 Output Enable Controls the TIOCA2 output on the P16 pin. When the TIOCA2 in TPU is output to generate the transfer clock, P16 is used as other function pin by setting this bit to 0. 0: Disables output of TIOCA2 in TPU 1: Enables output of TIOCA2 in TPU
2	TIOCA1E	1	R/W	TIOCA1 Output Enable Controls the TIOCA1 output on the P14 pin. When the TIOCA1 in TPU is output to generate the transfer clock, P14 is used as other function pin by setting this bit to 0. 0: Disables output of TIOCA1 in TPU 1: Enables output TIOCA1 in TPU
1	TIOCC0E	1	R/W	TIOCC0 Output Enable Controls the TIOCC0 output on the P12 pin. When the TIOCC0 in TPU is output to generate the transfer clock, P12 is used as other function pin by setting this bit to 0. 0: Disables output of TIOCC0 in TPU 1: Enables output of TIOCC0 in TPU
0	TIOCA0E	1	R/W	TIOCA0 Output Enable Controls the TIOCA0 output on the P10 pin. When the TIOCA0 in TPU is output to generate the transfer clock, P10 is used as other function pin by setting this bit to 0. 0: Disables output of TIOCA0 in TPU 1: Enables output of TIOCA0 in TPU

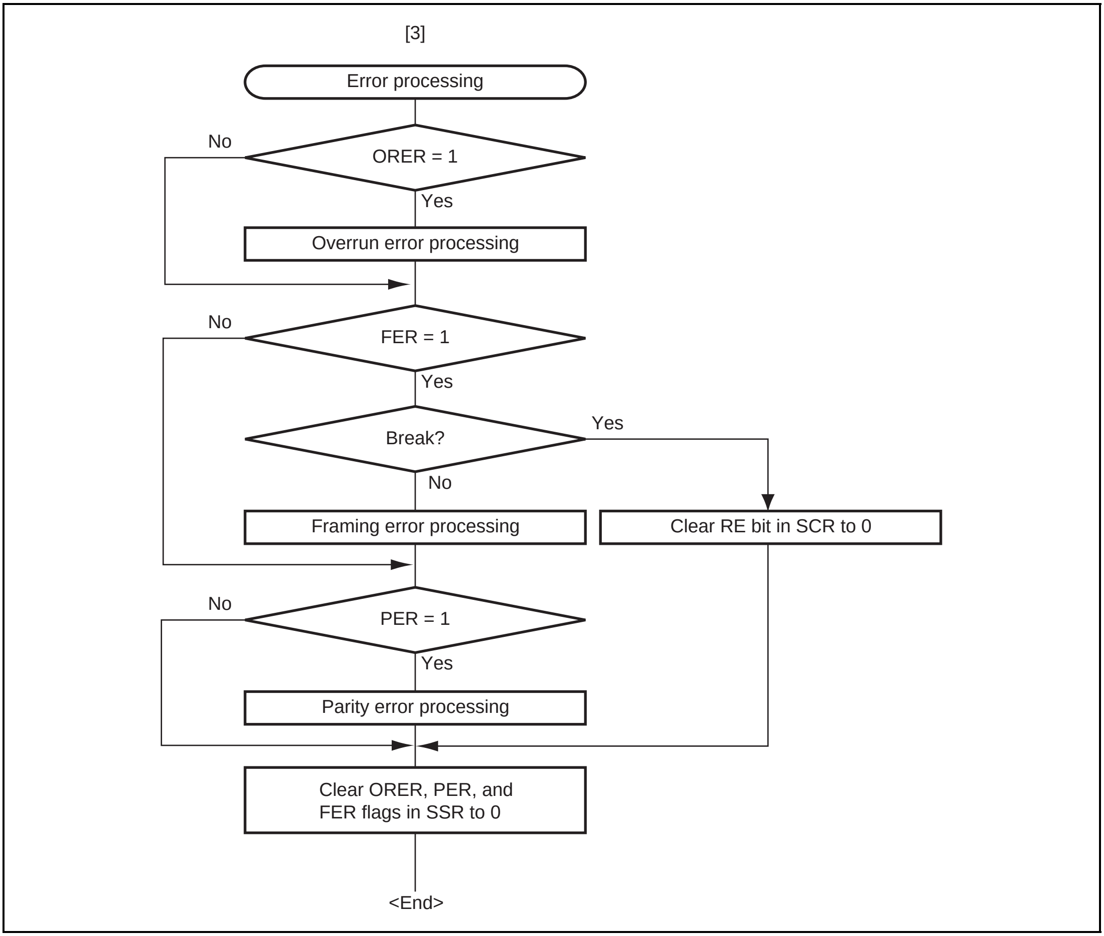


Figure 12.12 Sample Serial Data Reception Flowchart (2)

(3) Automatic Stall by USB Function Module

When a stall setting is made with the Set Feature command, when the information of this module differs from that returned to the host by the Get Descriptor, or in the event of a USB specification violation, the USB function module automatically sets the internal status bit for the corresponding endpoint without regarding to EPnSTL, and returns a stall handshake (1-1 in figure 14.21).

Once an internal status bit is set, it remains set until cleared by a Clear Feature command from the host, without regarding to EPnSTL. After a bit is cleared by the Clear Feature command, EPnSTL is referred (3-1 in figure 14.21). The USB function module continues to return a stall handshake while the internal status bit is set, since the internal status bit is set even if a transaction is executed for the corresponding endpoint (2-1 and 2-2 in figure 14.21). To clear a stall, therefore, the internal status bit must be cleared with a Clear Feature command (3-1 in figure 14.21). If set by the firmware, EPnSTL should also be cleared (2-1 in figure 14.21).

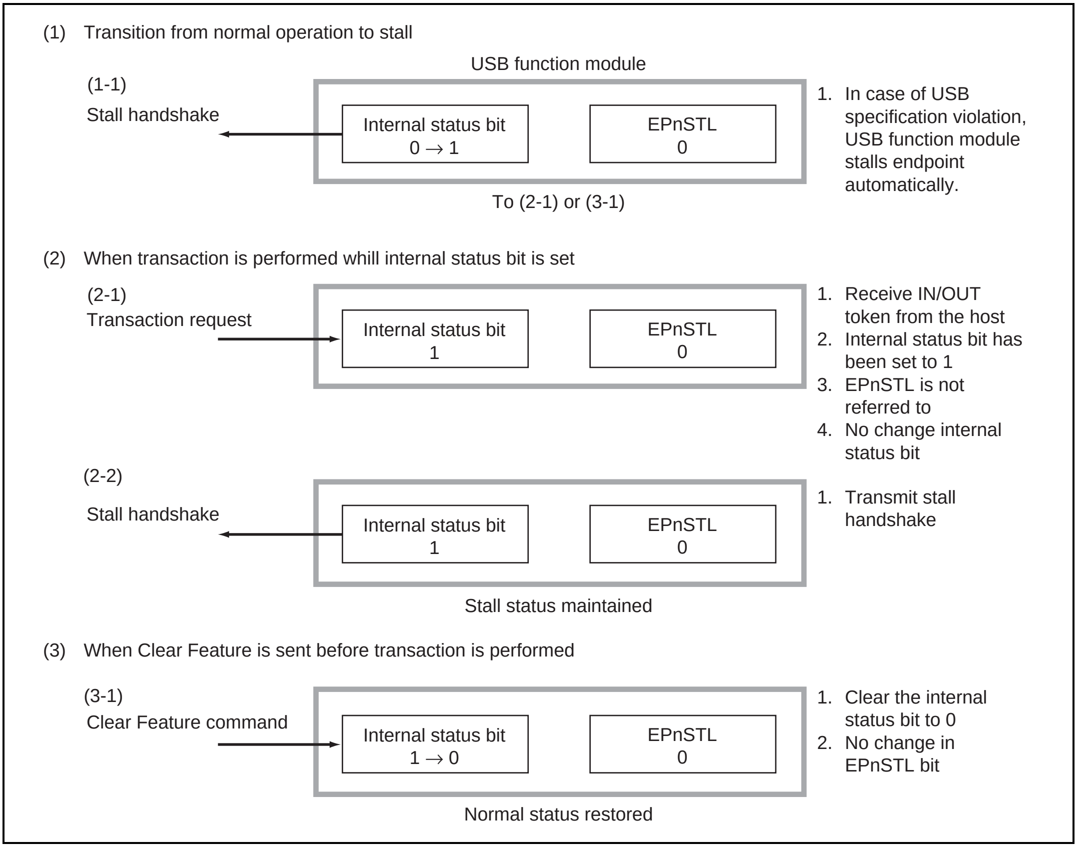

(1) Transition from normal operation to stall
USB function module
(1-1)
Stall handshake
Internal status bit
0 → 1
EPnSTL
0
1. In case of USB specification violation, USB function module stalls endpoint automatically.
To (2-1) or (3-1)
(2) When transaction is performed whill internal status bit is set
(2-1)
Transaction request
Internal status bit
1
EPnSTL
0
1. Receive IN/OUT token from the host
2. Internal status bit has been set to 1
3. EPnSTL is not referred to
4. No change internal status bit
(2-2)
Stall handshake
Internal status bit
1
EPnSTL
0
1. Transmit stall handshake
Stall status maintained
(3) When Clear Feature is sent before transaction is performed
(3-1)
Clear Feature command
Internal status bit
1 → 0
EPnSTL
0
1. Clear the internal status bit to 0
2. No change in EPnSTL bit
Normal status restored

Figure 14.21 Automatic Stall by USB Function Module

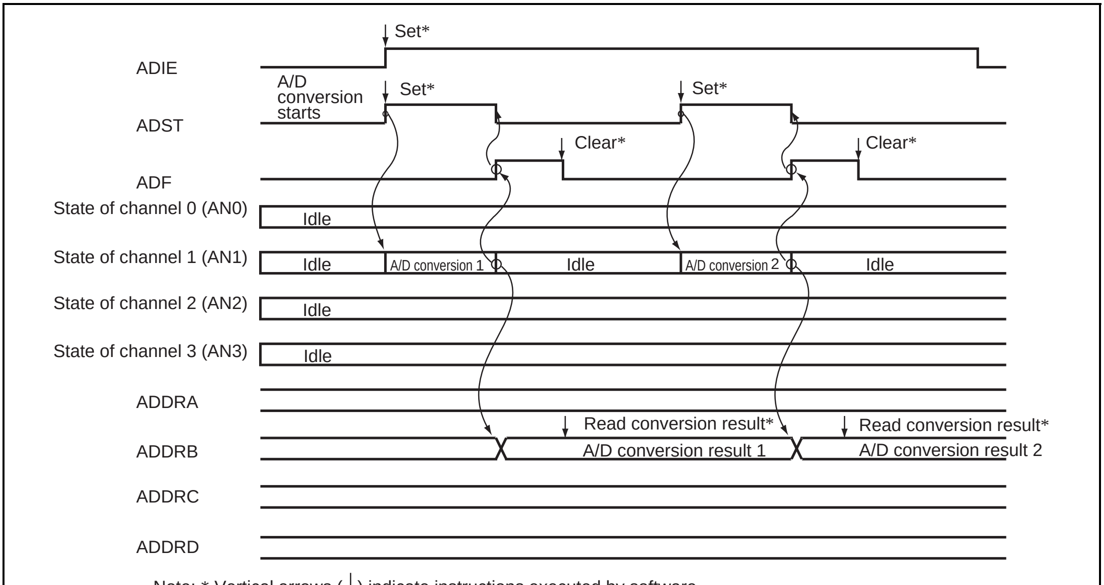
15.5 Operation

The A/D converter operates by successive approximation with 10-bit resolution. It has two operating modes; single mode and scan mode. When changing the operating mode or analog input channel, in order to prevent incorrect operation, first clear the bit ADST to 0 in ADCSR. The ADST bit can be set at the same time as the operating mode or analog input channel is changed.

15.5.1 Single Mode

In single mode, A/D conversion is to be performed only once on the specified single channel. The operations are as follows.

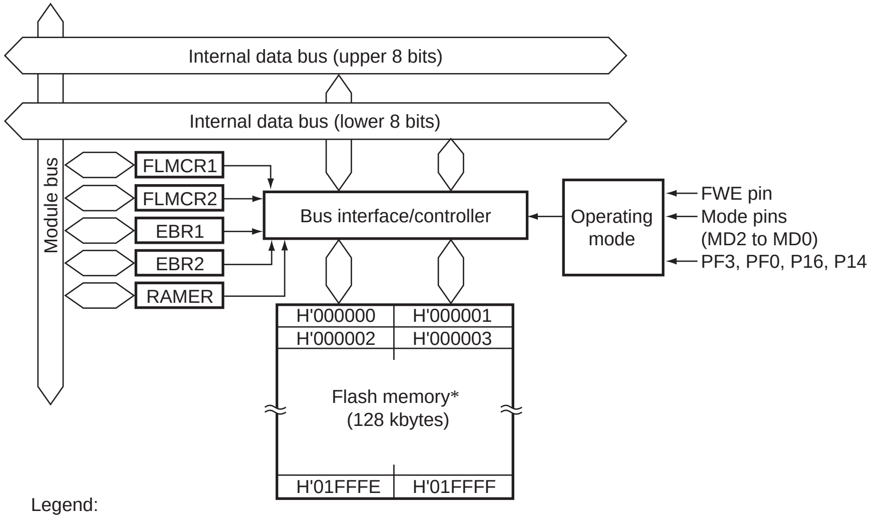
1. A/D conversion is started when the ADST bit is set to 1, according to software or external trigger input.
2. When A/D conversion is completed, the result is transferred to the corresponding A/D data register to the channel.
3. On completion of conversion, the ADF bit in ADCSR is set to 1. If the ADIE bit is set to 1 at this time, an ADI interrupt request is generated.
4. The ADST bit remains set to 1 during A/D conversion. When A/D conversion ends, the ADST bit is automatically cleared to 0 and the A/D converter enters the wait state.



Note: * Vertical arrows (↓) indicate instructions executed by software.

Figure 15.3 A/D Conversion Timing (Single-Chip Mode, Channel 1 Selected)

- Automatic bit rate adjustment
  - — With data transfer in SCI boot mode, this LSI's bit rate can be automatically adjusted to match the transfer bit rate of the host.
- Programming/erasing protection
  - — Sets hardware protection, software protection, and error protection against flash memory programming/erasing.
- Programmer mode
  - — Flash memory can be programmed/erased in programmer mode, using a PROM programmer, as well as in on-board programming mode.
- Flash memory emulation in RAM
  - — Flash memory programming can be emulated in real time by overlapping a part of RAM onto flash memory.



Legend:
FLMCR1: Flash memory control register 1
FLMCR2: Flash memory control register 2
EBR1: Erase block register 1
EBR2: Erase block register 2
RAMER: RAM emulation register

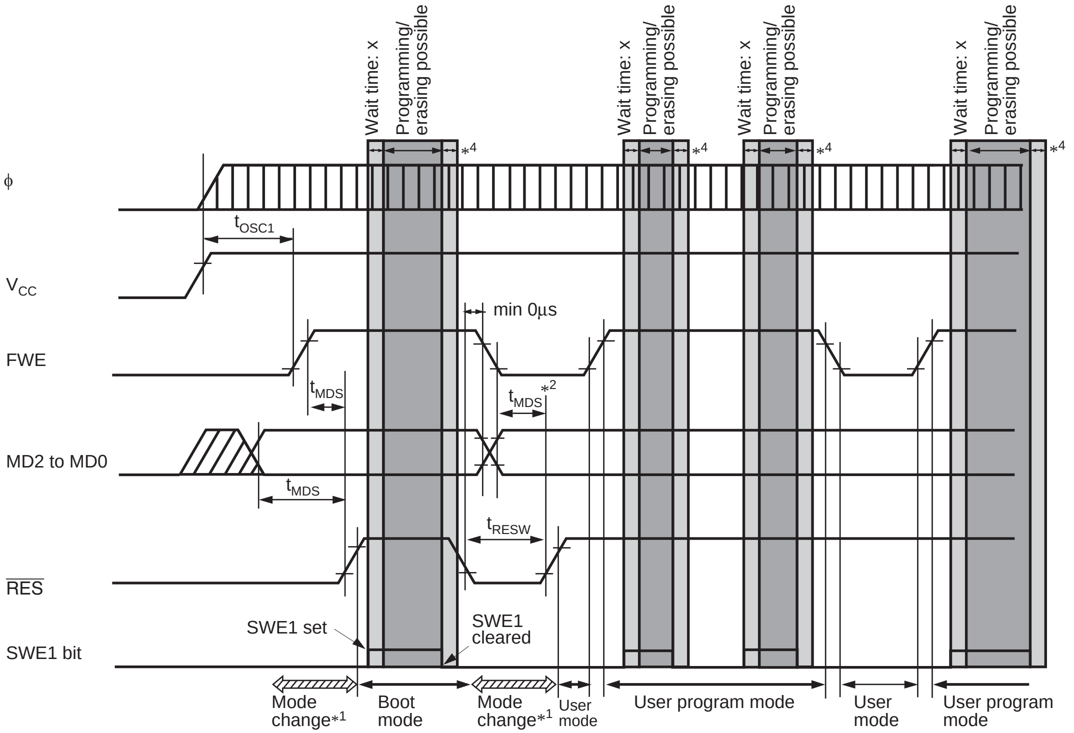
Note: * 128 kbytes in the HD64F2218, HD64F2218U, HD64F2218CU, HD64F2212, HD64F2212U and HD64F2212CU;
64 kbytes in the HD64F2217CU, HD64F2211, HD64F2211U and HD64F2211CU.
32 kbytes in the HD64F2210CU

Figure 17.1 Block Diagram of Flash Memory

17.8.2 Erase/Erase-Verify

When erasing flash memory, the erase/erase-verify flowchart shown in Figure 17.14 should be followed.

1. Prewriting (setting erase block data to all 0s) is not necessary.
2. Erasing is performed in block units. Make only a single-bit specification in the erase block register 1, 2 (EBR1, EBR2). To erase multiple blocks, each block must be erased in turn.
3. The time during which the E1 bit is set to 1 is the flash memory erase time.
4. The watchdog timer (WDT) is set to prevent overprogramming due to program runaway, etc. An overflow cycle of approximately ($y+z+\alpha+\beta$) ms is allowed.
5. For a dummy write to a verify address, write 1-byte data H'FF to an address whose lower 1 bit is B'0. Verify data can be read in longwords from the address to which a dummy write was performed.
6. If the read data is unerased, set erase mode again, and repeat the erase/erase-verify sequence as before. The maximum number of repetitions of the erase/erase-verify sequence is N.



░ Period during which flash memory access is prohibited
(x: Wait time after setting SWE1 bit)*3

▓ Period during which flash memory can be programmed
(Execution of program in flash memory prohibited, and data reads other than verify operations prohibited)

Notes: 1. When entering boot mode or making a transition from boot mode to another mode, mode switching must be carried out by means of $\overline{\text{RES}}$ input

2. When making a transition from boot mode to another mode, a mode programming setup time t_{MDS} (min) of 200 ns is necessary with respect to $\overline{\text{RES}}$ clearance timing.

3. See section 22.7, Flash Memory Characteristics.

4. Wait time: θ.

Figure 17.18 Mode Transition Timing
(Example: Boot Mode → User Mode ↔ User Program Mode)

Timing of Recovery from Hardware Standby Mode:

Drive the $\overline{\text{RES}}$ signal low approximately 100 ns or more before $\overline{\text{STBY}}$ goes high to execute a power-on reset.

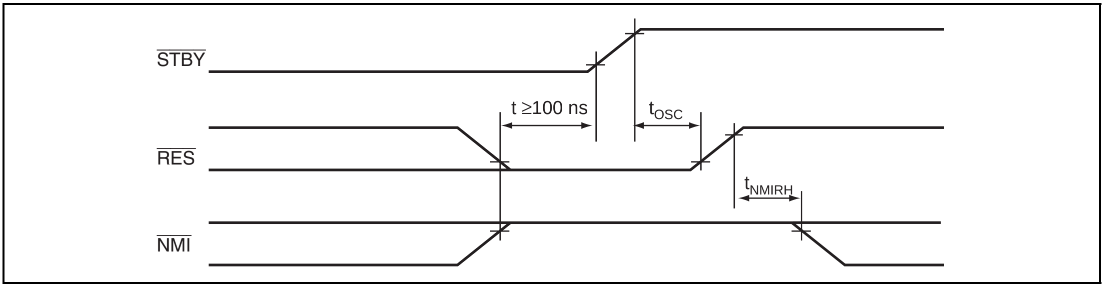


Figure 20.7 Timing of Recovery from Hardware Standby Mode

20.6 Module Stop Mode

Module stop mode can be set for individual on-chip supporting modules.

When the corresponding MSTP bit in MSTPCR is set to 1, module operation stops at the end of the bus cycle and a transition is made to module stop mode. The CPU continues operating independently.

When the corresponding MSTP bit is cleared to 0, module stop mode is cleared and the module starts operating at the end of the bus cycle. In module stop mode, the internal states of modules other than the A/D converter are retained.

After reset clearance, all modules other than DMAC and flash memory are in module stop mode.

When an on-chip supporting module is in module stop mode, read/write access to its registers is disabled.

When a transition is made to sleep mode with all modules stopped, the bus controller and I/O ports also stop operating, enabling current dissipation to be further reduced.