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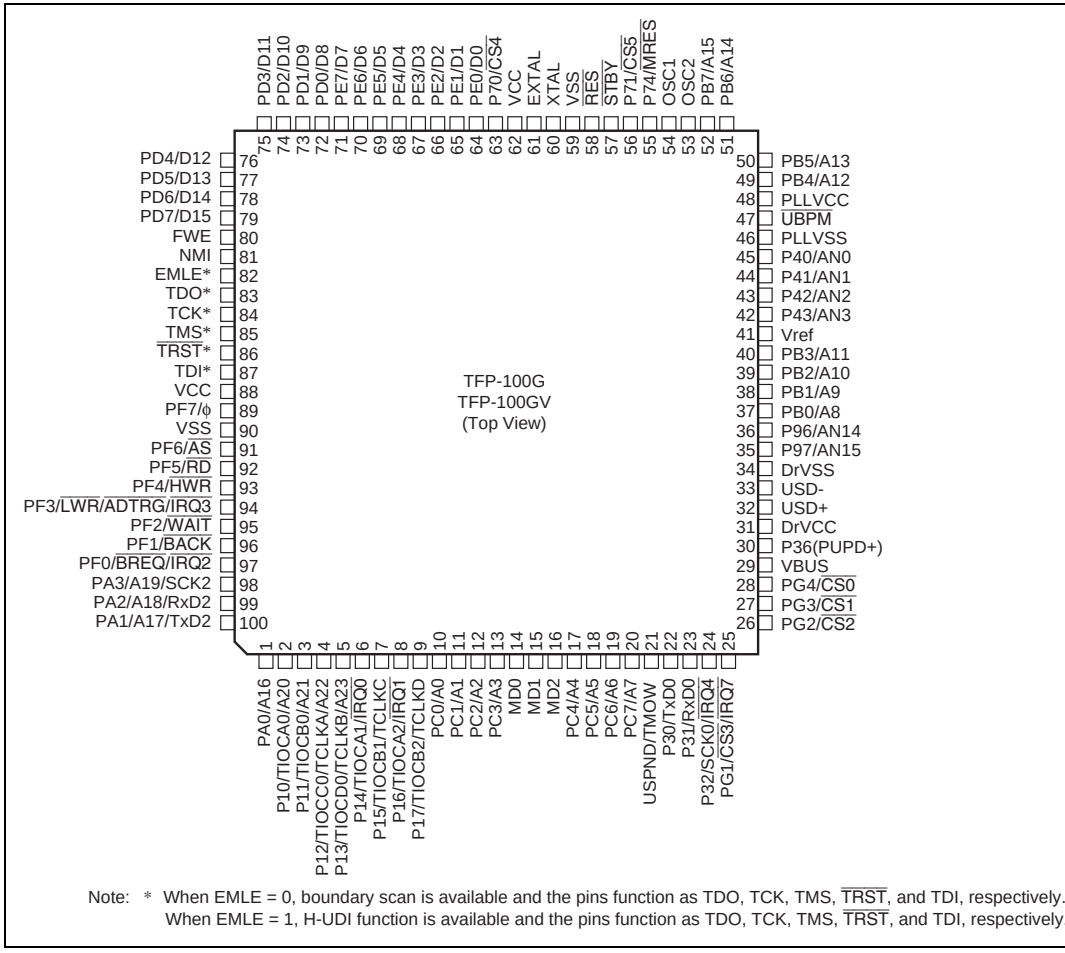
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	24MHz
Connectivity	SCI, SmartCard, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2211cufp24v

1.3 Pin Arrangements

The pin arrangements of the HD64F2218, HD64F2218U, HD64F2218CU and HD64F2217CU are shown in figures 1.5 and 1.6. The pin arrangements of the HD6432217 are shown in figures 1.7 and 1.8. The pin arrangements of the HD64F2212, HD64F2212U, HD64F2212CU, HD64F2211, HD64F2211U, HD64F2211CU and HD64F2210CU are shown in figures 1.9 and 1.11. The pin arrangements of the HD6432211, HD6432210 and HD6432210S is shown in figures 1.10 and 1.12.



Note: * When EMLE = 0, boundary scan is available and the pins function as TDO, TCK, TMS, TRST, and TDI, respectively.
When EMLE = 1, H-UDI function is available and the pins function as TDO, TCK, TMS, TRST, and TDI, respectively.

Figure 1.5 Pin Arrangements of HD64F2218, HD64F2218U, HD64F2218CU and HD64F2217CU (TFP-100G, TFP-100GV)

2.8 Processing States

The H8S/2000 CPU has five main processing states: the reset state, exception handling state, program execution state, bus-released state, and power-down state. Figure 2.13 indicates the state transitions.

- Reset State

  In this state the CPU and internal peripheral modules are all initialized and stop. When the $\overline{\text{RES}}$ input goes low all current processing stops and the CPU enters the reset state. All interrupts are masked in the reset state. Reset exception handling starts when the $\overline{\text{RES}}$ signal changes from low to high. For details, refer to section 4, Exception Handling.

  The reset state can also be entered by a watchdog timer overflow.

- Exception-Handling State

  The exception-handling state is a transient state that occurs when the CPU alters the normal processing flow due to an exception source, such as, a reset, trace, interrupt, or trap instruction. The CPU fetches a start address (vector) from the exception vector table and branches to that address. For further details, refer to section 4, Exception Handling.

- Program Execution State

  In this state the CPU executes program instructions in sequence.

- Bus-Released State

  In a product which has a bus master other than the CPU, such as a direct memory access controller (DMAC) and a data transfer controller (DTC), the bus-released state occurs when the bus has been released in response to a bus request from a bus master other than the CPU. While the bus is released, the CPU halts operations.

- Power-Down State

  This is a power-down state in which the CPU stops operating. The program stop state occurs when a SLEEP instruction is executed or the CPU enters hardware standby mode. For details, refer to section 20, Power-Down Modes.

Section 3 MCU Operating Modes

3.1 Operating Mode Selection

This LSI supports four operating modes (modes 4 to 7). These modes enable selection of the CPU operating mode, enabling/disabling of on-chip ROM, and the initial bus width setting, by setting the mode pins (MD2 to MD0) as show in table 3.1. Modes 4 to 6 are external extended modes that allow access to the external memory and peripheral devices. In external extended mode, 8-bit or 16-bit address space can be set for each area depending on the bus controller setting after program execution starts. If 16-bit access is selected for any one area, 16-bit bus mode is set; if 8-bit access is selected for all areas, 8-bit bus mode is set. In mode 7, the external address space cannot be used. Do not change the mode pin settings during operation. Only mode 7 is available in the H8S/2212 Group.

Table 3.1 MCU Operating Mode Selection

MCU Operating Mode	MD2	MD1	MD0	CPU Operating Mode	Description	On-chip ROM	External Data Bus	
							Initial Value	Maximum Value
4	1	0	0	Advanced mode	On-chip ROM disabled, extended mode	Disabled	16 bits	16 bits
5	1	0	1	Advanced mode	On-chip ROM disabled, extended mode	Disabled	8 bits	16 bits
6	1	1	0	Advanced mode	On-chip ROM enabled, extended mode	Enabled	8 bits	16 bits
7	1	1	1	Advanced mode	Single-chip mode	Enabled	–	–

Note: When using the E6000 emulator:

- Mode 7 is not available in the H8S/2218 Group. (The E6000 emulator does not support mode 7.)
- Note following restrictions to use the RTC and USB in mode 6.
  Specify PFCR so that A9 and A8 are output on the PB1 and PB0 pins.
  Set H'FF in PCDDR so that A7 to A0 are output on the PC7 to PC0 pins.

5.6 Interrupt Control Modes and Interrupt Operation

The interrupt controller has two modes: interrupt control mode 0 and interrupt control mode 2.

Interrupt operations differ depending on the interrupt control mode. The interrupt control mode is selected by SYSCR. Table 5.3 shows the differences between interrupt control mode 0 and interrupt control mode 2.

Table 5.3 Interrupt Control Modes

Interrupt Control Mode	Priority Setting Register	Interrupt Mask Bits	Description
0	Default	I	The priority of interrupt sources are fixed at the default settings. Interrupt sources except for NMI is marked by the I bit.
2	IPR	I2 to I0	8-level interrupt mask control is performed by bits I2 to I0. 8 priority levels other than NMI can be set with IPR.

5.6.1 Interrupt Control Mode 0

In interrupt control mode 0, interrupt requests except for NMI is masked by the I bit of CCR in the CPU. Figure 5.4 shows a flowchart of the interrupt acceptance operation in this case.

1. If an interrupt source occurs when the corresponding interrupt enable bit is set to 1, an interrupt request is sent to the interrupt controller.
2. If the I bit is set to 1, only an NMI interrupt is accepted, and other interrupt requests are held pending. If the I bit is cleared, an interrupt request is accepted.
3. Interrupt requests are sent to the interrupt controller, the highest-ranked interrupt according to the priority system is accepted, and other interrupt requests are held pending.
4. When the CPU accepts an interrupt request, it starts interrupt exception handling after execution of the current instruction has been completed.
5. The PC and CCR are saved to the stack area by interrupt exception handling. The PC saved on the stack shows the address of the first instruction to be executed after returning from the interrupt handling routine.
6. Next, the I bit in CCR is set to 1. This masks all interrupts except NMI.

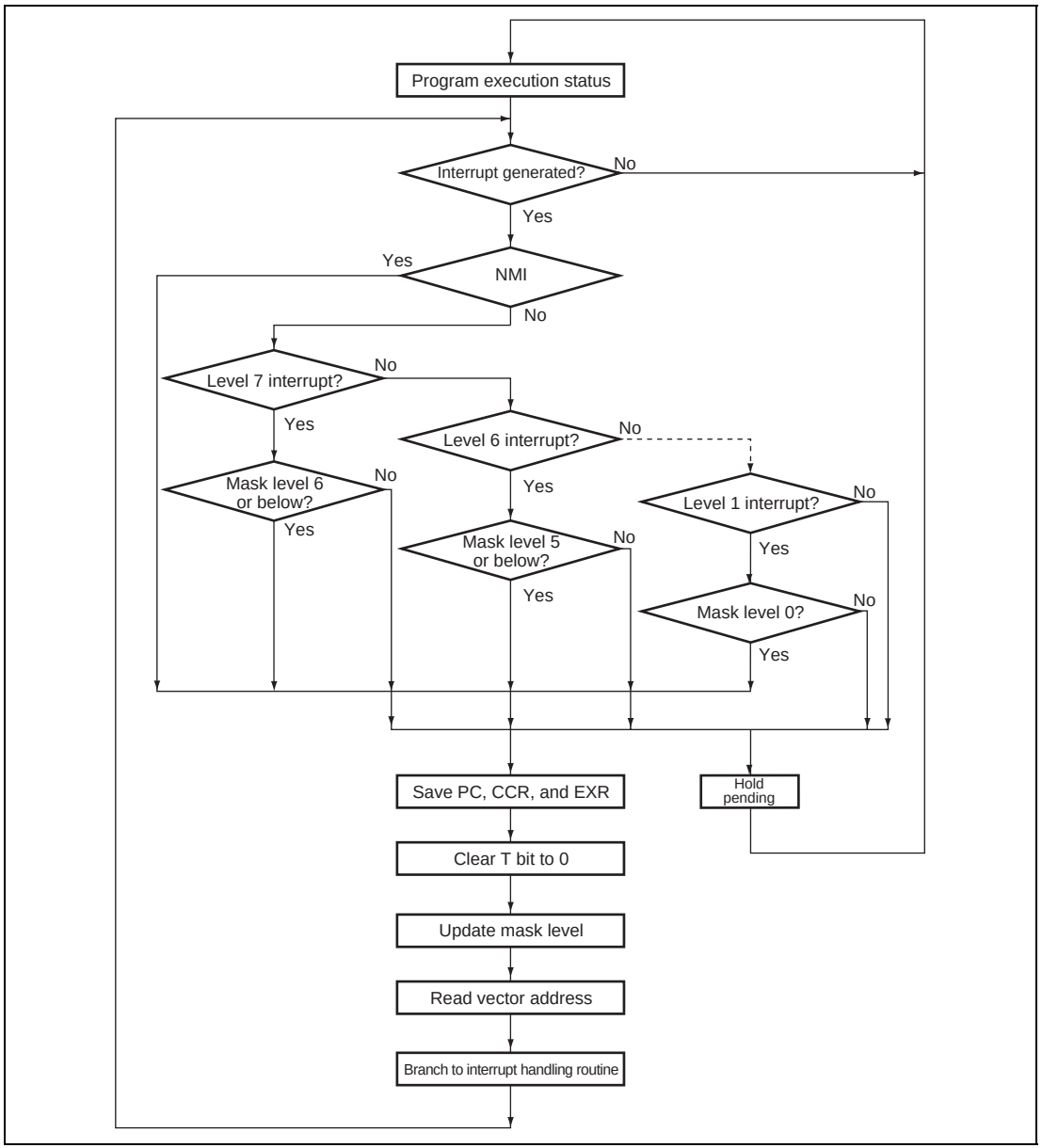


Figure 5.5 Flowchart of Procedure Up to Interrupt Acceptance in Interrupt Control Mode 2

8-Bit 3-State Access Space (Area 6 and RTC): Figure 6.12 shows the bus timing for area 6 and RTC area (address = H'FFFF40 to H'FFFF5F). When the areas are accessed, the data bus cannot be used.

Wait states cannot be inserted.

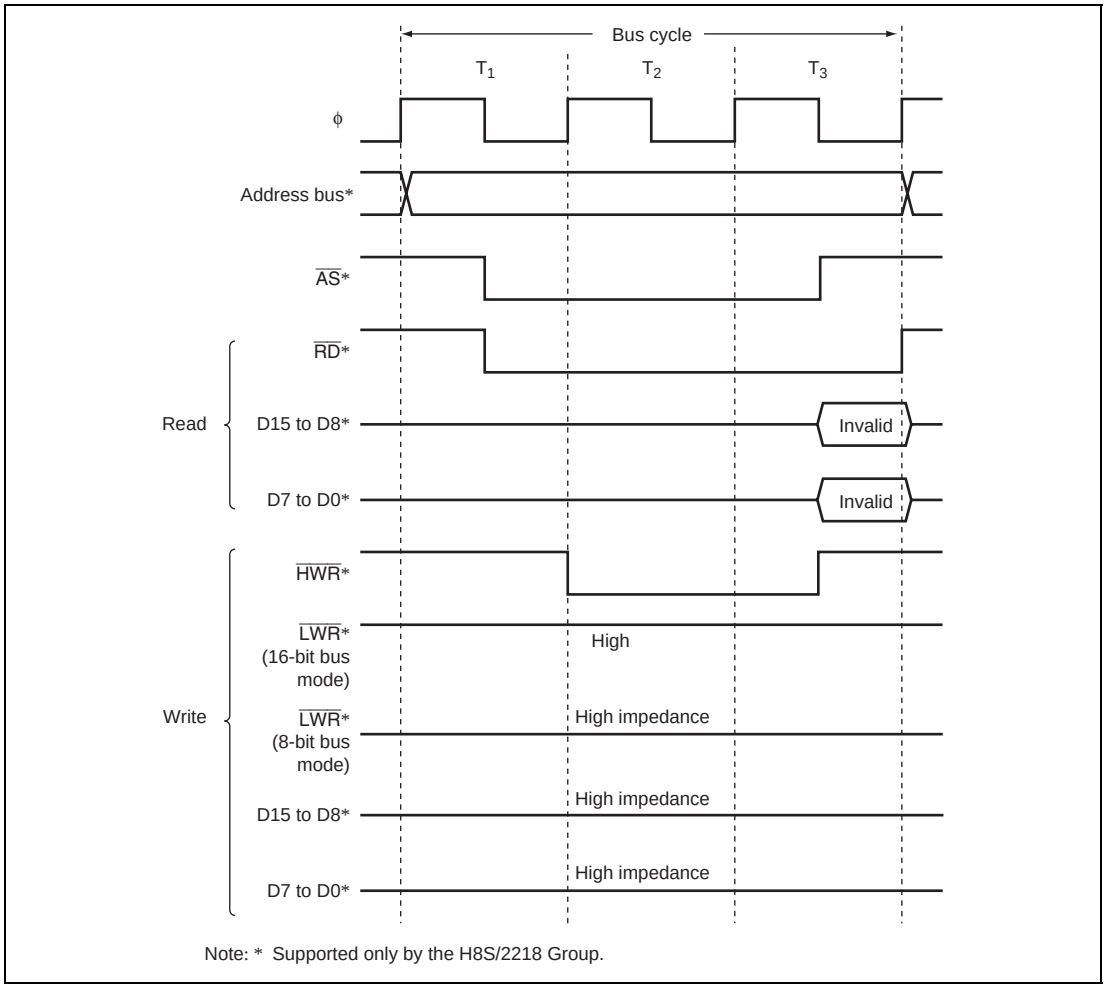


Figure 6.12 Bus Timing for Area 6 and RTC

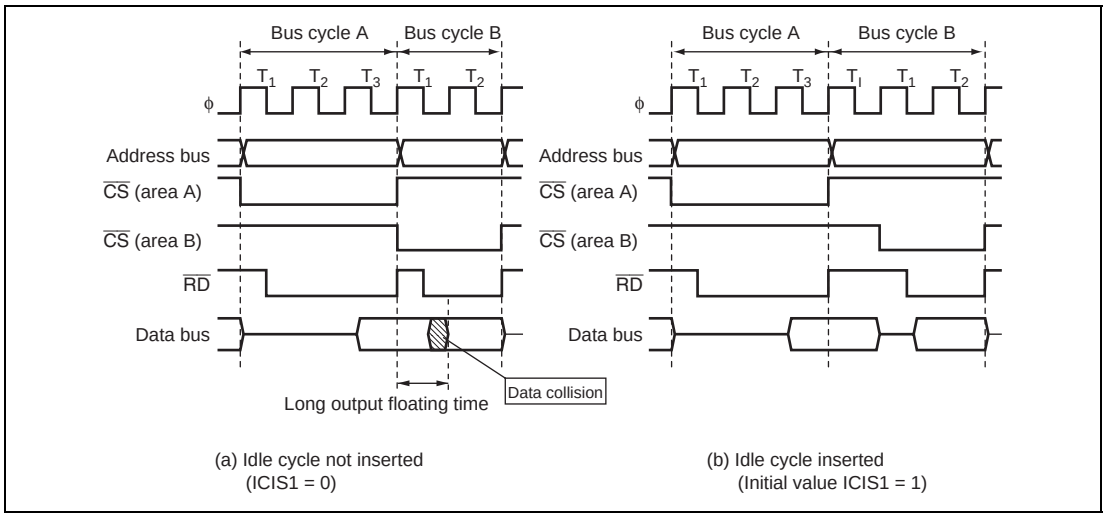


Figure 6.22 Example of Idle Cycle Operation (1)

Port	Description	Modes 4 and 5	Mode 6	Mode 7	Input/Output Type
Port E	General I/O port also functioning as data bus I/O pins	8-bit bus mode: PE7 16-bit bus mode: D7		PE7	On-chip input pull-up MOS
		8-bit bus mode: PE6 16-bit bus mode: D6		PE6	
		8-bit bus mode: PE5 16-bit bus mode: D5		PE5	
		8-bit bus mode: PE4 16-bit bus mode: D4		PE4	
		8-bit bus mode: PE3 16-bit bus mode: D3		PE3	
		8-bit bus mode: PE2 16-bit bus mode: D2		PE2	
		8-bit bus mode: PE1 16-bit bus mode: D1		PE1	
		8-bit bus mode: PE0 16-bit bus mode: D0		PE0	
Port F	General I/O port also functioning as bus control signal I/O pins and interrupt input pins	When DDR = 0: PF7 When DDR = 1 (after reset): ϕ		When DDR = 0 (after reset): PF7 When DDR = 1: ϕ	Schmitt trigger input ($\overline{IRQ3}$, $\overline{IRQ2}$)
		$\overline{AS}$		PF6	
		$\overline{RD}$		PF5	
		$\overline{HWR}$		PF4	
		8-bit bus mode: PF3/$\overline{ADTRG}$/$\overline{IRQ3}$ 16-bit bus mode: $\overline{LWR}$		PF3/$\overline{ADTRG}$/$\overline{IRQ3}$	
		When WAITE = 0 (after reset): PF2 When WAITE = 1: $\overline{WAIT}$		PF2	
		When BRLE = 0 (after reset): PF1 When BRLE = 1: $\overline{BACK}$		PF1	
		When BRLE = 0 (after reset): PF0/$\overline{IRQ2}$ When BRLE = 1: $\overline{BREQ}$/$\overline{IRQ2}$		PF0/$\overline{IRQ2}$	

Bit	Bit Name	Initial value	R/W	Description
1	TGFB	0	R/(W)*	Input Capture/Output Compare Flag B Status flag that indicates the occurrence of TGRB input capture or compare match. The write value should always be 0 to clear this flag. [Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register [Clearing condition] When 0 is written to TGFB after reading TGFB = 1
0	TGFA	0	R/(W)*	Input Capture/Output Compare Flag A Status flag that indicates the occurrence of TGRA input capture or compare match. The write value should always be 0 to clear this flag. [Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register [Clearing conditions] • When DMAC is activated by TGIA interrupt while DTA bit of DMABCR in DMAC is 1 • When 0 is written to TGFA after reading TGFA = 1

Note: * Only 0 can be written to clear the flags.

Buffer Operation Timing: Figures 9.36 and 9.37 show the timing in buffer operation.

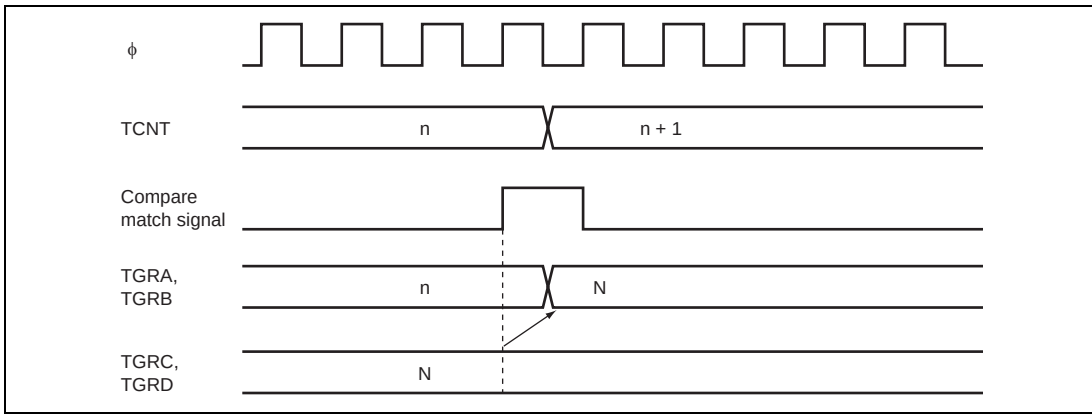


Figure 9.36 Buffer Operation Timing (Compare Match)

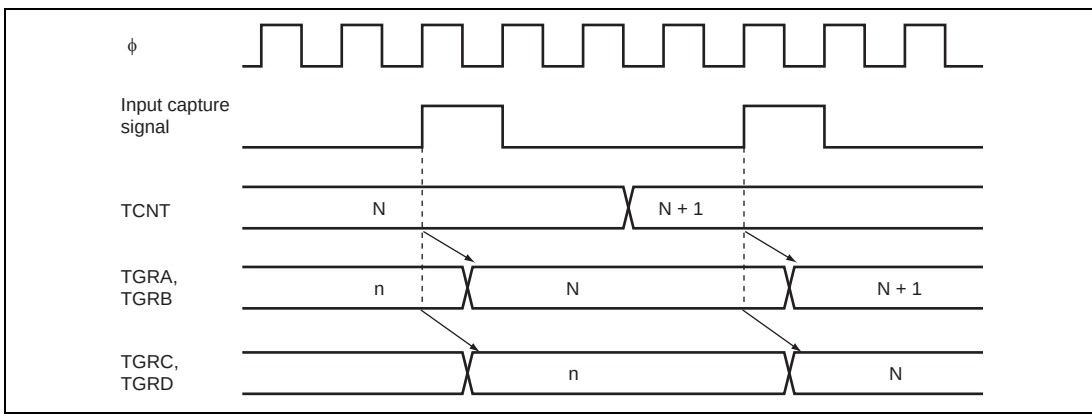


Figure 9.37 Buffer Operation Timing (Input Capture)

9.7.2 Interrupt Signal Timing

TGF Flag Setting Timing in Case of Compare Match: Figure 9.38 shows the timing for setting of the TGF flag in TSR by compare match occurrence, and TGI interrupt request signal timing.

Contention between TCNT Write and Clear Operations: If the counter clear signal is generated in the T_2 state of a TCNT write cycle, TCNT clearing takes precedence and the TCNT write is not performed. Figure 9.45 shows the timing in this case.

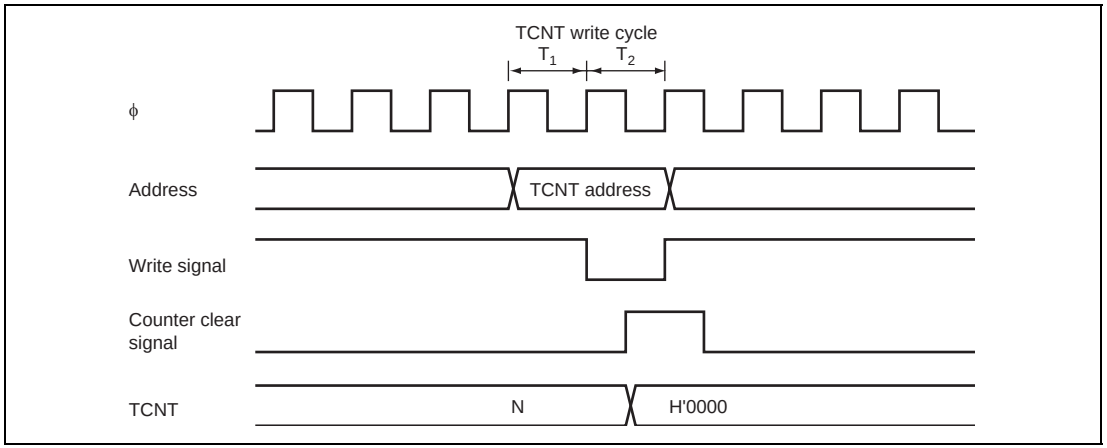


Figure 9.45 Contention between TCNT Write and Clear Operations

Contention between TCNT Write and Increment Operations: If incrementing occurs in the T_2 state of a TCNT write cycle, the TCNT write takes precedence and TCNT is not incremented. Figure 9.46 shows the timing in this case.

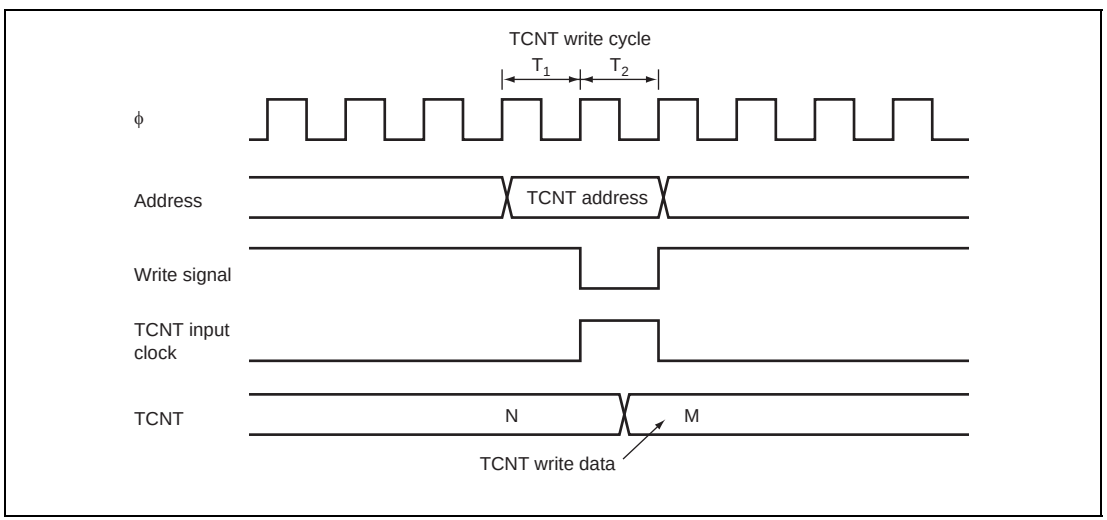


Figure 9.46 Contention between TCNT Write and Increment Operations

Timing and Reception Margin. Tables 12.5 and 12.7 show the maximum bit rates with external clock input.

When the ABCS bit in SCI_0's serial extended mode register A_0 (SEMRA_0) is set to 1 in asynchronous mode, the maximum bit rates are twice those shown in table 12.3.

Table 12.3 BRR Settings for Various Bit Rates (Asynchronous Mode)

Bit Rate	Operating Frequency ϕ (MHz)											
	2			2.097152			2.4576			3		
(bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	1	141	0.03	1	148	–0.04	1	174	–0.26	1	212	0.03
150	1	103	0.16	1	108	0.21	1	127	0.00	1	155	0.16
300	0	207	0.16	0	217	0.21	0	255	0.00	1	77	0.16
600	0	103	0.16	0	108	0.21	0	127	0.00	0	155	0.16
1200	0	51	0.16	0	54	–0.70	0	63	0.00	0	77	0.16
2400	0	25	0.16	0	26	1.14	0	31	0.00	0	38	0.16
4800	0	12	0.16	0	13	–2.48	0	15	0.00	0	19	–2.34
9600	—	—	—	0	6	–2.48	0	7	0.00	0	9	–2.34
19200	—	—	—	—	—	—	0	3	0.00	0	4	–2.34
31250	0	1	0.00	—	—	—	—	—	—	0	2	0.00
38400	—	—	—	—	—	—	0	1	0.00	—	—	—

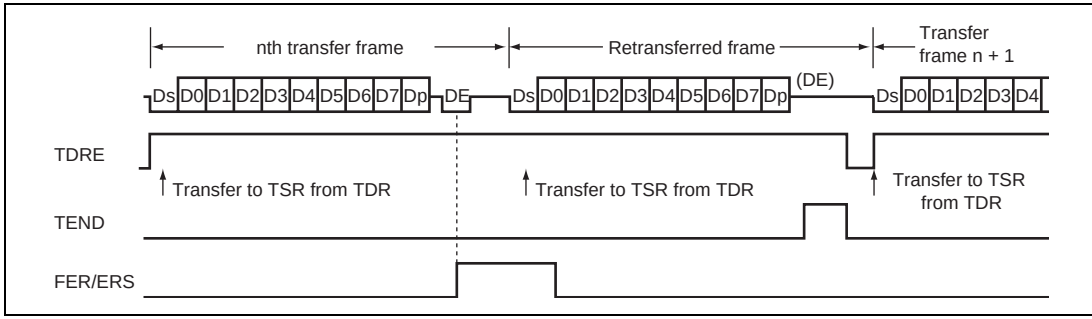


Figure 12.29 Retransfer Operation in SCI Transmit Mode

The timing for setting the TEND flag depends on the value of the GM bit in SMR. The TEND flag set timing is shown in figure 12.30.

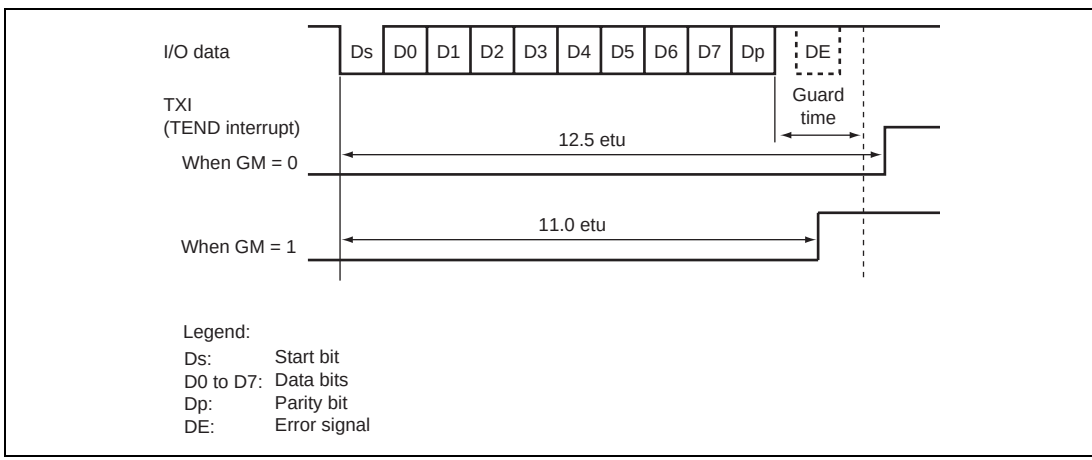


Figure 12.30 TEND Flag Generation Timing in Transmission Operation

Table 14.3 Relationship between Pin Input and UTSTR1 Monitoring Value

Pin Input		UTSTR1 Monitoring Value		Register Setting		Pin Input			UTSTR1 Monitoring Value		
VBUS	$\overline{\text{UBPM}}$	VBUS	$\overline{\text{UBPM}}$	UTSTR0/ PTSTE	UTSTR0/ SUSPEND	VBUS	USD+	USD-	RCV	VP	VM
0/1	×	0/1	×	×	×	0	×	×	0	0	0
×	0/1	×	0/1	0	×	1	0	0	×	0	0
				0	×	1	0	1	0	0	1
				0	×	1	1	0	1	1	0
				0	×	1	1	1	×	1	1
				1	0	1	0	0	×	0	0
				1	0	1	0	1	0	0	1
				1	0	1	1	0	1	1	0
				1	0	1	1	1	×	1	1
				1	1	1	0	0	0	0	0
				1	1	1	0	1	0	0	1
				1	1	1	1	0	0	1	0
				1	1	1	1	1	0	1	1

Legend:

×: Don’t care

0/1: Combination for pin input = UTSTR1 monitoring value.

(3) EP0, EP1, or EP3 DMA Transfer

(a) EPnPKTE Bits of UTRG0 (n = 0i, 1, or 3)

Note that 1 is not automatically written to EPnPKTE in case of auto-request transfer. Always write 1 to EPnPKTE by the CPU. The following example shows when 150-byte data is transmitted from EP1 to the host. In this case, 1 should be written to EP2PKTE three times as shown in figure 14.24.

(b) EP1 DMA Transfer Procedure

The DMAC transfer unit should be one packet. Therefore, set the number of transfers so that it is equal to or less than the maximum packet size of each endpoint.

1. Confirm that UIFR1/EP1EMPTY flag is 1.
2. DMAC settings for EP1 data transfer (such as auto-request and address setting).
3. Set the number of transfers for 64 bytes (the maximum packet size or less) in the DMAC.
4. Activate the DMAC (write 1 to DTE after reading DTE as 0).
5. DMA transfer.
6. Write 1 to the UTRG0/EP1PKTE bit after the DMA transfer is completed.
7. Repeat steps 1 to 6 above.
8. Confirm that UIFR1/EP1EMPTY flag is 1.
9. Set the number of transfer for 22 bytes in the DMAC.
10. Activate the DMAC (write 1 to DTE after reading DTE as 0).
11. DMA transfer.
12. Write 1 to the UTRG0/EP1PKTE bit after the DMA transfer is completed.

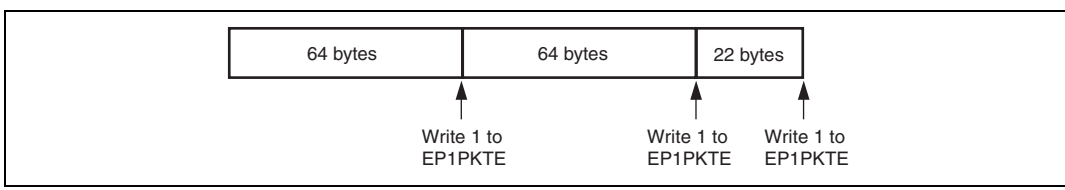


Figure 14.24 EP1PKTE Operation in UTRG0 (Auto-Request)

(4) EP0o or EP2 DMA Transfer

(a) EPnRDFN Bits of UTRG0 (n = 0o or 2)

Note that 1 is not automatically written to EPnRDFN in case of auto-request transfer. Always write 1 to EPnRDFN by the CPU. The following example shows when EP2 receives 150-byte data from the host. In this case, 1 should be written to EP2RDFN three times as shown in figure 14.25.

17.4 Input/Output Pins

The flash memory is controlled by means of the pins shown in table 17.2.

Table 17.2 Pin Configuration

Pin Name	I/O	Function	
$\overline{\text{RES}}$	Input	Reset	All
FWE	Input	Flash program/erase protection by hardware	
MD2, MD1, MD0	Input	Sets this LSI's operating mode	
PF3, PF0, P16, P14	Input	Sets this LSI's operating mode in programmer mode	
EMLE	Input	Emulator enable	
TxD2	Output	Serial transmit data output	HD64F2218, HD64F2212, HD64F2211
RxD2	Input	Serial receive data input	
USD+, USD−	Input/output	USB data input/output	HD64F2218U, HD64F2218CU, HD64F2217CU, HD64F2212U, HD64F2212CU, HD64F2211U
VBUS	Input	USB cable connect/cut detect	
$\overline{\text{UBPM}}$	Input	USB bus power mode/self power mode select	
USPND	Output	USB suspend output	
P36 (PUPD+)	Output	D+ pull-up control	

17.5 Register Descriptions

The flash memory has the following registers. For details on register addresses and register states during each processing, refer to section 21, List of Registers.

- Flash memory control register 1 (FLMCR1)
- Flash memory control register 2 (FLMCR2)
- Erase block register 1 (EBR1)
- Erase block register 2 (EBR2)
- RAM emulation register (RAMER)
- Serial control register X (SCRX)

The masked ROM version is not equipped with the above registers. Attempting to read them with produce an undetermined value, and writing to them is invalid.

17.5.1 Flash Memory Control Register 1 (FLMCR1)

FLMCR1 is a register that makes the flash memory transit to program mode, program-verify mode, erase mode, or erase-verify mode. For details on register setting, refer to section 17.8, Flash Memory Programming/Erasing.

Bit	Bit Name	Initial Value	R/W	Description
7	FWE	—*	R	Flash Write Enable Reflects the input level at the FWE pin. It is set to 1 when a low level is input to the FWE pin, and cleared to 0 when a high level is input.
6	SWE1	0	R/W	Software Write Enable When this bit is set to 1, flash memory programming/erasing is enabled. When this bit is cleared to 0, other FLMCR1 register bits and all EBR1, EBR2 bits cannot be set. [Setting condition] When FWE = 1
5	ESU1	0	R/W	Erase Setup When this bit is set to 1, the flash memory transits to the erase setup state. When it is cleared to 0, the erase setup state is cancelled. Set this bit to 1 before setting the E1 bit in FLMCR1. [Setting condition] When FWE = 1 and SWE1 = 1
4	PSU1	0	R/W	Program Setup When this bit is set to 1, the flash memory transits to the program setup state. When it is cleared to 0, the program setup state is cancelled. Set this bit to 1 before setting the P1 bit in FLMCR1. [Setting condition] When FWE = 1 and SWE1 = 1
3	EV1	0	R/W	Erase-Verify When this bit is set to 1, the flash memory transits to erase-verify mode. When it is cleared to 0, erase-verify mode is cancelled. [Setting condition] When FWE = 1 and SWE1 = 1

Section 22 Electrical Characteristics

22.1 Absolute Maximum Ratings

Table 22.1 lists the absolute maximum ratings.

Table 22.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}, $PLLV_{CC}$, DrV_{CC}	–0.3 to +4.3	V
Input voltage	V_{in}	–0.3 to V_{CC} +0.3	V
Reference voltage	V_{ref}	–0.3 to V_{CC} +0.3	V
Analog input voltage	V_{AN}	–0.3 to V_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85*	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum rating are exceeded.

Note: * The operating temperature ranges for flash memory programming/erasing are T_a = –20°C to +75°C.

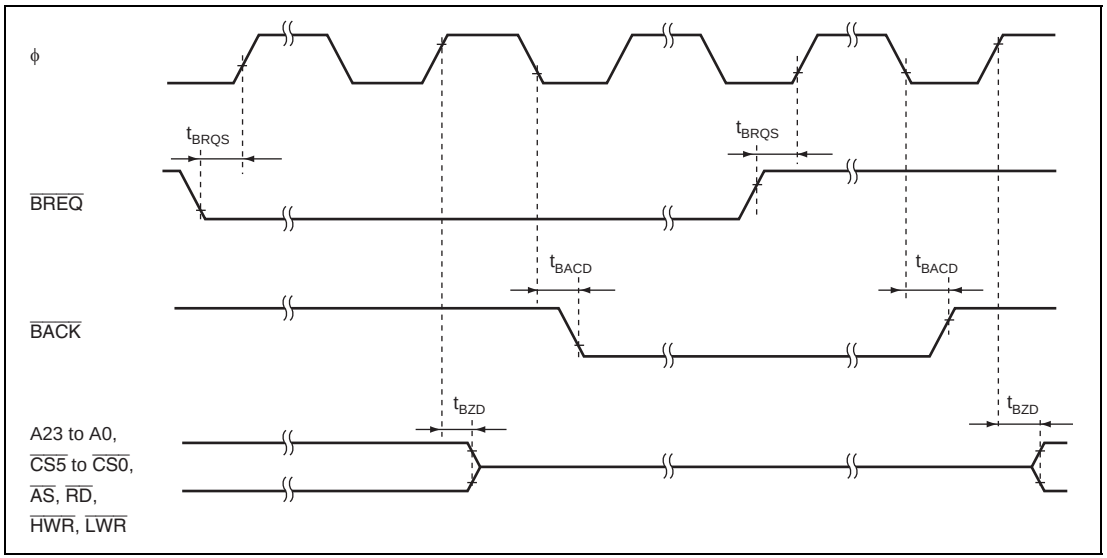


Figure 22.11 External Bus Release Timing

Product Class		Part No.	Model Name	Marking	Package (code)
H8S/2212 Group	Flash memory Version	HD64F2211U	HD64F2211UFP24	2211UFP24	64-pin LQFP (FP-64E, FP-64EV)
			HD64F2211UNP24	F2211UNP24	64-pin VQFN (TNP-64B, TNP-64BV)
		HD64F2211CU	HD64F2211CUFP24	2211CUFP24	64-pin LQFP (FP-64EV)
			HD64F2211CUNP24	F2211CUNP24	64-pin VQFN (TNP-64BV)
		HD64F2210CU	HD64F2210CUFP24	2210CUFP24	64-pin LQFP (FP-64EV)
			HD64F2210CUNP24	F2210CUNP24	64-pin VQFN (TNP-64BV)
	Masked ROM Version	HD6432211	HD6432211(***)FP	2211(***)FP	64-pin LQFP (FP-64E, FP-64EV)
			HD6432211(***)NP	2211(***)NP	64-pin VQFN (TNP-64B, TNP-64BV)
		HD6432210	HD6432210(***)FP	2210(***)FP	64-pin LQFP (FP-64E, FP-64EV)
			HD6432210(***)NP	2210(***)NP	64-pin VQFN (TNP-64B, TNP-64BV)
		HD6432210S	HD6432210S(***)FP	2210S(***)FP	64-pin LQFP (FP-64E, FP-64EV)
			HD6432210S(***)NP	2210S(***)NP	64-pin VQFN (TNP-64B, TNP-64BV)

Legend:
***: ROM code