Renesas Electronics America Inc - DF2212CUNP24V Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	24MHz
Connectivity	SCI, SmartCard, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN
Supplier Device Package	64-VQFN (8.2x8.2)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2212cunp24v

Item	Page	Revision (See Manual for Details)
Section 16 RAM	551	Table amended

Product Class		ROM Type	RAM Size	RAM Address
H8S/2218 Group	HD64F2218 HD64F2218U HD64F2218CU HD64F2217CU	Flash memory Version	12 kbytes	H'FFC000 to H'FFEFBF H'FFFFC0 to H'FFFFFF
	HD6432217	Masked ROM Version	8 kbytes	H'FFD000 to H'FFEFBF H'FFFFC0 to H'FFFFFF
H8S/2212 Group	HDF64F2212 HDF64F2212U HDF64F2212CU	Flash memory Version	12 kbytes	H'FFC000 to H'FFEFBF H'FFFFC0 to H'FFFFFF
	HD64F2211 HD64F2211U HD64F2211CU HD64F2210CU		8 kbytes	H'FFD000 to H'FFEFBF H'FFFFC0 to H'FFFFFF
	HD6432211	Masked ROM Version	8 kbytes	H'FFD000 to H'FFEFBF H'FFFFC0 to H'FFFFFF
	HD6432210 HD6432210S		4 kbytes	H'FFE000 to H'FFEFBF H'FFFFC0 to H'FFFFFF

17.1 Features	553	Table amended

- Size:

Product Class		ROM Size	ROM Address
H8S/2218 Group	HD64F2218, HD64F2218U HD64F2218CU	128 kbytes	H'000000 to H'01FFFF (Modes 6 and 7)
	HD64F2217CU	64 kbytes	H'000000 to H'00FFFF (Modes 6 and 7)
H8S/2212 Group	HD64F2212, HD64F2212U HD64F2212CU	128 kbytes	H'000000 to H'01FFFF (Mode 7)
	HD64F2211, HD64F2211U HD64F2211CU	64 kbytes	H'000000 to H'00FFFF (Mode 7)
	HD64F2210CU	32 kbytes	H'000000 to H'007FFF (Mode 7)

- Two flash memory operating modes

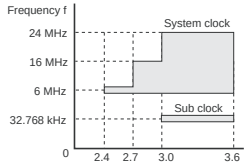
Description amended

— Boot mode

SCI boot mode: HD64F2218, HD64F2212, and HD64F2211
USB boot mode: HD64F2218U, HD64F2218CU, HD64F2217CU, HD64F2212U, HD64F2212CU, HD64F2211U, HD64F2211CU and HD64F2210CU

Item	Page	Revision (See Manual for Details)
22.2 Power Supply Voltage and Operating Frequency Range Figure 22.1 Power Supply Voltage and Operating Ranges	658	Figure amended

(1) Mask ROM versions (except for HD6432210S)



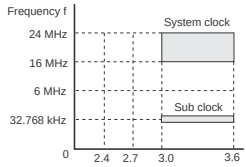
Condition A: Vcc = PLLVcc = DrVcc = 2.4 to 3.6V
Vref = 2.4V to Vcc
Vss = PLLVss = DrVss = 0V
f = 32.768 kHz, 6 MHz
Ta = -20 to +75 (Regular specifications)
Ta = -40 to +85 (Wide-range specifications)

Condition B: Vcc = PLLVcc = DrVcc = 2.7 to 3.6V
Vref = 2.7V to Vcc
Vss = PLLVss = DrVss = 0V
f = 32.768 kHz, 6 to 16 MHz
Ta = -20 to +75 (Regular specifications)
Ta = -40 to +85 (Wide-range specifications)

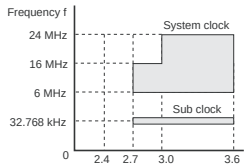
Condition C: Vcc = PLLVcc = DrVcc = 3.0 to 3.6V
Vref = 3.0V to Vcc
Vss = PLLVss = DrVss = 0V
f = 32.768 kHz, 6 to 24 MHz
Ta = -20 to +75 (Regular specifications)
Ta = -40 to +85 (Wide-range specifications)

Condition D: Vcc = PLLVcc = DrVcc = 3.0 to 3.6V
Vref = 3.0V to Vcc
Vss = PLLVss = DrVss = 0V
f = 32.768 kHz, 16 to 24 MHz
Ta = -20 to +75 (Regular specifications)
Ta = -40 to +85 (Wide-range specifications)

(2) Masked ROM version (HD6432210S)



(3) F-ZTAT versions (except for H8S/2218C, H8S/2212C)

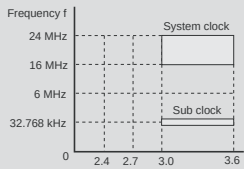


Condition A: None

Condition B: Vcc = PLLVcc = DrVcc = 2.7 to 3.6V
Vref = 2.7V to Vcc
Vss = PLLVss = DrVss = 0V
f = 32.768 kHz, 6 to 16 MHz
Ta = -20 to +75 (Regular specifications)
Ta = -40 to +85 (Wide-range specifications)

Condition C: Vcc = PLLVcc = DrVcc = 3.0 to 3.6V
Vref = 3.0V to Vcc
Vss = PLLVss = DrVss = 0V
f = 32.768 kHz, 6 to 24 MHz
Ta = -20 to +75 (Regular specifications)
Ta = -40 to +85 (Wide-range specifications)

(4) F-ZTAT versions (H8S/2218C, H8S/2212C)



Condition D: Vcc = PLLVcc = DrVcc = 3.0 to 3.6V
Vref = 3.0V to Vcc
Vss = PLLVss = DrVss = 0V
f = 32.768 kHz, 6 to 24 MHz
Ta = -20 to +75 (Regular specifications)
Ta = -40 to +85 (Wide-range specifications)

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Section 19 Clock Pulse Generator

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Type	Symbol	Pin No. TFP-100G, TFP-100GV	Pin No. BP-112, BP-112V	Pin No. FP-64E, FP-64EV, TNP-64B, TNP-64BV	I/O	Function
I/O port	P77	—	—	52	I/O	3-bit I/O pins
	P76	—	—	53		
	P75	—	—	54		
	P74	55	H9	—		
	P71	56	H10	—		
	P70	63	F11	—		
	P97	35	J5	23	Input	2-bit input pins
	P96	36	L5	24		
	PA3	98	A3	62	I/O	4-bit I/O pins for the H8S/2218 Group. 3-bit I/O pins for the H8S/2212 Group.
	PA2	99	C4	63		
	PA1	100	B3	64		
	PA0	1	B2	—		
	PB7	52	K11	—	I/O	8-bit I/O pins (Supported only by the H8S/2218 Group)
	PB6	51	K10	—		
	PB5	50	L10	—		
	PB4	49	K9	—		
	PB3	40	K6	—		
	PB2	39	L6	—		
	PB1	38	J6	—		
	PB0	37	K5	—		
	PC7	20	H1	—	I/O	8-bit I/O pins (Supported only by the H8S/2218 Group)
	PC6	19	G3	—		
	PC5	18	G2	—		
	PC4	17	G1	—		
	PC3	13	F3	—		
	PC2	12	E2	—		
	PC1	11	E1	—		
	PC0	10	E3	—		

Instruction	Size*	Function
BXOR	B	C ⊕ (<bit-No.> of <EAd>) → C Exclusive-ORs the carry flag with a specified bit in a general register or memory operand and stores the result in the carry flag.
BIXOR	B	C ⊕ ~ (<bit-No.> of <EAd>) → C Exclusive-ORs the carry flag with the inverse of a specified bit in a general register or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
BLD	B	(<bit-No.> of <EAd>) → C Transfers a specified bit in a general register or memory to the carry flag.
BILD	B	~ (<bit-No.> of <EAd>) → C Transfers the inverse of a specified bit in a general register or memory operand to the carry flag. The bit number is specified by 3-bit immediate data.
BST	B	C → (<bit-No.> of <EAd>) Transfers the carry flag value to a specified bit in a general register or memory operand.
BIST	B	~ C → (<bit-No.> of <EAd>) Transfers the inverse of the carry flag value to a specified bit in a general register or memory operand. The bit number is specified by 3-bit immediate data.

Note:* Size refers to the operand size.
B: Byte

Section 4 Exception Handling

4.1 Exception Handling Types and Priority

As table 4.1 indicates, exception handling may be caused by a reset, trace, trap instruction, or interrupt. Exception handling is prioritized as shown in table 4.1. If two or more exceptions occur simultaneously, they are accepted and processed in order of priority. Exception sources, the stack structure, and operation of the CPU vary depending on the interrupt control mode. For details on the interrupt control mode, refer to section 5, Interrupt Controller.

Table 4.1 Exception Types and Priority

Priority	Exception Type	Start of Exception Handling
High	Reset	Starts immediately after a low-to-high transition at the $\overline{\text{RES}}$ or $\overline{\text{MRES}}$* pin, or when the watchdog timer overflows. The CPU enters the reset state when the $\overline{\text{RES}}$ pin is low. The CPU enters the manual reset state when the $\overline{\text{MRES}}$ pin* is low.
	Trace	Starts when execution of the current instruction or exception handling ends, if the trace (T) bit in the EXR is set to 1. This is enabled only in trace interrupt control mode 2. Trace exception processing is not performed after RTE instruction execution.
	Interrupt	Starts when execution of the current instruction or exception handling ends, if an interrupt request has been issued. Note that after executing the ANDC, ORC, XORC, or LDC instruction or at the completion of reset exception processing, no interrupt is detected.
Low	Trap instruction (TRAPA)	Started by execution of a trap instruction (TRAPA). Trap exception processing is always accepted in program execution state.

Note: * Supported only by the H8S/2218 Group.

4.2 Exception Sources and Exception Vector Table

Different vector addresses are assigned to different exception sources. Table 4.2 lists the exception sources and their vector addresses. Since the usable modes differ depending on the product, for details on each product, refer to section 3, MCU Operating Modes.

Table 4.2 Exception Handling Vector Table

Exception Source		Vector Number	Vector Address*1	
			Normal Mode*4	Advanced Mode
Power-on reset		0	H'0000 to H'0001	H'0000 to H'0003
Manual reset		1	H'0002 to H'0003	H'0004 to H'0007
Reserved for system use		2	H'0004 to H'0005	H'0008 to H'000B
		3	H'0006 to H'0007	H'000C to H'000F
		4	H'0008 to H'0019	H'0010 to H'0013
Trace		5	H'000A to H'000B	H'0014 to H'0017
Direct transitions*2		6	H'000C to H'000D	H'0018 to H'001B
External interrupt (NMI)		7	H'000E to H'000F	H'001C to H'001F
Trap instruction	#0	8	H'0010 to H'0011	H'0020 to H'0023
	#1	9	H'0012 to H'0013	H'0024 to H'0027
	#2	10	H'0014 to H'0015	H'0028 to H'002B
	#3	11	H'0016 to H'0017	H'002C to H'002F
Reserved for system use		12	H'0018 to H'0019	H'0030 to H'0033
		13	H'001A to H'001B	H'0034 to H'0037
		14	H'001C to H'001D	H'0038 to H'003B
		15	H'001E to H'001F	H'003C to H'003F
External interrupt	IRQ0	16	H'0020 to H'0021	H'0040 to H'0043
External interrupt	IRQ1	17	H'0022 to H'0023	H'0044 to H'0047
External interrupt	IRQ2	18	H'0024 to H'0025	H'0048 to H'004B
External interrupt	IRQ3	19	H'0026 to H'0027	H'004C to H'004F
External interrupt	IRQ4	20	H'0028 to H'0029	H'0050 to H'0053
RTC interrupt	IRQ5	21	H'002A to H'002B	H'0054 to H'0057
USB interrupt	IRQ6	22	H'002C to H'002D	H'0058 to H'005B
External interrupt	IRQ7	23	H'002E to H'002F	H'005C to H'005F
Internal interrupt*3		24	H'0030 to H'0031	H'0060 to H'0063
		⎪	⎪	⎪
		127	H'00FE to H'00FF	H'01FC to H'01FF

Notes: 1. Lower 16 bits of the address.
2. For direct transfer, see section 20.10, Direct Transitions.
3. For details of internal interrupt vectors, see section 5.5, Interrupt Exception Handling Vector Table.
4. Not available in this LSI.

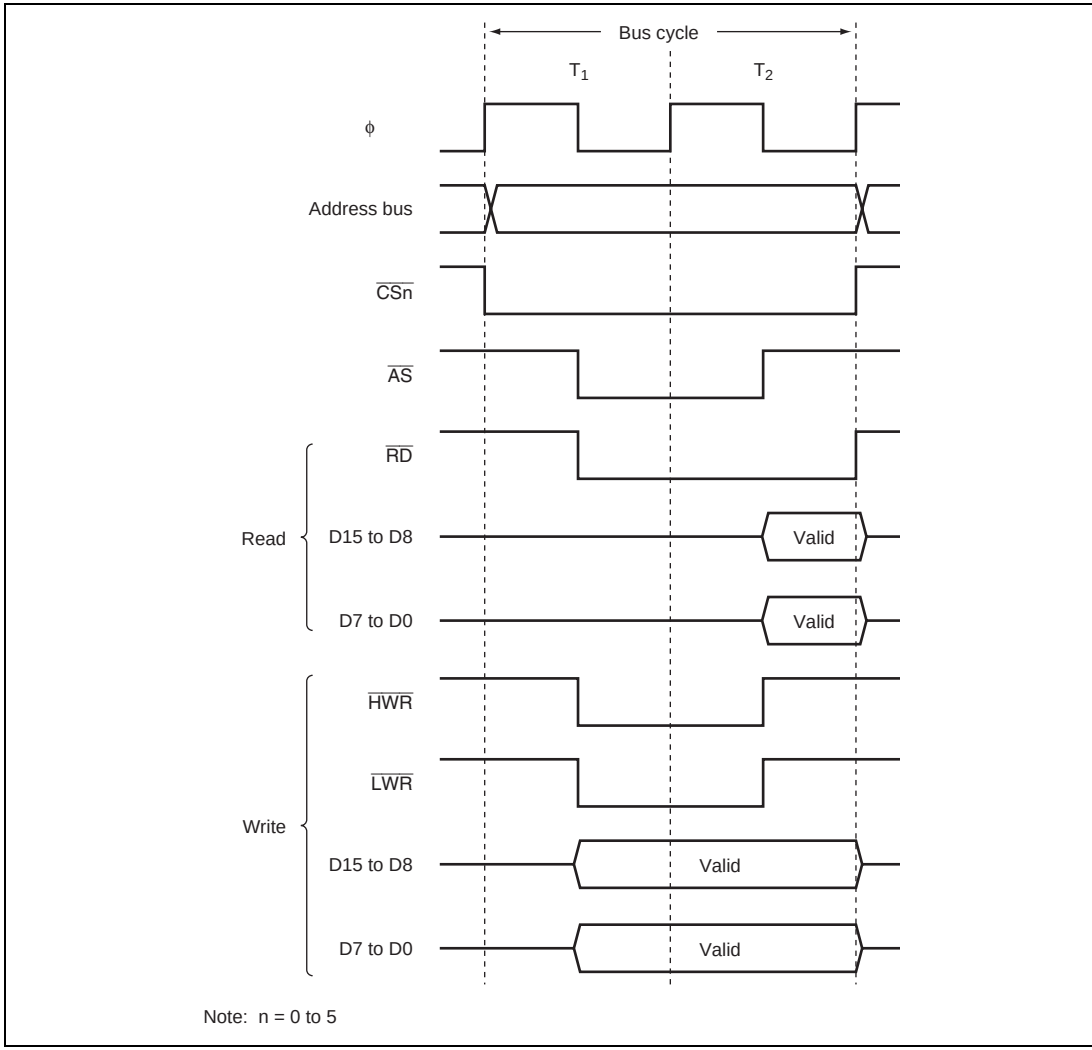
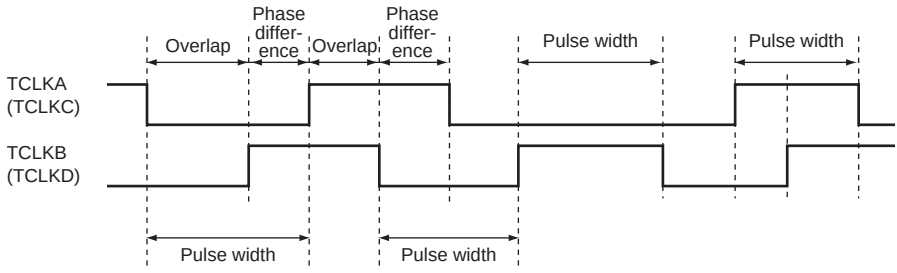


Figure 6.15 Bus Timing for 16-Bit 2-State Access Space (3) (Word Access)

9.8 Usage Notes

Input Clock Restrictions: The input clock pulse width must be at least 1.5 states in the case of single-edge detection, and at least 2.5 states in the case of both-edge detection. The TPU will not operate properly with a narrower pulse width. In phase counting mode, the phase difference and overlap between the two input clocks must be at least 1.5 states, and the pulse width must be at least 2.5 states. Figure 9.44 shows the input clock conditions in phase counting mode.



Notes: Phase difference and overlap : 1.5 states or more
Pulse width : 2.5 states or more

Figure 9.44 Phase Difference, Overlap, and Pulse Width in Phase Counting Mode

Caution on Period Setting: When counter clearing by compare match is set, TCNT is cleared in the final state in which it matches the TGR value (the point at which the count value matched by TCNT is updated). Consequently, the actual counter frequency is given by the following formula:

$$f = \frac{\phi}{(N + 1)}$$

Where f : Counter frequency
ϕ : Operating frequency
N : TGR set value

12.6.4 Serial Data Reception (Clocked Synchronous Mode)

Figure 12.21 shows an example of SCI operation for reception in clocked synchronous mode. In serial reception, the SCI operates as described below.

1. The SCI performs internal initialization synchronous with a synchronous clock input or output, starts receiving data, and stores the received data in RSR.
2. If an overrun error occurs (when reception of the next data is completed while the RDRF flag in SSR is still set to 1), the ORER bit in SSR is set to 1. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated, receive data is not transferred to RDR, and the RDRF flag remains to be set to 1.
3. If reception is completed successfully, the RDRF bit in SSR is set to 1, and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an RXI interrupt request is generated. Continuous reception is possible because the RXI interrupt routine reads the receive data transferred to RDR before reception of the next receive data has finished.

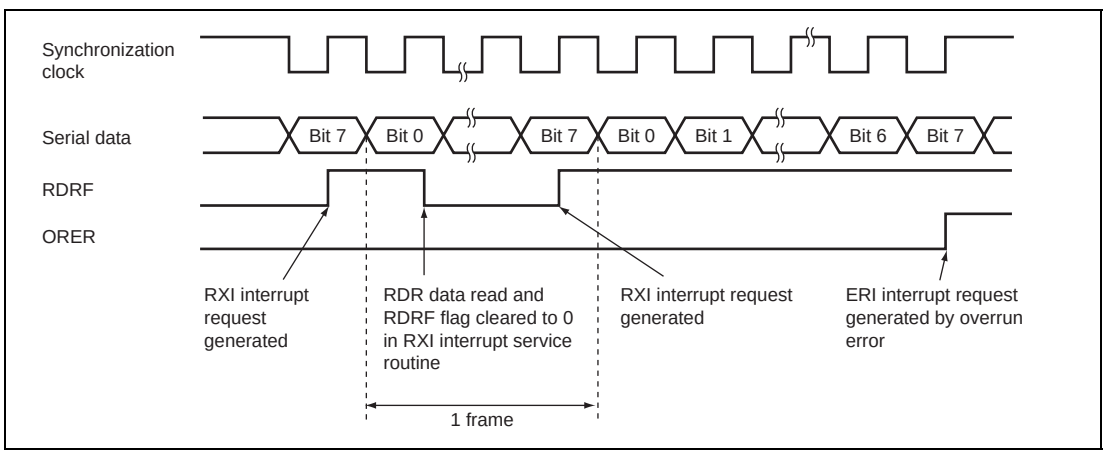
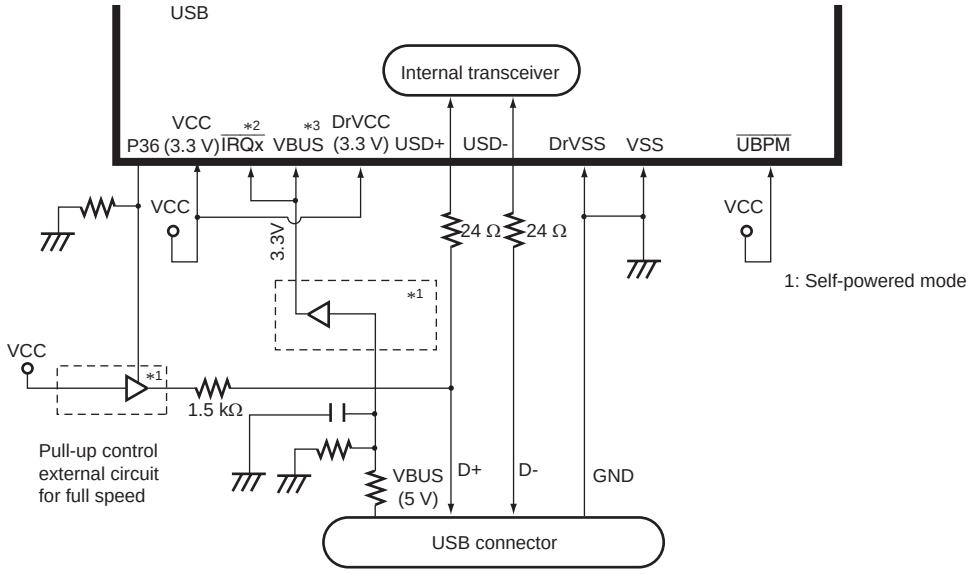


Figure 12.21 Example of SCI Operation in Reception

Reception cannot be resumed while a receive error flag is set to 1. Accordingly, clear the ORER, FER, PER, and RDRF bits to 0 before resuming reception. Figure 12.22 shows a sample flow chart for serial data reception.

When the internal clock is selected during reception, the synchronization clock will be output until an overrun error occurs or the RE bit is cleared. To receive data in frame units, a dummy data of one frame must be transmitted simultaneously.



Notes: 1. To protect the LSI, voltage applicable IC such as HD74LV-A series must be used even when the system power is turned off.
2. To cancel power-down mode by detecting the USB cable connection, theVBUS signal must be connected to the IRQx pin. Note that power-down mode state cannot be canceled by the USB interrupt EXIRQx.
3. Prevent the VBUS pin from being affected by noise while USB is in communication.

Figure 14.27 USB External Circuit in Self-Powered Mode

19.2 System Clock Oscillator

Clock pulses can be supplied by connecting a crystal resonator, or by input of an external clock.

19.2.1 Connecting a Crystal Resonator

A crystal resonator can be connected as shown in the example in figure 19.2. Select the damping resistance R_d according to table 19.1. An AT-cut parallel-resonance crystal should be used.

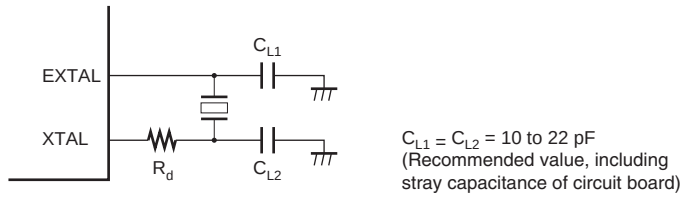


Figure 19.2 Connection of Crystal Resonator (Example)

Table 19.1 Damping Resistance Value

Frequency (MHz)	6	8	10	13	16	20	24
R_d (Ω)	300	200	100	0	0	0	0

Figure 19.3 shows the equivalent circuit of the crystal resonator. Use a crystal resonator that has the characteristics shown in table 19.2.

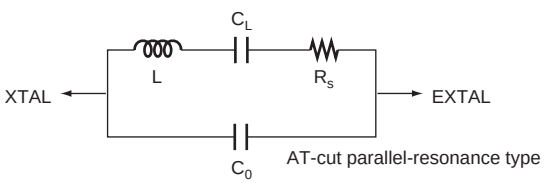


Figure 19.3 Crystal Resonator Equivalent Circuit

Table 19.2 Crystal Resonator Characteristics

Frequency (MHz)	6	8	10	13	16	20	24
R_S max (Ω)	100	80	60	60	50	40	40
C_0 max (pF)	7	7	7	7	7	7	7

20.5.3 Hardware Standby Mode Timing

Figure 20.5 shows an example of hardware standby mode timing.

When the $\overline{\text{STBY}}$ pin is driven low after the $\overline{\text{RES}}$ pin has been driven low, a transition is made to hardware standby mode. Hardware standby mode is cleared by driving the $\overline{\text{STBY}}$ pin high, waiting for the oscillation stabilization time, then changing the $\overline{\text{RES}}$ pin from low to high.

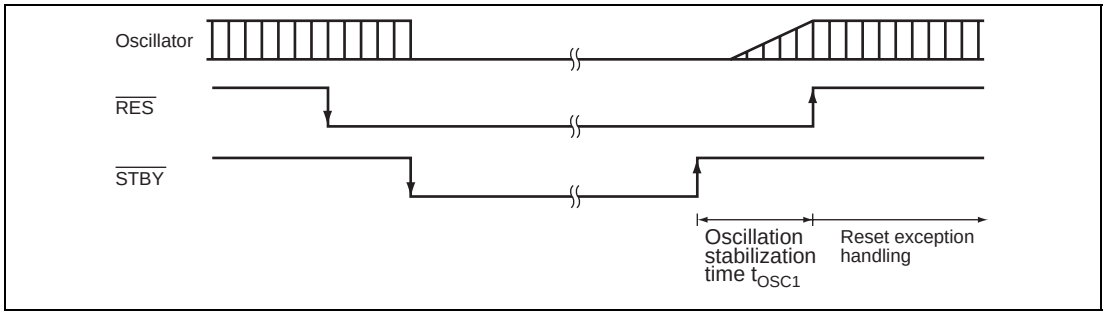


Figure 20.5 Hardware Standby Mode Timing (Example)

20.5.4 Hardware Standby Mode Timings

Timing of Transition to Hardware Standby Mode:

1. To retain RAM contents with the RAME bit set to 1 in SYSCR
   Drive the $\overline{\text{RES}}$ signal low at least 10 states before the $\overline{\text{STBY}}$ signal goes low, as shown in figure 20.6. After $\overline{\text{STBY}}$ has gone low, $\overline{\text{RES}}$ has to wait for at least 0 ns before becoming high.

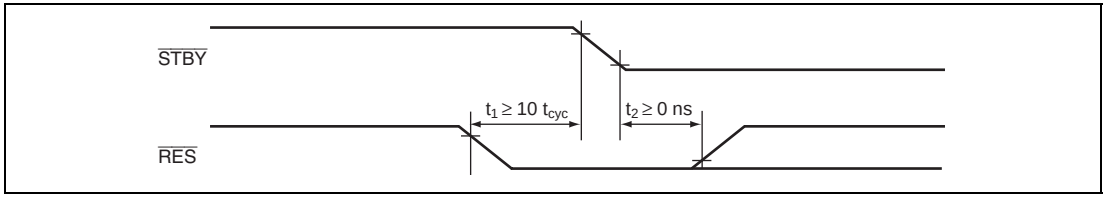


Figure 20.6 Timing of Transition to Hardware Standby Mode

2. To retain RAM contents with the RAME bit cleared to 0 in SYSCR, or when RAM contents do not need to be retained
   $\overline{\text{RES}}$ does not have to be driven low as in the above case.

21.2 Register Bits

Register bit names of the on-chip peripheral modules are described below.

Each line covers eight bits, so 16-bit registers are shown as two lines and 32-bit registers as four lines.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
UCTLR	—	USPNDE	UCKS3	UCKS2	UCKS1	UCKS0	UIFRST	UDCRST	USB
UTSTRA	—	—	—	—	—	—	—	—	
UDMAR	—	—	—	—	EP2T1	EP2T0	EP1T1	EP1T0	
UDRR	—	—	—	—	—	—	RWUPs	DVR	
UTRG0	—	—	EP2RDFN	EP1PKTE	EP3PKTE	EP0oRDFN	EP0iPKTE	EP0sRDFN	
UFCLR0	—	—	EP2CLR	EP1CLR	EP3CLR	EP0oCLR	EP0iCLR	—	
UESTL0	—	—	EP2STL	EP1STL	EP3STL	—	—	EP0STL	
UESTL1	SCME	—	—	—	—	—	—	—	
UEDR0s	D7	D6	D5	D4	D3	D2	D1	D0	
UEDR0i	D7	D6	D5	D4	D3	D2	D1	D0	
UEDR0o	D7	D6	D5	D4	D3	D2	D1	D0	
UEDR3	D7	D6	D5	D4	D3	D2	D1	D0	
UEDR1	D7	D6	D5	D4	D3	D2	D1	D0	
UEDR2	D7	D6	D5	D4	D3	D2	D1	D0	
UESZ0o	—	D6	D5	D4	D3	D2	D1	D0	
UESZ2	—	D6	D5	D4	D3	D2	D1	D0	
UIFR0	BRST	—	EP3TR	EP3TS	EP0oTS	EP0iTR	EP0iTS	SetupTS	
UIFR1	—	—	—	—	EP1ALL EMPTYs	EP2 READY	EP1TR	EP1 EMPTY	
UIFR3	CK48 READY	SOF	SETC	—	SPRSs	SPRSi	VBUSs	VBUSi	
UIER0	BRSTE	—	EP3TRE	EP3TSE	EP0oTSE	EP0iTRE	EP0iTSE	SetupTSE	
UIER1	—	—	—	—	—	EP2 READYE	EP1TRE	EP1 EMPTYE	
UIER3	CK48 READYE	SOFE	SETCE	—	—	SPRSiE	—	VBUSiE	
UISR0	BRSTS	—	EP3TRS	EP3TSS	EP0oTSS	EP0iTRS	EP0iTSS	SetupTSS	

Register Name	Power-on Reset	Manual Reset	High-Speed	Medium-Speed	Sleep	Module Stop	Watch	Subactive	Subsleep	Software Standby	Hardware Standby	Module
UTSTR0	Initialized*	—	—	—	—	—	—	—	—	—	Initialized	USB
UTSTR1	Initialized*	—	—	—	—	—	—	—	—	—	Initialized	
UTSTR2	Initialized*	—	—	—	—	—	—	—	—	—	Initialized	
UTSTRB	Initialized*	—	—	—	—	—	—	—	—	—	Initialized	
UTSTRC	Initialized*	—	—	—	—	—	—	—	—	—	Initialized	
UTSTRD	Initialized*	—	—	—	—	—	—	—	—	—	Initialized	
UTSTRE	Initialized*	—	—	—	—	—	—	—	—	—	Initialized	
UTSTRF	Initialized*	—	—	—	—	—	—	—	—	—	Initialized	
SCRX	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	FLASH
SBYCR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	SYSTEM
SYSCR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
SCKCR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
MDCR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	
MSTPCRA	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
MSTPCRB	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
MSTPCRC	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
PFCR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	BSC
LPWRCR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	SYSTEM
OUTCR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	PORT
SEMRA_0	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	SCI_0
SEMRB_0	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
ISCRH	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	INT
ISCRL	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IER	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
ISR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
P1DDR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	PORT
P3DDR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	
P7DDR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	
PADDR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	
PBDDR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	
PCDDR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	

22.4.1 Clock Timing

Table 22.4 lists the clock timing

Table 22.4 Clock Timing

Condition A: V_{CC} = PLL V_{CC} = Dr V_{CC} = 2.4 V to 3.6 V, Vref = 2.4 V to V_{CC}, V_{SS} = $PLLV_{SS}$ = Dr V_{SS} = 0 V, f = 32.768 kHz, 6 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = PLL V_{CC} = Dr V_{CC} = 2.7 V to 3.6 V, Vref = 2.7 V to V_{CC}, V_{SS} = $PLLV_{SS}$ = Dr V_{SS} = 0 V, f = 32.768 kHz, 6 MHz to 16 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = PLL V_{CC} = Dr V_{CC} = 3.0 V to 3.6 V, Vref = 3.0 V to V_{CC}, V_{SS} = $PLLV_{SS}$ = Dr V_{SS} = 0 V, f = 32.768 kHz, 6 MHz to 24 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition D: V_{CC} = PLL V_{CC} = Dr V_{CC} = 3.0 V to 3.6 V, Vref = 3.0 V to V_{CC}, V_{SS} = $PLLV_{SS}$ = Dr V_{SS} = 0 V, f = 32.768 kHz, 16 MHz to 24 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

		Condition A		Condition B		Condition C		Condition D			Test
Item	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**	**Conditions**
Clock cycle time	t_{cyc}		166.6	62.5	166.6	41.6	166.6	41.6	62.5	ns	
Clock high pulse width	t_{CH}	50	—	20	—	13	—	13	—	ns	
Clock low pulse width	t_{CL}	50	—	20	—	13	—	13	—	ns	
Clock rise time	t_{Cr}	—	25	—	10	—	7	—	7	ns	
Clock fall time	t_{Cf}	—	25	—	10	—	7	—	7	ns	
Oscillation stabilization time at reset (crystal)	t_{OSC1}	40	—	20	—	20	—	20	—	ms	Figure 22.4
Oscillation stabilization time in software standby (crystal)	t_{OSC2}	16	—	8	—	8	—	8	—	ms	Figures 20.4, 19.2 C_{L1} = C_{L2} = 10 to 22 pF
		16	—	8	—	4	—	4	—	ms	Figures 20.4, 19.2 C_{L1} = C_{L2} = 10 to 15 pF