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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	24MHz
Connectivity	SCI, SmartCard, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
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Main Revisions for This Edition

Item	Page	Revision (See Manual for Details)
1.1 Overview • On-chip memory	1	Table amended H8S/2218 Group **ROM** / **Part No.** / **ROM** / **RAM** / **Remarks** Flash memory Version / HD64F2218 / 128 kbytes / 12 kbytes / SCI boot mode HD64F2218U / 128 kbytes / 12 kbytes / USB boot mode HD64F2218CU / 128 kbytes / 12 kbytes / USB boot mode HD64F2217CU / 64 kbytes / 12 kbytes / USB boot mode Masked ROM Version / HD6432217 / 64 kbytes / 8 kbytes / —
	2	Table amended H8S/2212 Group **ROM** / **Part No.** / **ROM** / **RAM** / **Remarks** Flash memory Version / HD64F2212 / 128 kbytes / 12 kbytes / SCI boot mode HD64F2212U / 128 kbytes / 12 kbytes / USB boot mode HD64F2212CU / 128 kbytes / 12 kbytes / USB boot mode HD64F2211 / 64 kbytes / 8 kbytes / SCI boot mode HD64F2211U / 64 kbytes / 8 kbytes / USB boot mode HD64F2211CU / 64 kbytes / 8 kbytes / USB boot mode HD64F2210CU / 32 kbytes / 8 kbytes / USB boot mode Masked ROM Version / HD6432211 / 64 kbytes / 8 kbytes / — HD6432210 / 32 kbytes / 4 kbytes / — HD6432210S / 32 kbytes / 4 kbytes / —
1.2 Internal Block Diagram	3	Description amended The internal block diagram of the HD64F2218, HD64F2218U, HD64F2218CU and HD64F2217CU is shown in figure 1.1. The internal block diagram of the HD6432217 is shown in figure 1.2. The internal block diagram of the HD64F2212, HD64F2212U, HD64F2212CU, HD64F2211, HD64F2211U, HD64F2211CU and HD64F2210CU is shown in figure 1.3.

Figures

Section 1 Overview

Section 2 CPU

2.2.2 Advanced Mode

- Address Space
  Linear access is provided to a 16-Mbyte maximum address space.
- Extended Registers (En)
  The extended registers (E0 to E7) can be used as 16-bit registers, or as the upper 16-bit segments of 32-bit registers or address registers.
- Instruction Set
  All instructions and addressing modes can be used.
- Exception Vector Table and Memory Indirect Branch Addresses
  In advanced mode the top area starting at H'00000000 is allocated to the exception vector table in units of 32 bits. In each 32 bits, the upper 8 bits are ignored and a branch address is stored in the lower 24 bits (figure 2.3). For details of the exception vector table, see section 4, Exception Handling.

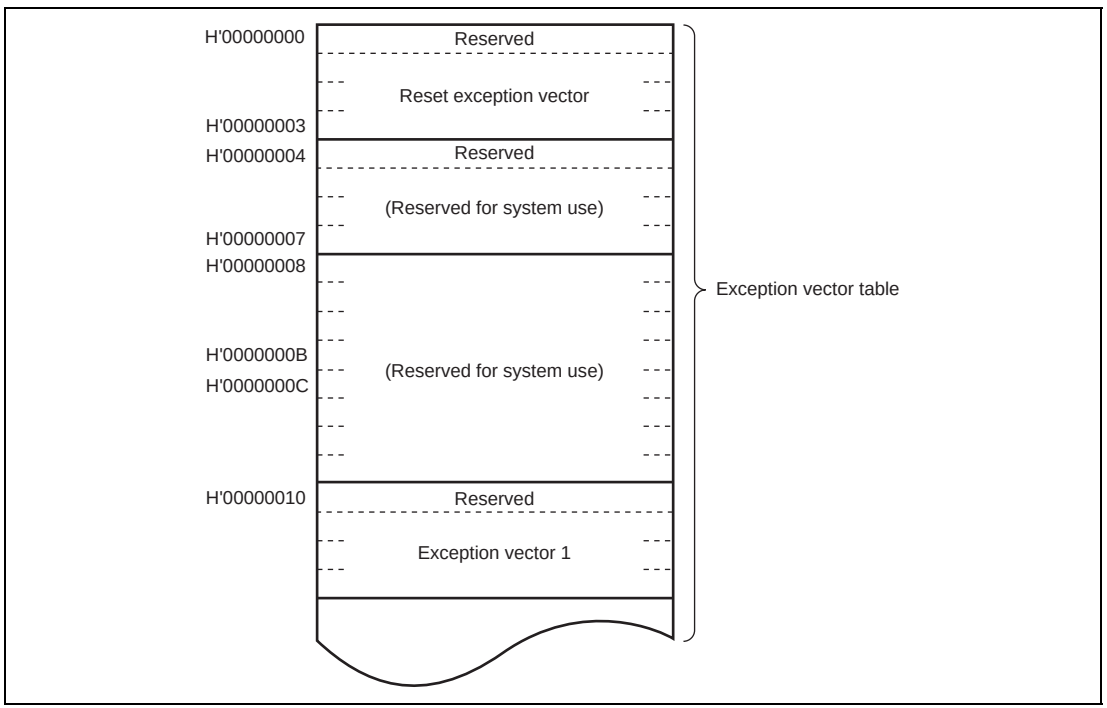


Figure 2.3 Exception Vector Table (Advanced Mode)

Table 2.3 Data Transfer Instructions

Instruction	Size*[1]	Function
MOV	B/W/L	(EAs) → Rd, Rs → (EAd) Moves data between two general registers or between a general register and memory, or moves immediate data to a general register.
MOVFPE	B	Cannot be used in this LSI.
MOVTPE	B	Cannot be used in this LSI.
POP	W/L	@SP+ → Rn Pops a general register from the stack. POP.W Rn is identical to MOV.W @SP+, Rn. POP.L ERn is identical to MOV.L @SP+, ERn
PUSH	W/L	Rn → @-SP Pushes a general register onto the stack. PUSH.W Rn is identical to MOV.W Rn, @-SP. PUSH.L ERn is identical to MOV.L ERn, @-SP.
LDM*[2]	L	@SP+ → Rn (register list) Pops two or more general registers from the stack.
STM*[2]	L	Rn (register list) → @-SP Pushes two or more general registers onto the stack.

Notes: 1. Size refers to the operand size.
B: Byte
W: Word
L: Longword
2. ER7 is used as a stack pointer in STM and LDM instructions. ER7, therefore, should not be used as a saving (STM) or restoring (LDM) register.

Section 3 MCU Operating Modes

3.1 Operating Mode Selection

This LSI supports four operating modes (modes 4 to 7). These modes enable selection of the CPU operating mode, enabling/disabling of on-chip ROM, and the initial bus width setting, by setting the mode pins (MD2 to MD0) as show in table 3.1. Modes 4 to 6 are external extended modes that allow access to the external memory and peripheral devices. In external extended mode, 8-bit or 16-bit address space can be set for each area depending on the bus controller setting after program execution starts. If 16-bit access is selected for any one area, 16-bit bus mode is set; if 8-bit access is selected for all areas, 8-bit bus mode is set. In mode 7, the external address space cannot be used. Do not change the mode pin settings during operation. Only mode 7 is available in the H8S/2212 Group.

Table 3.1 MCU Operating Mode Selection

MCU Operating Mode	MD2	MD1	MD0	CPU Operating Mode	Description	On-chip ROM	External Data Bus	
							Initial Value	Maximum Value
4	1	0	0	Advanced mode	On-chip ROM disabled, extended mode	Disabled	16 bits	16 bits
5	1	0	1	Advanced mode	On-chip ROM disabled, extended mode	Disabled	8 bits	16 bits
6	1	1	0	Advanced mode	On-chip ROM enabled, extended mode	Enabled	8 bits	16 bits
7	1	1	1	Advanced mode	Single-chip mode	Enabled	–	–

Note: When using the E6000 emulator:

- Mode 7 is not available in the H8S/2218 Group. (The E6000 emulator does not support mode 7.)
- Note following restrictions to use the RTC and USB in mode 6.
  Specify PFCR so that A9 and A8 are output on the PB1 and PB0 pins.
  Set H'FF in PCDDR so that A7 to A0 are output on the PC7 to PC0 pins.

5.2 Input/Output Pins

Table 5.1 summarizes the pins of the interrupt controller.

Table 5.1 Pin Configuration

Name	I/O	Function
NMI	Input	Nonmaskable external interrupt Rising or falling edge can be selected
$\overline{\text{IRQ7}}$	Input	Maskable external interrupts
$\overline{\text{IRQ4}}$	Input	Rising, falling, or both edges, or level sensing can be selected ($\overline{\text{IRQ6}}$ is an interrupt signal only for the on-chip USB. $\overline{\text{IRQ5}}$ is an interrupt signal only for the on-chip RTC.)
$\overline{\text{IRQ3}}$	Input	
$\overline{\text{IRQ2}}$	Input	
$\overline{\text{IRQ1}}$	Input	
$\overline{\text{IRQ0}}$	Input	

5.3 Register Descriptions

The interrupt controller has the following registers. For details on the system control register, refer to section 3.2.2, System Control Register (SYSCR).

- System control register (SYSCR)
- IRQ sense control register H (ISCRH)
- IRQ sense control register L (ISCRL)
- IRQ enable register (IER)
- IRQ status register (ISR)
- Interrupt priority register A (IPRA)
- Interrupt priority register B (IPRB)
- Interrupt priority register C (IPRC)
- Interrupt priority register D (IPRD)
- Interrupt priority register E (IPRE)
- Interrupt priority register F (IPRF)
- Interrupt priority register G (IPRG)
- Interrupt priority register J (IPRJ)
- Interrupt priority register K (IPRK)
- Interrupt priority register M (IPRM)

5.3.2 IRQ Enable Register (IER)

IER controls enabling and disabling of interrupt requests IRQ7 to IRQ0.

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ7E	0	R/W	IRQ7 Enable The IRQ7 interrupt request is enabled when this bit is 1.
6	IRQ6E	0	R/W	IRQ6 Enable*[1] The IRQ6 interrupt request is enabled when this bit is 1.
5	IRQ5E	0	R/W	IRQ5 Enable*[2] The IRQ5 interrupt request is enabled when this bit is 1.
4	IRQ4E	0	R/W	IRQ4 Enable The IRQ4 interrupt request is enabled when this bit is 1.
3	IRQ3E	0	R/W	IRQ3 Enable The IRQ3 interrupt request is enabled when this bit is 1.
2	IRQ2E	0	R/W	IRQ2 Enable The IRQ2 interrupt request is enabled when this bit is 1.
1	IRQ1E	0	R/W	IRQ1 Enable The IRQ1 interrupt request is enabled when this bit is 1.
0	IRQ0E	0	R/W	IRQ0 Enable The IRQ0 interrupt request is enabled when this bit is 1.

Notes: 1. IRQ6 is an interrupt only for the on-chip USB.
2. IRQ5 is an interrupt only for the on-chip RTC.

- The bus is transferred at a break between bus cycles. However, if a bus cycle is executed in discrete operations, as in the case of a longword-size access, the bus is not transferred between the operations.
- If the CPU is in sleep mode, it transfers the bus immediately.

DMAC: The DMAC sends the bus arbiter a request for the bus when an activation request is generated.

In the case of a USB request in short address mode or normal mode, and in cycle steal mode, the DMAC releases the bus after a single transfer.

In block transfer mode, it releases the bus after transfer of one block, and in burst mode, after completion of the transfer.

6.10.3 External Bus Release Usage Note

External bus release can be performed on completion of an external bus cycle in the H8S/2218 Group. The $\overline{CS}$ signal remains low until the end of the external bus cycle. Therefore, when external bus release is performed, the $\overline{CS}$ signal may change from the low level to the high-impedance state.

6.11 Resets and the Bus Controller

In a power-on reset, this LSI, including the bus controller, enters the reset state at that point, and an executing bus cycle is discontinued.

In a manual reset*, the bus controller's registers and internal state are maintained, and an executing external bus cycle is completed. In this case, $\overline{WAIT}$ input is ignored and write data is not guaranteed.

Note: * Supported only by the H8S/2218 Group.

8.9 Port D (H8S/2218 Group Only)

The port D is an 8-bit I/O port also functioning as data bus (D15 to D8) I/O pins. The port D has the following registers.

- Port D data direction register (PDDDR)
- Port D data register (PDDR)
- Port D register (PORTD)
- Port D pull-up MOS control register (PDPCR)

8.9.1 Port D Data Direction Register (PDDDR)

PDDDR specifies input or output for the pins of the port D.

Since PDDDR is a write-only register, the bit manipulation instructions must not be used to write PDDDR. For details, see section 2.9.4, Accessing Registers Containing Write-Only Bits.

Bit	Bit Name	Initial Value	R/W	Description
7	PD7DDR	0	W	Modes 4 to 6: Port D pins automatically function as data input/output pins. Mode 7: Setting a PDDDR bit to 1 makes the corresponding port D pin an output port, while clearing the bit to 0 makes the pin an input port.
6	PD6DDR	0	W	
5	PD5DDR	0	W	
4	PD4DDR	0	W	
3	PD3DDR	0	W	
2	PD2DDR	0	W	
1	PD1DDR	0	W	
0	PD0DDR	0	W	

8.10 Port E

The port E is an 8-bit I/O port also functioning as data bus (D7 to D0) I/O pins. The port E has the following registers.

- Port E data direction register (PEDDR)
- Port E data register (PEDR)
- Port E register (PORTE)
- Port E pull-up MOS control register (PEPCR)

8.10.1 Port E Data Direction Register (PEDDR)

PEDDR specifies input or output for the pins of the port E.

Since PEDDR is a write-only register, the bit manipulation instructions must not be used to write PEDDR. For details, see section 2.9.4, Accessing Registers Containing Write-Only Bits.

Bit	Bit Name	Initial Value	R/W	Description
7	PE7DDR	0	W	(H8S/2218 Group)
6	PE6DDR	0	W	Modes 4 to 6:
5	PE5DDR	0	W	When 8-bit bus mode is selected, port E functions as an I/O port. Setting a PEDDR bit to 1 makes the corresponding port E pin an output port, while clearing the bit to 0 makes the pin an input port.
4	PE4DDR	0	W	
3	PE3DDR	0	W	
2	PE2DDR	0	W	When 16-bit bus mode is selected, the input/output direction settings in PEDDR are ignored, and port E pins automatically function as data input/output pins. For details on 8-bit/16-bit bus mode, refer to section 6, Bus Controller.
1	PE1DDR	0	W	
0	PE0DDR	0	W	
				Mode 7: Setting a PEDDR bit to 1 makes the corresponding port E pin an output port, while clearing the bit to 0 makes the pin an input port.
				(H8S/2212 Group)
				Setting a PEDDR bit to 1 makes the corresponding port E pin an output port, while clearing the bit to 0 makes the pin an input port.

12.7.2 Data Format (Except for Block Transfer Mode)

Figure 12.25 shows the transfer data format in Smart Card interface mode.

- One frame consists of 8-bit data plus a parity bit in asynchronous mode.
- In transmission, a guard time of at least 2 etu (Elementary time unit: the time for transfer of one bit) is left between the end of the parity bit and the start of the next frame.
- If a parity error is detected during reception, a low error signal level is output for one etu period, 10.5 etu after the start bit.
- If an error signal is sampled during transmission, the same data is retransmitted automatically after a delay of 2 etu or longer.

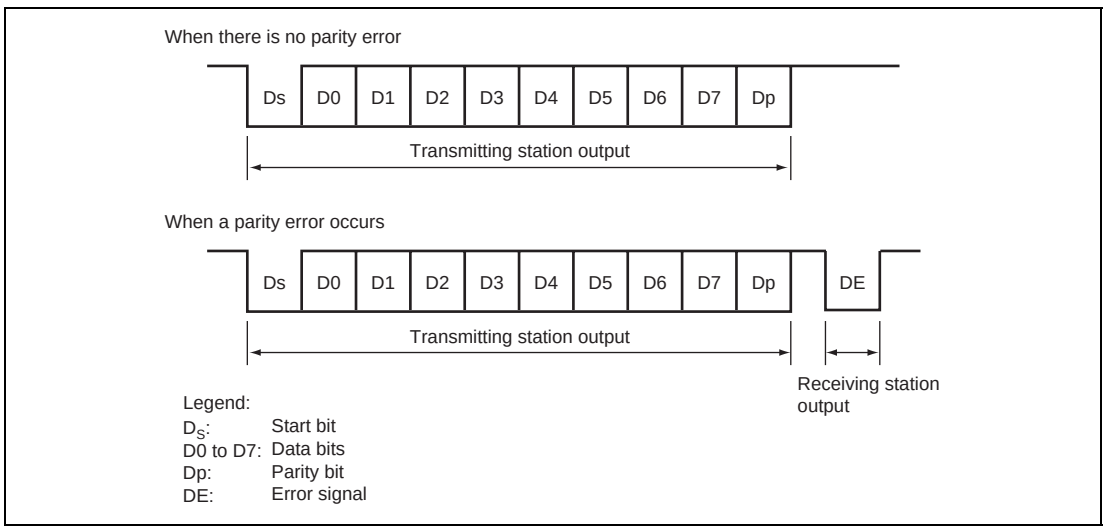


Figure 12.25 Normal Smart Card Interface Data Format

Data transfer with other types of IC cards (direct convention and inverse convention) are performed as described in the following.

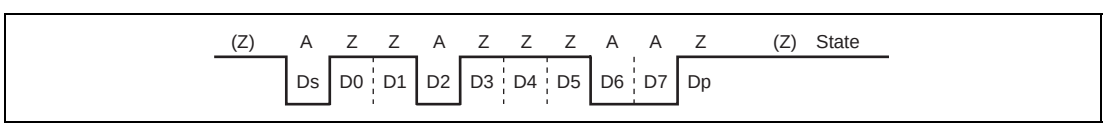


Figure 12.26 Direct Convention (SDIR = SINV = O/$\overline{E}$ = 0)

With the direction convention type IC and the above sample start character, the logic 1 level corresponds to state Z and the logic 0 level to state A, and transfer is performed in LSB-first order. The start character data above is H'3B. For the direct convention type, clear the SDIR and SINV

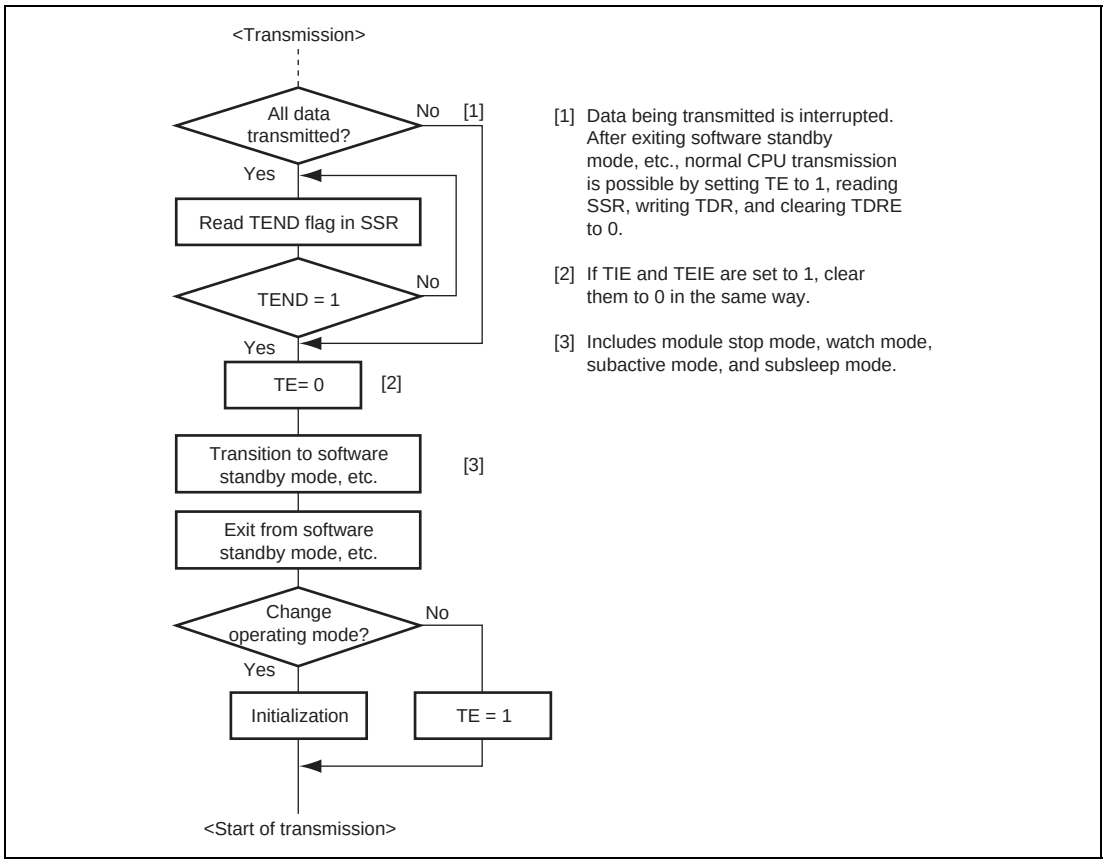


Figure 12.39 Sample Flowchart for Mode Transition during Transmission

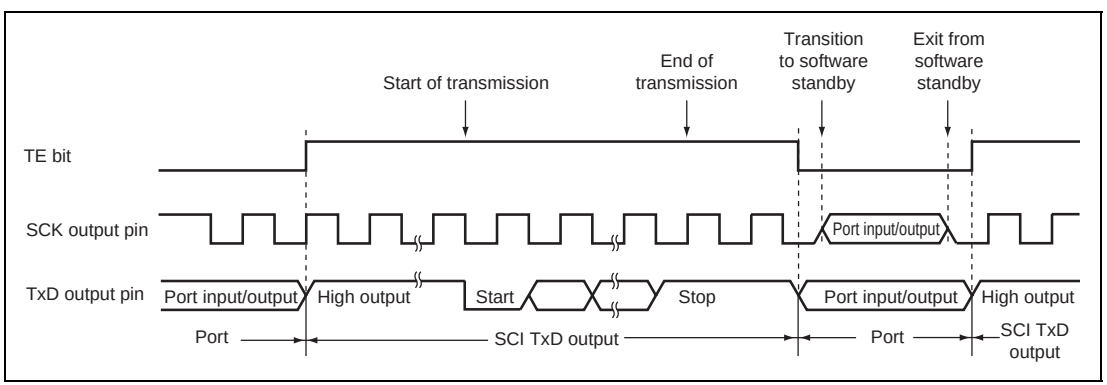


Figure 12.40 Port Pin State of Asynchronous Transmission Using Internal Clock

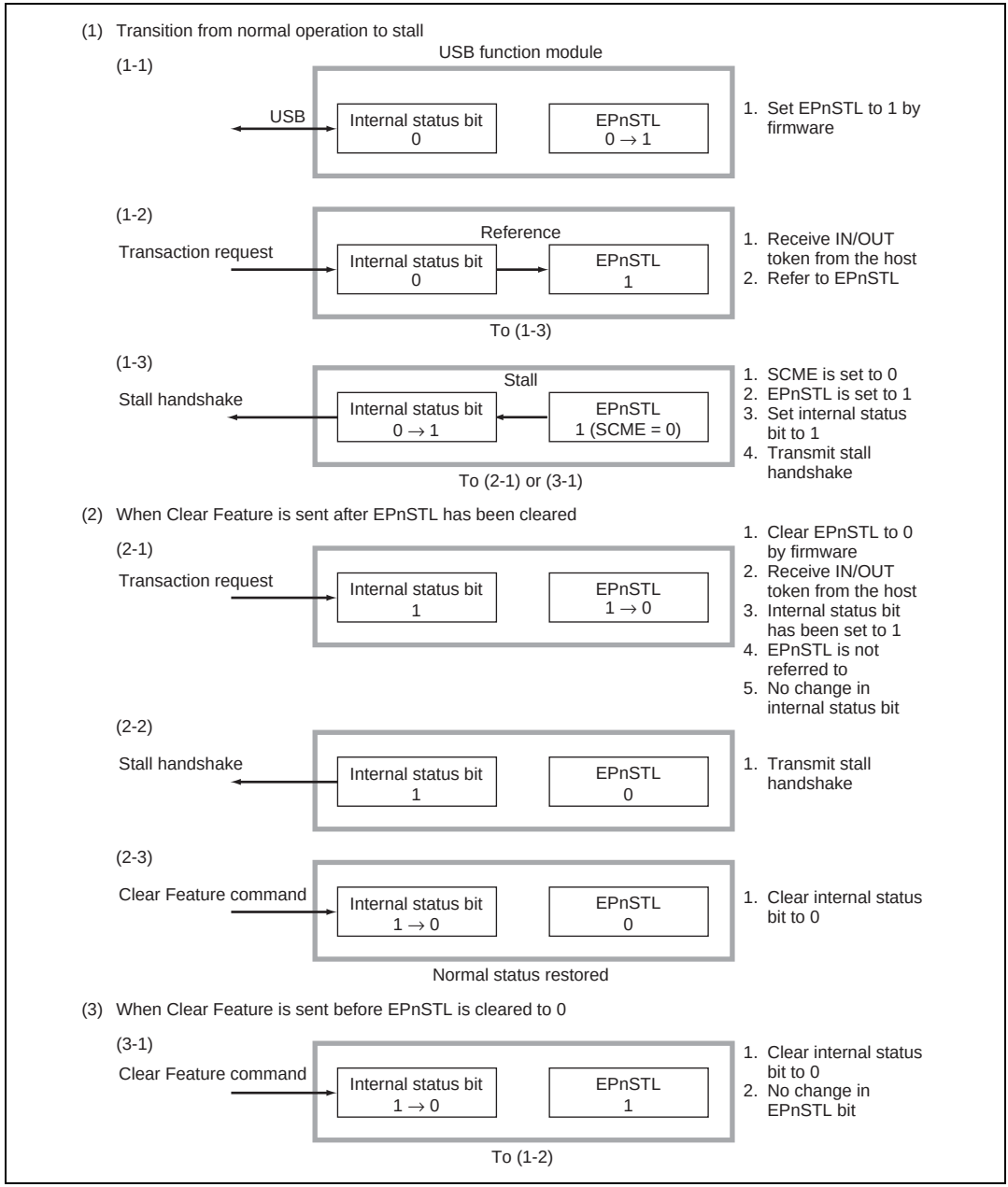
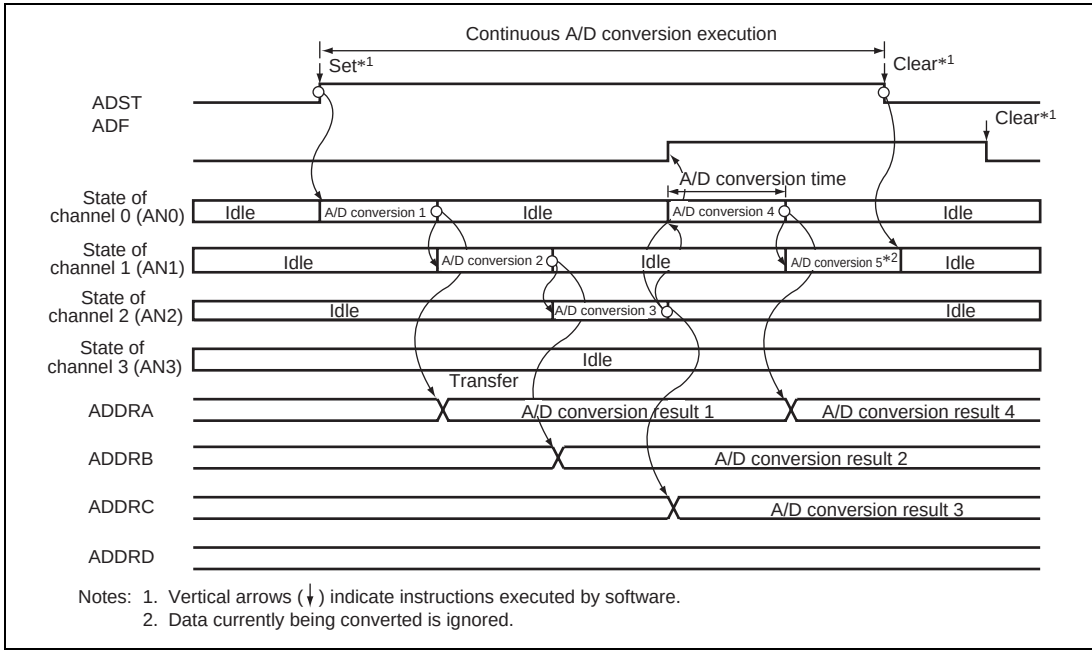


Figure 14.20 Forcible Stall by Firmware

15.5.2 Scan Mode

In scan mode, A/D conversion is to be performed sequentially on the specified channels (four channels maximum). The operations are as follows.

1. When the ADST bit is set to 1 by software, TPU or external trigger input, A/D conversion starts on the first channel in the group (AN0 when CH3 and CH2 = 00, AN4 when CH3 and CH2 = 01, or AN8 when CH3 and CH2 = 10).
2. When A/D conversion for each channel is completed, the result is sequentially transferred to the A/D data register corresponding to each channel.
3. When conversion of all the selected channels is completed, the ADF flag is set to 1. If the ADIE bit is set to 1 at this time, an ADI interrupt is requested after A/D conversion ends. Conversion of the first channel in the group starts again.
4. Steps 2 to 3 are repeated as long as the ADST bit remains set to 1. When the ADST bit is cleared to 0, A/D conversion stops.



Notes: 1. Vertical arrows (↓) indicate instructions executed by software.
2. Data currently being converted is ignored.

Figure 15.4 A/D Conversion Timing (Scan Mode, Channels AN0 to AN2 Selected)

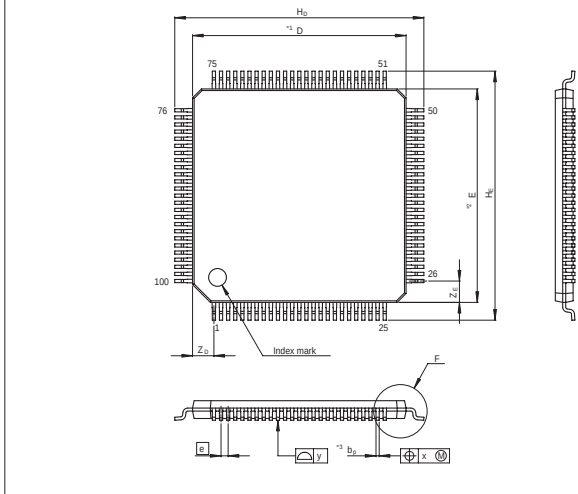
Register Name	Power-on Reset	Manual Reset	High-Speed	Medium-Speed	Sleep	Module Stop	Watch	Subactive	Subsleep	Software Standby	Hardware Standby	Module
TCR_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	TPU_1
TMDR_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TIOR_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TIER_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TSR_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TCNT_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TGRA_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TGRB_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TCR_2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	TPU_2
TMDR_2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TIOR_2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TIER_2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TSR_2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TCNT_2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TGRA_2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TGRB_2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
EXMDLSTP	Initialized	—	—	—	—	—	—	—	—	—	Initialized	SYSTEM
RSECDR	—	—	—	—	—	—	—	—	—	—	Initialized	RTC
RMINDR	—	—	—	—	—	—	—	—	—	—	Initialized	
RHRDR	—	—	—	—	—	—	—	—	—	—	Initialized	
RWKDR	—	—	—	—	—	—	—	—	—	—	Initialized	
RTCCR1	—	—	—	—	—	—	—	—	—	—	Initialized	
RTCCR2	—	—	—	—	—	—	—	—	—	—	Initialized	
RTCCSR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	
DMACR0A	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	DMAC
DMACR0B	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
DMACR1A	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
DMACR1B	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
DMABCR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TCSR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	WDT
TCNT	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
RSTCSR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	

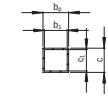
Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD2 to MD0, $\overline{TRST}$, TCK, TMS, TDI, EMLE, VBUS, $\overline{UBPM}$, FWE*[4]	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	EXTAL, NMI, ports 1, 3, 4, 7, 9, and A to G		–0.3	—	$V_{CC} \times 0.2$	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 0.8 mA
Input leakage current	$\overline{RES}$, VBUS, $\overline{UBPM}$, $\overline{STBY}$, NMI, EMLE, MD2 to MD0, FWE*[4], ports 4, 9	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
Three-state leakage current (off state)	Ports 1, 3, 7, and A to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
Input pull-up MOS current	Ports A to E TDI, TCK, TMS, $\overline{TRST}$	$-I_P$	10	—	300	µA	V_{in} = 0 V
Input capacitance	$\overline{RES}$, NMI	C_{in}	—	—	30	pF	V_{in} = 0 V f = 1 MHz
	All input pins other than $\overline{RES}$, NMI		—	—	15	pF	T_a = 25°C
Current dissipation*[1]	Normal operation	I_{CC}*[2]	—	22 V_{CC} = 3.3 V	35 V_{CC} = 3.6 V	mA	f = 16 MHz
	(USB halts)		—	31 V_{CC} = 3.3 V	50 V_{CC} = 3.6 V	mA	f = 24 MHz

C. Package Dimensions

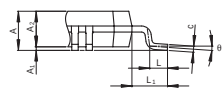
The package dimension that is shown in the Renesas Semiconductor Package Data Book has priority.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TQFP100-12x12-0.40	PTQP0100LC-A	TFP-100G/TFP-100GV	0.4g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS"*1"AND"*2" DO NOT INCLUDE MOLD FLASH
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	12	—
E	—	12	—
A_2	—	1.00	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.20
A_1	0.00	0.10	0.20
b_p	0.13	0.18	0.23
b_1	—	0.16	—
c	0.12	0.17	0.22
c_1	—	0.15	—
θ	0°	—	8°
e	—	0.4	—
x	—	—	0.07
y	—	—	0.10
Z_D	—	1.2	—
Z_E	—	1.2	—
L	0.4	0.5	0.6
L_1	—	1.0	—

Figure C.1 TFP-100G and TFP-100GV Package Dimensions