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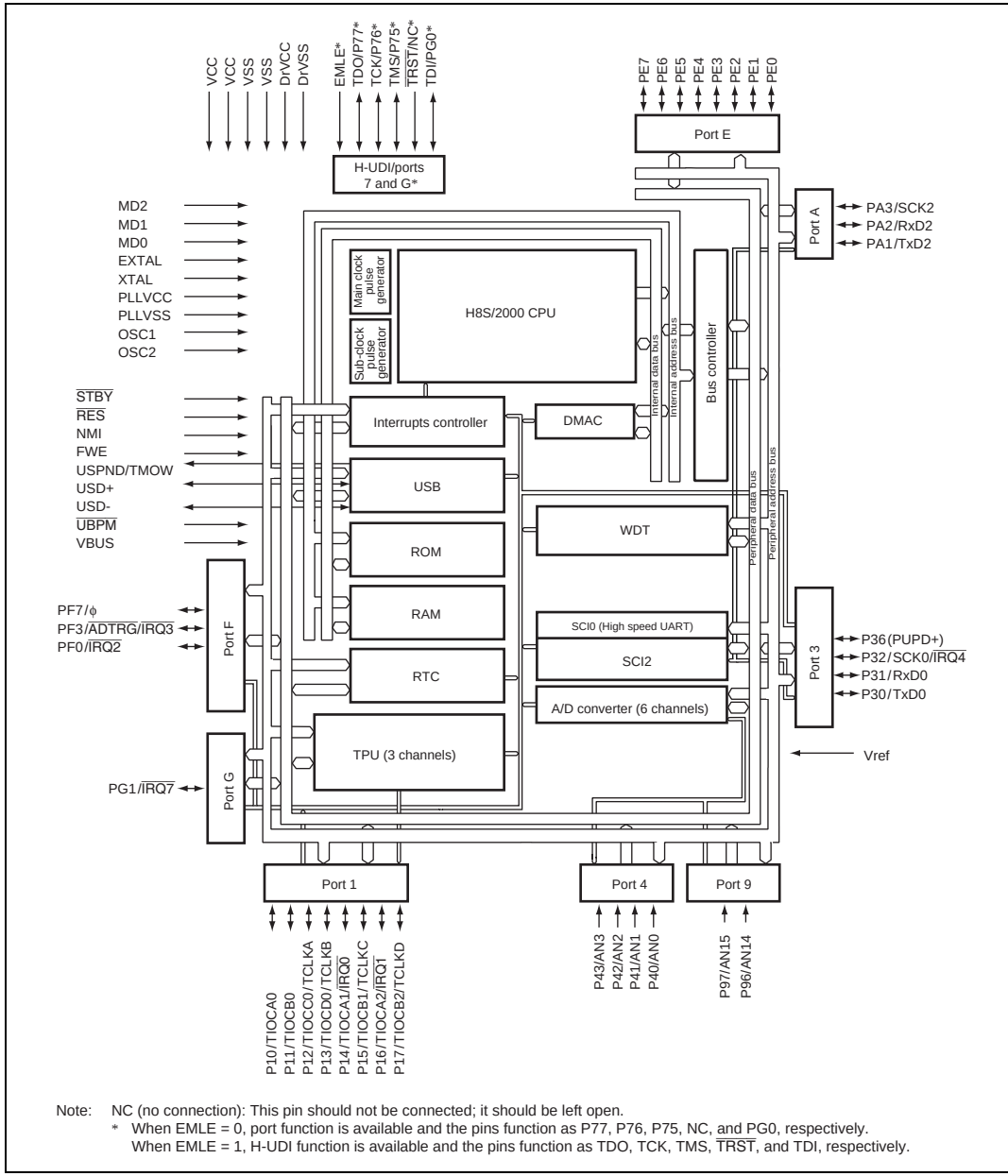
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	24MHz
Connectivity	SCI, SmartCard, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	69
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2217cubr24v



Note: NC (no connection): This pin should not be connected; it should be left open.
* When EMLE = 0, port function is available and the pins function as P77, P76, P75, NC, and PG0, respectively.
When EMLE = 1, H-UDI function is available and the pins function as TDO, TCK, TMS, TRST, and TDI, respectively.

Figure 1.3 Internal Block Diagram of HD64F2212, HD64F2212U, HD64F2212CU, HD64F2211, HD64F2211U, HD64F2211CU and HD64F2210CU

4.8 Notes on Use of the Stack

When accessing word data or longword data, this LSI assumes that the lowest address bit is 0. The stack should always be accessed by word transfer instruction or longword transfer instruction, and the value of the stack pointer (SP: ER7) should always be kept even. Use the following instructions to save registers:

PUSH.W Rn (or MOV.W Rn, @-SP)
PUSH.L ERn (or MOV.L ERn, @-SP)

Use the following instructions to restore registers:

POP.W Rn (or MOV.W @SP+, Rn)
POP.L ERn (or MOV.L @SP+, ERn)

Setting SP to an odd value may lead to a malfunction. Figure 4.4 shows an example of what happens when the SP value is odd.

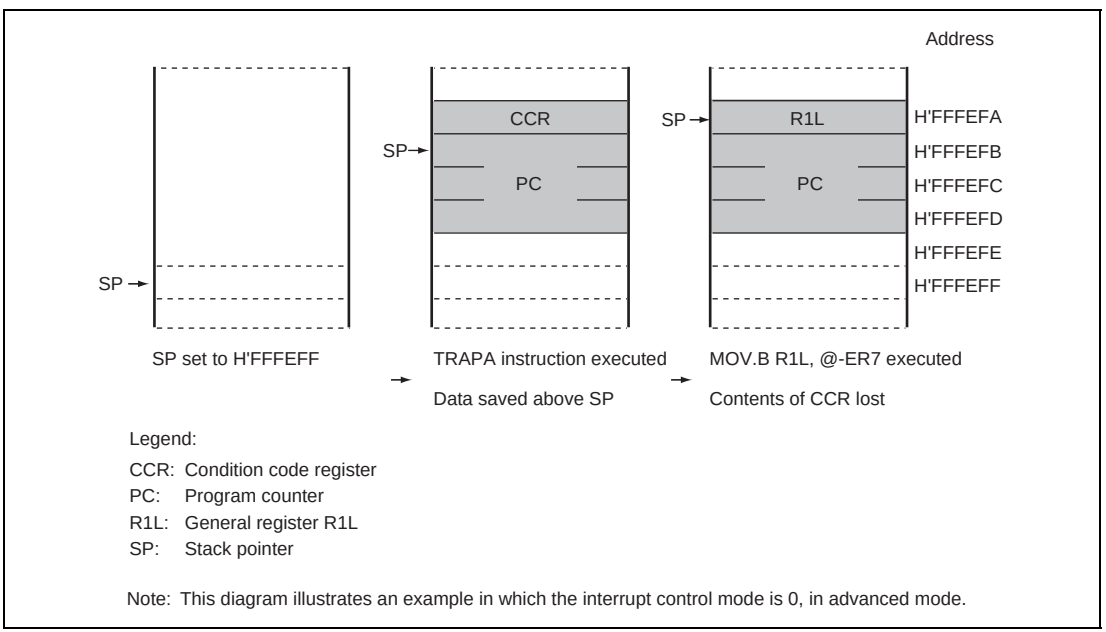


Figure 4.4 Operation when SP Value Is Odd

7. The CPU generates a vector address for the accepted interrupt and starts execution of the interrupt handling routine at the address indicated by the contents of the vector address in the vector table.

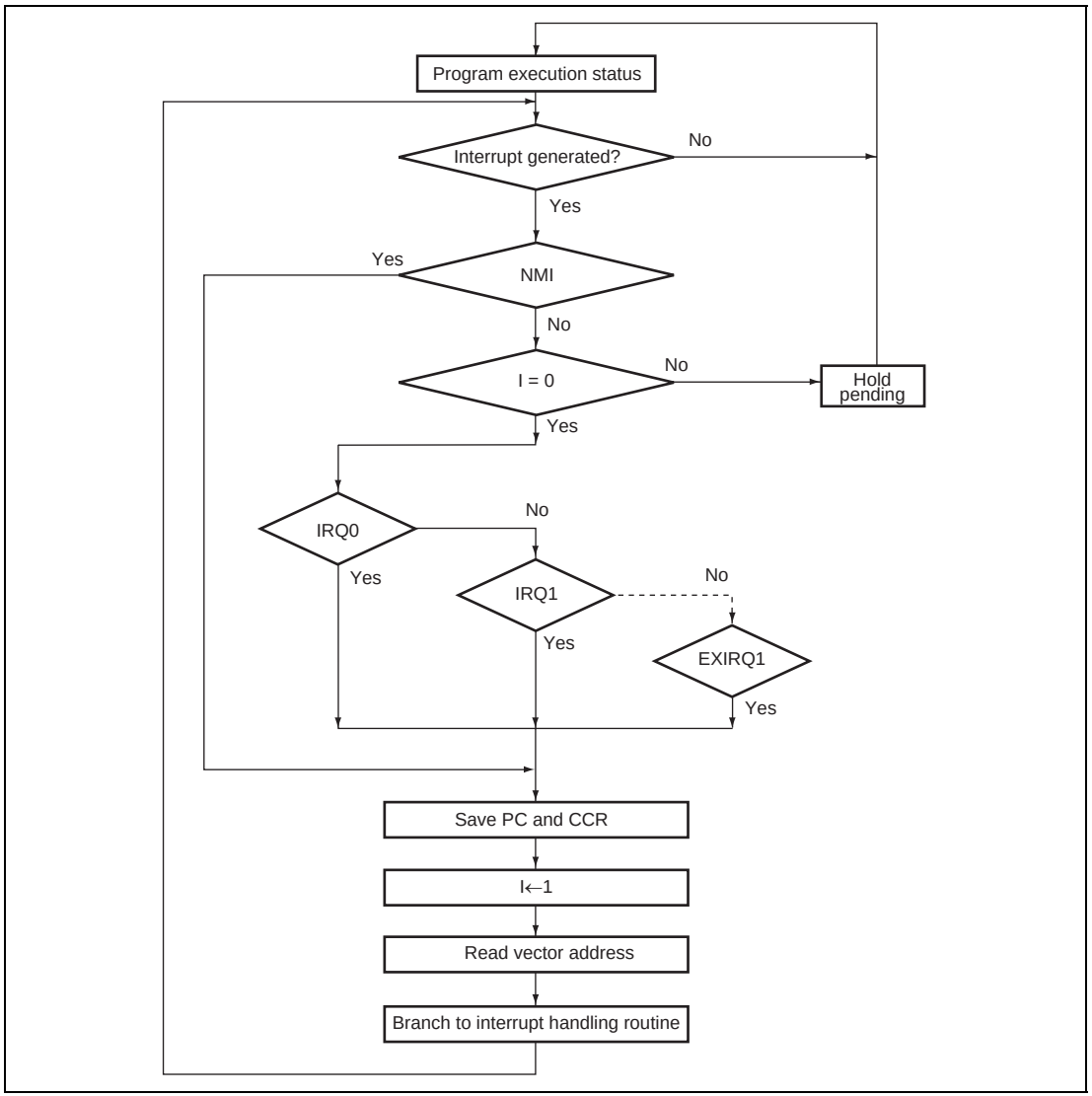


Figure 5.4 Flowchart of Procedure Up to Interrupt Acceptance in Interrupt Control Mode 0

8-Bit 3-State Access Space (Area 6 and RTC): Figure 6.12 shows the bus timing for area 6 and RTC area (address = H'FFFF40 to H'FFFF5F). When the areas are accessed, the data bus cannot be used.

Wait states cannot be inserted.

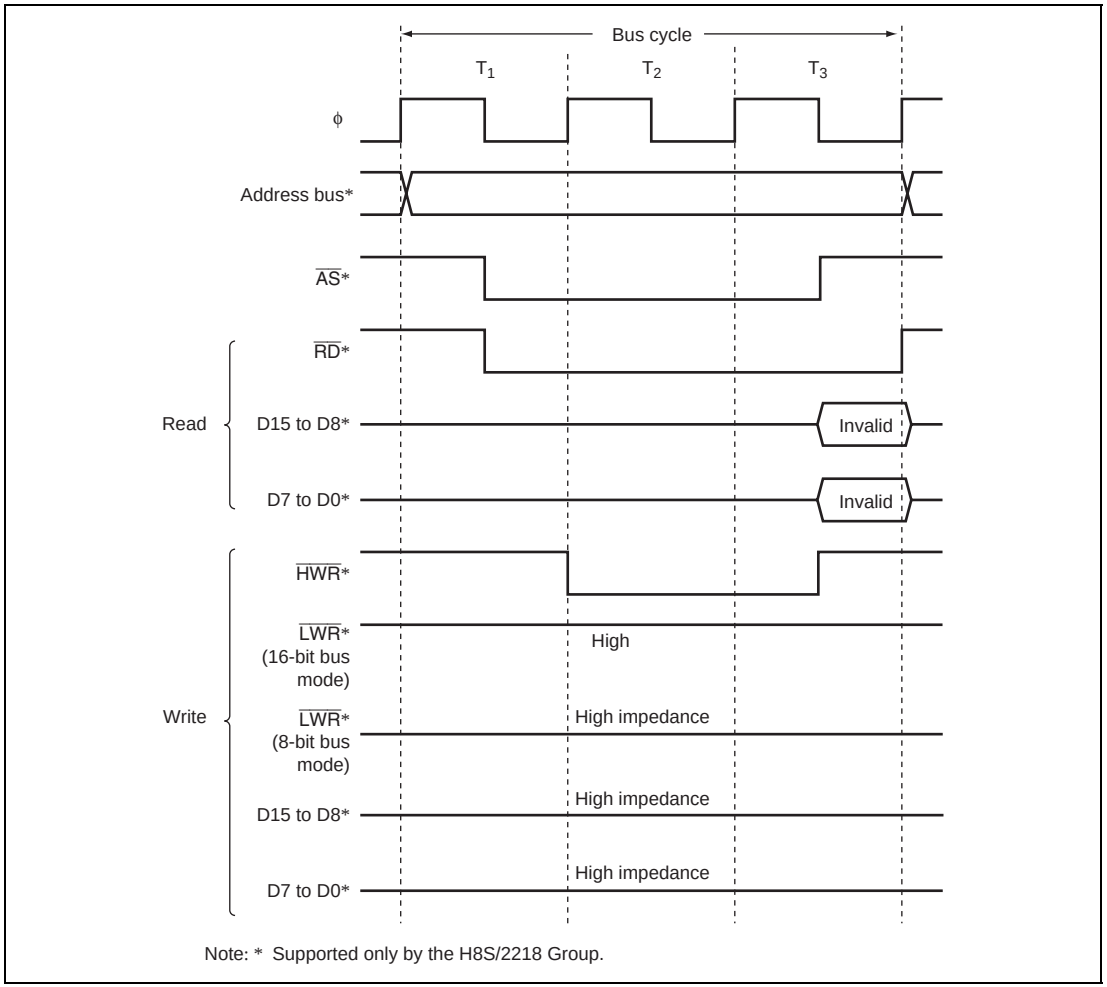


Figure 6.12 Bus Timing for Area 6 and RTC

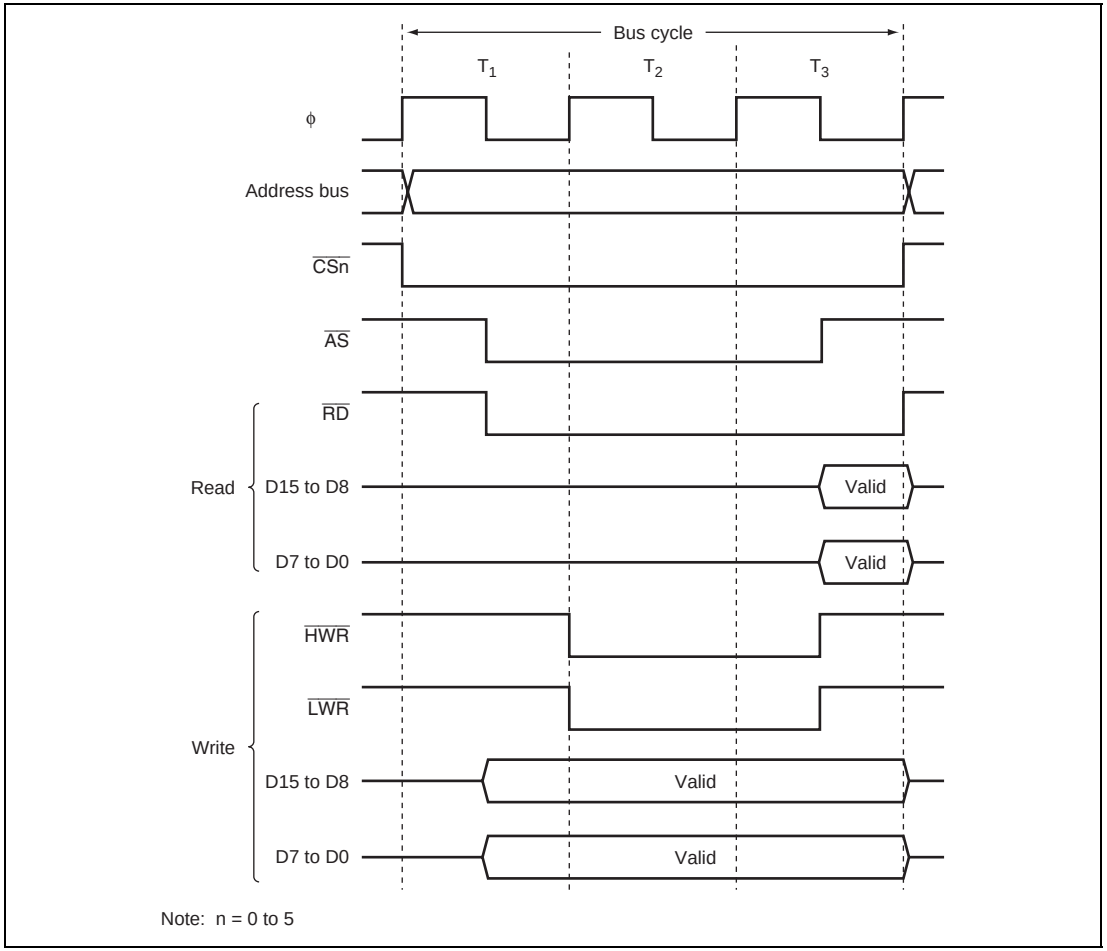


Figure 6.18 Bus Timing for 16-Bit 3-State Access Space (3) (Word Access)

6.7 Burst ROM Interface

With the H8S/2218 Group, external space area 0 can be designated as burst ROM space, and burst ROM interfacing can be performed. The burst ROM space interface enables 16-bit configuration ROM with burst access capability to be accessed at high speed.

Area 0 can be designated as burst ROM space by means of the BRSTRM bit in BCRH.

Consecutive burst accesses of a maximum of 4 words or 8 words can be performed for CPU instruction fetches only. One or two states can be selected for burst access.

6.7.1 Basic Timing

The number of states in the initial cycle (full access) of the burst ROM interface is in accordance with the setting of the AST0 bit in ASTCR. Also, when the AST0 bit is set to 1, wait state insertion is possible. One or two states can be selected for the burst cycle, according to the setting of the BRSTS1 bit in BCRH. Wait states cannot be inserted. When area 0 is designated as burst ROM space, it becomes 16-bit access space regardless of the setting of the ABW0 bit in ABWCR.

When the BRSTS0 bit in BCRH is cleared to 0, burst access of up to 4 words is performed; when the BRSTS0 bit is set to 1, burst access of up to 8 words is performed.

The basic access timing for burst ROM space is shown in figures 6.20 and 6.21. The timing shown in figure 6.20 is for the case where the AST0 and BRSTS1 bits are both set to 1, and that in figure 6.21 is for the case where both these bits are cleared to 0.

8.2 Port 3

The port 3 is a 4-bit I/O port also functioning as the SCI I/O pins and external interrupt input ($\overline{IRQ4}$) pins. The port 3 of the H8S/2218 Group has the same function as that of the H8S/2212 Group. The port 3 has the following registers.

- Port 3 data direction register (P3DDR)
- Port 3 data register (P3DR)
- Port 3 register (PORT3)
- Port 3 open-drain control register (P3ODR)

8.2.1 Port 3 Data Direction Register (P3DDR)

P3DDR specifies input or output for the pins of the port 3.

Since P3DDR is a write-only register, the bit manipulation instructions must not be used to write P3DDR. For details, see section 2.9.4, Accessing Registers Containing Write-Only Bits.

Bit	Bit Name	Initial Value	R/W	Description
7	—	Undefined	—	Reserved This bit is undefined and cannot be modified.
6	P36DDR	0	W	Setting a P3DDR bit to 1 makes the corresponding port 3 pin an output pin, while clearing the bit to 0 makes the pin an input pin.
5 to 3	—	Undefined	—	Reserved These bits are undefined and cannot be modified.
2	P32DDR	0	W	Setting a P3DDR bit to 1 makes the corresponding port 3 pin an output pin, while clearing the bit to 0 makes the pin an input pin.
1	P31DDR	0	W	
0	P30DDR	0	W	

Table 8.27 P76 Pin Function

EMLE	0		1
P76DDR	0	1	—
Pin Function	P76 input pin	P76 output pin	TCK input pin

Table 8.28 P75 Pin Function

EMLE	0		1
P75DDR	0	1	—
Pin Function	P75 input pin	P75 output pin	TMS input pin

8.5 Port 9

The port 9 is a 2-bit input port also functioning as A/D converter analog input pins. The port 9 of the H8S/2218 Group has the same function as that of the H8S/2212 Group.

- Port 9 register (PORT9)

8.5.1 Port 9 Register (PORT9)

PORT9 indicates the pin states of the port 9.

Bit	Bit Name	Initial Value	R/W	Description
7	P97	—*	R	The pin states are always read when these bits are read.
6	P96	—*	R	
5 to 0	—	Undefined	—	Reserved These bits are undefined.

Note: * Determined by the states of pins P97 and P96.

8.5.2 Pin Function

The port 9 also functions as A/D converter analog input (AN15 and AN14) pins.

Table 8.31 PA1 Pin Function

Operating mode	Modes 4 to 6				Mode 7		
AE3 to AE0	B'101× or B'11××	Other than B'101× or B'11××			—		
TE in SCR_2	—	0		1	0		1
PA1DDR	—	0	1	—	0	1	—
Pin Function	A17 output pin	PA1 input pin	PA1 output pin	TxD2 output pin	PA1 input pin	PA1 output pin	TxD2 output pin

Table 8.32 PA0 Pin Function

Operating mode	Modes 4 to 6			Mode 7	
AE3 to AE0	Other than B'0××× or B'1000	B'0××× or B'1000		—	
PA0DDR	—	0	1	0	1
Pin Function	A16 output pin	PA0 input pin	PA0 output pin	PA0 input pin	PA0 output pin

Legend:
×: Don't care.

Pin Functions of H8S/2212 Group

Port A pins also function as SCI_2 I/O pins. The correspondence between the register specification and the pin functions is shown below.

Table 8.33 PA3 Pin Function

CKE1 in SCR_2	0				1
C/$\overline{A}$ in SMR_2	0			1	—
CKE0 in SCR_2	0		1	—	—
PA3DDR	0	1	—	—	—
Pin Function	PA3 input pin	PA3 output pin	SCK2 output pin	SCK2 output pin	SCK2 input pin

Table 8.66 PE5 Pin Function

Operating Mode	Modes 4 to 6			Mode 7	
Bus Mode	8-bit bus mode		16-bit bus mode	—	
PE5DDR	0	1	—	0	1
Pin Function	PE5 input pin	PE5 output pin	D5 input/output pin	PE5 input pin	PE5 output pin

Table 8.67 PE4 Pin Function

Operating Mode	Modes 4 to 6			Mode 7	
Bus Mode	8-bit bus mode		16-bit bus mode	—	
PE4DDR	0	1	—	0	1
Pin Function	PE4 input pin	PE4 output pin	D4 input/output pin	PE4 input pin	PE4 output pin

Table 8.68 PE3 Pin Function

Operating Mode	Modes 4 to 6			Mode 7	
Bus Mode	8-bit bus mode		16-bit bus mode	—	
PE3DDR	0	1	—	0	1
Pin Function	PE3 input pin	PE3 output pin	D3 input/output pin	PE3 input pin	PE3 output pin

Table 8.69 PE2 Pin Function

Operating Mode	Modes 4 to 6			Mode 7	
Bus Mode	8-bit bus mode		16-bit bus mode	—	
PE2DDR	0	1	—	0	1
Pin Function	PE2 input pin	PE2 output pin	D2 input/output pin	PE2 input pin	PE2 output pin

Table 11.3 Operating State in Each Mode

Function	High-Speed	Medium-Speed	Sleep	Module Stop	Watch	Subactive	Subsleep	Software Standby	Hard-ware Standby
Clock operation	Subclock operation	Subclock operation	Subclock operation	Halted (Retained)	Subclock operation	Subclock operation	Subclock operation	Subclock operation	Halted (Reset)
Free running timer operation	Operating	Operating	Operating	Halted (Retained)	Halted (Retained)	Halted (Retained)	Halted (Retained)	Halted (Retained)	Halted (Reset)

11.7 Usage Notes

(1) Notes on Using the Emulator

In the E6000 emulator the RTC module is mounted on an external extended board. Since it must be accessed as an external module, the limitations listed below apply. These limitations do not apply to the E10A or to product chips.

- RTC operation is not supported in the H8S/2218 Group's mode 7 (single-chip mode).
- When using the RTC module in the H8S/2218 Group's mode 6 (on-chip ROM-enabled mode) or the H8S/2212 Group's mode 7 (single-chip mode), A7 to A0 are input pins in the initial status. Therefore, A7 to A0 must be set as output pins by setting PC7DDR to PC0DDR to H'FF before accessing the RTC module.
- The above setting is not necessary when using the RTC module in the H8S/2218 Group's modes 4 and 5 (on-chip ROM-disabled mode) because A7 to A0 are output pins.

(2) Bus Interface

The bus interface of the module conforms to the bus specifications for external area 7. Consequently, before accessing the RTC module, area 7 must be specified as having an 8-bit bus width and 3-state access using the bus controller register.

(3) Method for Reading Pin States Using the Port D Register (PORTD)

First access EXMDLSTP or the RTC register (address range: H'FFFF40 to H'FFFF5F). Then, you must perform a dummy read to the external address space (such as H'FFEF00 to H'FF7FF) outside the range H'FFFF40 to H'FFFF5F before reading PORTD.

12.7.6 Initialization

Before transmitting and receiving data, initialize the SCI as described below. Initialization is also necessary when switching from transmit mode to receive mode, or vice versa.

1. Clear the TE and RE bits in SCR to 0.
2. Clear the error flags ERS, PER, and ORER in SSR to 0.
3. Set the GM, BLK, O/$\overline{E}$, BCP0, BCP1, CKS0, CKS1 bits in SMR. Set the PE bit to 1.
4. Set the SMIF, SDIR, and SINV bits in SCMR.
   When the SMIF bit is set to 1, the TxD and RxD pins are both switched from ports to SCI pins, and are placed in the high-impedance state.
5. Set the value corresponding to the bit rate in BRR.
6. Set the CKE0 and CKE1 bits in SCR. Clear the TIE, RIE, TE, RE, MPIE, and TEIE bits to 0.
   If the CKE0 bit is set to 1, the clock is output from the SCK pin.
7. Wait at least one bit interval, then set the TIE, RIE, TE, and RE bits in SCR. Do not set the TE bit and RE bit at the same time, except for self-diagnosis.

To switch from receive mode to transmit mode, after checking that the SCI has finished reception, initialize the SCI, and set RE to 0 and TE to 1. Whether SCI has finished reception or not can be checked with the RDRF, PER, or ORER flags. To switch from transmit mode to receive mode, after checking that the SCI has finished transmission, initialize the SCI, and set TE to 0 and RE to 1. Whether SCI has finished transmission or not can be checked with the TEND flag.

12.10.3 Mark State and Break Detection (Asynchronous Mode Only)

When TE is 0, the TxD pin is used as an I/O port whose direction (input or output) and level are determined by DR and DDR. This can be used to set the TxD pin to mark state (high level) or send a break during serial data transmission. To maintain the communication line at mark state until TE is set to 1, set both DDR and DR to 1. As TE is cleared to 0 at this point, the TxD pin becomes an I/O port, and 1 is output from the TxD pin. To send a break during serial transmission, first set PCR to 1 and PDR to 0, and then clear TE to 0. When TE is cleared to 0, the transmitter is initialized regardless of the current transmission state, the TxD pin becomes an I/O port, and 0 is output from the TxD pin.

12.10.4 Receive Error Flags and Transmit Operations (Clocked Synchronous Mode Only)

Transmission cannot be started when a receive error flag (ORER, PER, or FER) is set to 1, even if the TDRE flag is cleared to 0. Be sure to clear the receive error flags to 0 before starting transmission. Note also that receive error flags cannot be cleared to 0 even if the RE bit is cleared to 0.

12.10.5 Restrictions on Use of DMAC

- When an external clock source is used as the serial clock, the transmit clock should not be input until at least 5 ϕ clock cycles after TDR is updated by the DMAC. Misoperation may occur if the transmit clock is input within 4 ϕ clocks after TDR is updated. (figure 12.38)
- When RDR is read by the DMAC, be sure to set the activation source to the relevant SCI reception end interrupt (RXI).

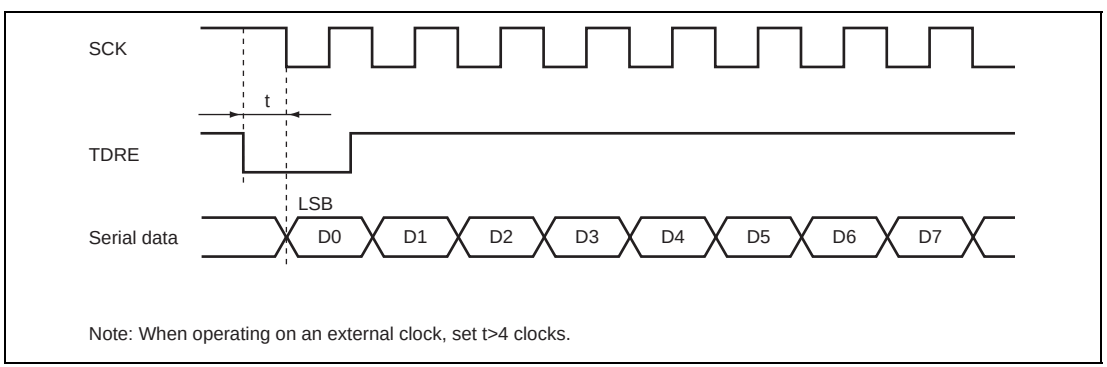


Figure 12.38 Example of Clocked Synchronous Transmission by DMAC

12.10.6 Operation in Case of Mode Transition

- Transmission

  Operation should be stopped (by clearing TE, TIE, and TEIE to 0) before making a module stop mode, software standby mode, watch mode, subactive mode, or subsleep mode transition. TSR, TDR, and SSR are reset. The output pin states in module stop mode, software standby mode, watch mode, subactive mode, or subsleep mode depend on the port settings, and becomes high-level output after the relevant mode is cleared. If a transition is made during transmission, the data being transmitted will be undefined. When transmitting without changing the transmit mode after the relevant mode is cleared, transmission can be started by setting TE to 1 again, and performing the following sequence:

  SSR read -> TDR write -> TDRE clearance. To transmit with a different transmit mode after clearing the relevant mode, the procedure must be started again from initialization. Figure 12.39 shows a sample flowchart for mode transition during transmission. Port pin states are shown in figures 12.40 and 12.41.

14.5.4 Control Transfer

The control transfer consists of three stages; setup, data (sometimes omitted), and status, as shown in figure 14.11. The data stage consists of multiple bus transactions. Figures 14.12 to 14.16 show operation flows in each stage.

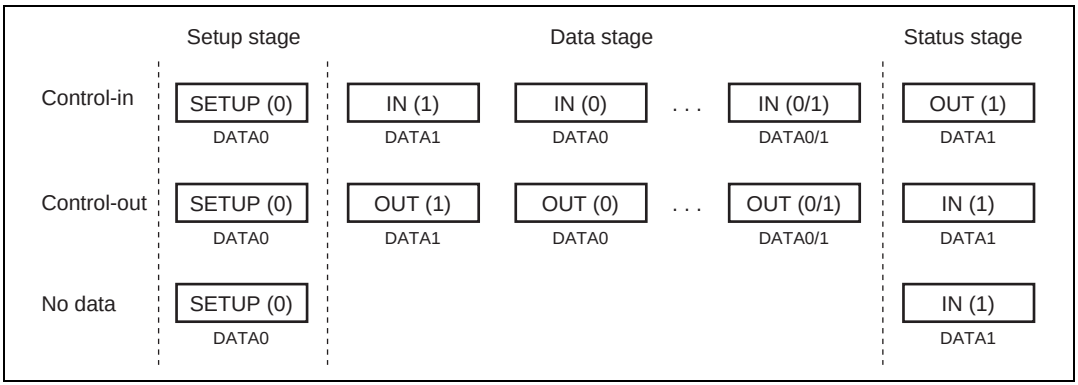


Figure 14.11 Control Transfer Stage Configuration

15.2 Input/Output Pins

Table 15.1 summarizes the input pins used by the A/D converter. The AN0 to AN3 and AN14 to AN15 pins are analog input pins. The VCC and VSS pins are the power supply pins for the analog block in the A/D converter. The Vref pin is the reference voltage pin for the A/D conversion.

Table 15.1 Pin Configuration

Pin Name	Symbol	I/O	Function
Power supply pin	VCC	Input	Analog block power supply and reference voltage (also used for digital block)
Ground pin	VSS	Input	Analog block ground and reference voltage (also used for digital block)
Reference voltage pin	Vref	Input	Reference voltage pin for A/D conversion
Analog input pin 0	AN0	Input	Analog input pins
Analog input pin 1	AN1	Input	
Analog input pin 2	AN2	Input	
Analog input pin 3	AN3	Input	
Analog input pin 14	AN14	Input	
Analog input pin 15	AN15	Input	
A/D external trigger input pin	$\overline{\text{ADTRG}}$	Input	External trigger input pin for starting A/D conversion

15.3 Register Descriptions

The A/D converter has the following registers.

- A/D data register A (ADDRA)
- A/D data register B (ADDRB)
- A/D data register C (ADDRC)
- A/D data register D (ADDRD)
- A/D control/status register (ADCSR)
- A/D control register (ADCR)

Register Name	Power-on Reset	Manual Reset	High-Speed	Medium-Speed	Sleep	Module Stop	Watch	Subactive	Subsleep	Software Standby	Hardware Standby	Module
TCR_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	TPU_1
TMDR_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TIOR_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TIER_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TSR_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TCNT_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TGRA_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TGRB_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TCR_2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	TPU_2
TMDR_2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TIOR_2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TIER_2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TSR_2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TCNT_2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TGRA_2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TGRB_2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
EXMDLSTP	Initialized	—	—	—	—	—	—	—	—	—	Initialized	SYSTEM
RSECDR	—	—	—	—	—	—	—	—	—	—	Initialized	RTC
RMINDR	—	—	—	—	—	—	—	—	—	—	Initialized	
RHRDR	—	—	—	—	—	—	—	—	—	—	Initialized	
RWKDR	—	—	—	—	—	—	—	—	—	—	Initialized	
RTCCR1	—	—	—	—	—	—	—	—	—	—	Initialized	
RTCCR2	—	—	—	—	—	—	—	—	—	—	Initialized	
RTCCSR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	
DMACR0A	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	DMAC
DMACR0B	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
DMACR1A	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
DMACR1B	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
DMABCR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TCSR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	WDT
TCNT	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
RSTCSR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	

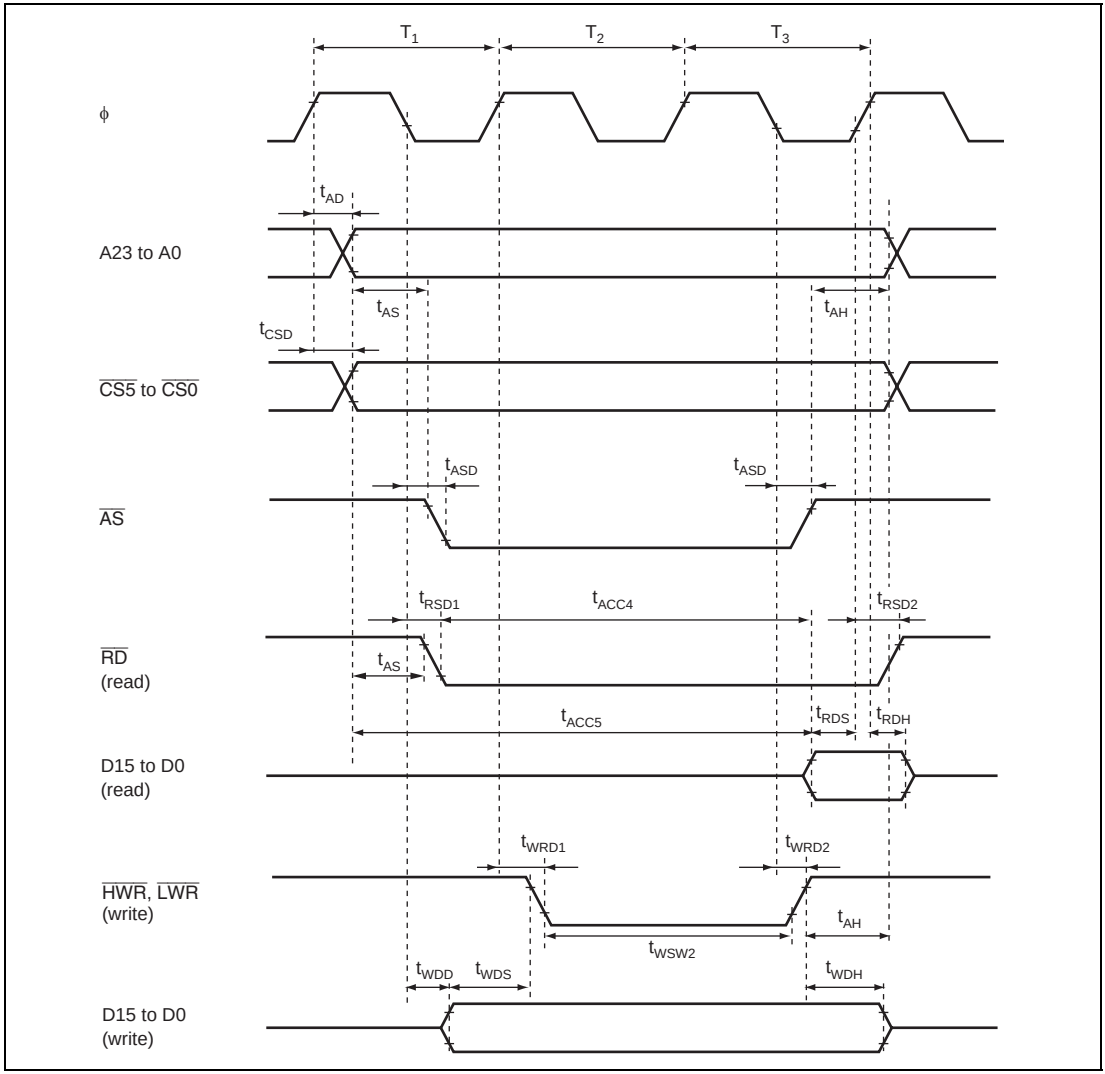


Figure 22.8 Basic Bus Timing (Three-State Access)

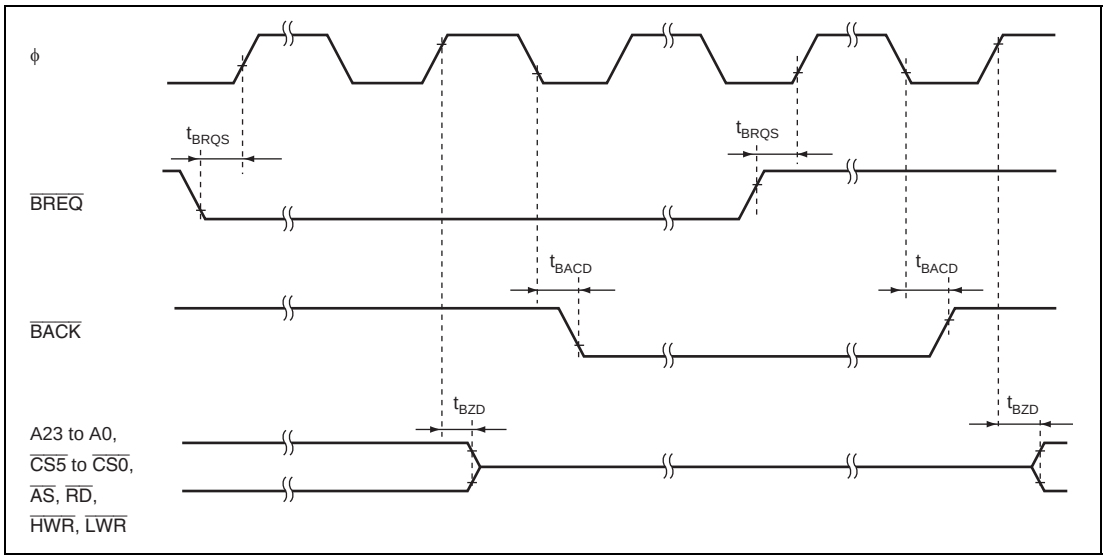


Figure 22.11 External Bus Release Timing