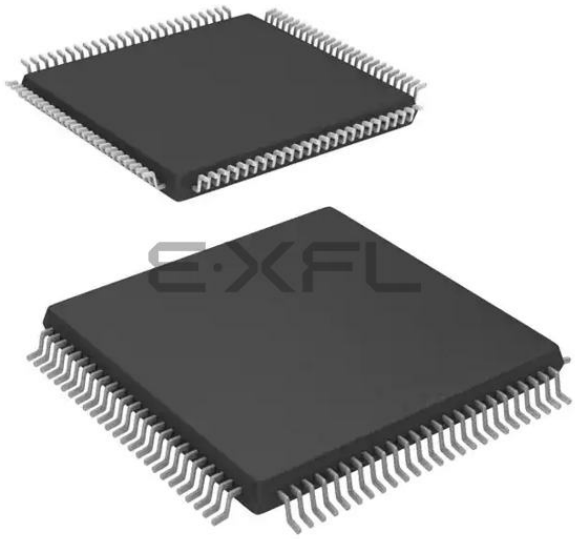

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	24MHz
Connectivity	SCI, SmartCard, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	69
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2217cutf24v

Pin No.		Pin Name*			
TFP-100G, TFP-100GV	**BP-112, BP-112V**	**Modes 4, 5**	**Mode 6**	**Mode 7**	**Programmer Mode**
56	H10	P71/$\overline{CS5}$	P71/$\overline{CS5}$	P71	NC
57	H11	$\overline{STBY}$	$\overline{STBY}$	$\overline{STBY}$	VCC
58	G8	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$
59	G9	VSS	VSS	VSS	VSS
60	G11	XTAL	XTAL	XTAL	XTAL
61	G10	EXTAL	EXTAL	EXTAL	EXTAL
62	F9	VCC	VCC	VCC	VCC
63	F11	P70/$\overline{CS4}$	P70/$\overline{CS4}$	P70	NC
64	F10	PE0/D0	PE0/D0	PE0	D0
65	F8	PE1/D1	PE1/D1	PE1	D1
66	E11	PE2/D2	PE2/D2	PE2	D2
67	E10	PE3/D3	PE3/D3	PE3	D3
68	E9	PE4/D4	PE4/D4	PE4	D4
69	D11	PE5/D5	PE5/D5	PE5	D5
70	E8	PE6/D6	PE6/D6	PE6	D6
71	D10	PE7/D7	PE7/D7	PE7	D7
72	C11	D8	D8	PD0	NC
73	D9	D9	D9	PD1	NC
74	C10	D10	D10	PD2	NC
75	B11	D11	D11	PD3	NC
76	B10	D12	D12	PD4	NC
77	A10	D13	D13	PD5	NC
78	D8	D14	D14	PD6	NC
79	B9	D15	D15	PD7	NC
80	A9	FWE	FWE	FWE	FWE
81	C8	NMI	NMI	NMI	VCC
82	B8	EMLE/NC	EMLE/NC	EMLE/NC	VSS
83	A8	TDO/NC	TDO/NC	TDO/NC	NC
84	D7	TCK/NC	TCK/NC	TCK/NC	VCC
85	C7	TMS/NC	TMS/NC	TMS/NC	VCC

Type	Symbol	Pin No. TFP-100G, TFP-100GV	Pin No. BP-112, BP-112V	Pin No. FP-64E, FP-64EV, TNP-64B, TNP-64BV	I/O	Function
I/O port	P77	—	—	52	I/O	3-bit I/O pins
	P76	—	—	53		
	P75	—	—	54		
	P74	55	H9	—		
	P71	56	H10	—		
	P70	63	F11	—		
	P97	35	J5	23	Input	2-bit input pins
	P96	36	L5	24		
	PA3	98	A3	62	I/O	4-bit I/O pins for the H8S/2218 Group. 3-bit I/O pins for the H8S/2212 Group.
	PA2	99	C4	63		
	PA1	100	B3	64		
	PA0	1	B2	—		
	PB7	52	K11	—	I/O	8-bit I/O pins (Supported only by the H8S/2218 Group)
	PB6	51	K10	—		
	PB5	50	L10	—		
	PB4	49	K9	—		
	PB3	40	K6	—		
	PB2	39	L6	—		
	PB1	38	J6	—		
	PB0	37	K5	—		
	PC7	20	H1	—	I/O	8-bit I/O pins (Supported only by the H8S/2218 Group)
	PC6	19	G3	—		
	PC5	18	G2	—		
	PC4	17	G1	—		
	PC3	13	F3	—		
	PC2	12	E2	—		
	PC1	11	E1	—		
	PC0	10	E3	—		

2.7.8 Memory Indirect—@@aa:8

This mode can be used by the JMP and JSR instructions. The instruction code contains an 8-bit absolute address specifying a memory operand. This memory operand contains a branch address.

The upper bits of the absolute address are all assumed to be 0, so the address range is 0 to 255 (H'0000 to H'00FF in normal mode*, H'000000 to H'0000FF in advanced mode). In normal mode the memory operand is a word operand and the branch address is 16 bits long. In advanced mode the memory operand is a longword operand, the first byte of which is assumed to be H'00.

Note that the first part of the address range is also the exception vector area. For further details, refer to section 4, Exception Handling.

If an odd address is specified in word or longword memory access, or as a branch address, the least significant bit is regarded as 0, causing data to be accessed or instruction code to be fetched at the address preceding the specified address. (For further information, see section 2.5.2, Memory Data Formats.)

Note: * Not available in this LSI.

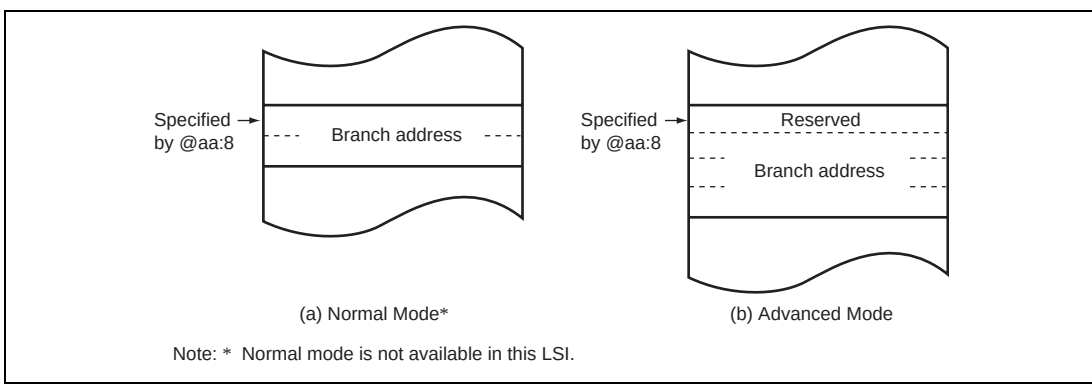

Figure 2.12 Branch Address Specification in Memory Indirect Mode

6.7.2 Wait Control

As with the basic bus interface, either program wait insertion or pin wait insertion using the $\overline{\text{WAIT}}$ pin can be used in the initial cycle (full access) of the burst ROM interface. See section 6.6.4, Wait Control.

Wait states cannot be inserted in a burst cycle.

6.8 Idle Cycle

When the H8S/2218 Group accesses external space, it can insert a 1-state idle cycle (T_I) between bus cycles in the following two cases: (1) when read accesses between different areas occur consecutively, and (2) when a write cycle occurs immediately after a read cycle. By inserting an idle cycle it is possible, for example, to avoid data collisions between ROM, with a long output floating time, and high-speed memory, I/O interfaces, and so on.

Consecutive Reads between Different Areas: If consecutive reads between different areas occur while the ICIS1 bit in BCRH is set to 1, an idle cycle is inserted at the start of the second read cycle.

Figure 6.22 shows an example of the operation in this case. In this example, bus cycle A is a read cycle from ROM with a long output floating time, and bus cycle B is a read cycle from SRAM, each being located in a different area. In (a), an idle cycle is not inserted, and a collision occurs in cycle B between the read data from ROM and that from SRAM. In (b), an idle cycle is inserted, and a data collision is prevented.

7.3.5 DMA Band Control Register (DMABCR)

DMABCR controls the operation of each DMAC channel.

- Short Address Mode

Bit	Bit Name	Initial Value	R/W	Description
15	FAE1	0	R/W	Full Address Enable 1 Specifies whether channel 1 is to be used in short address mode or full address mode. In short address mode, channels 1A and 1B are used as independent channels. 0: Short address mode 1: Full address mode
14	FAE0	0	R/W	Full Address Enable 0 Specifies whether channel 0 is to be used in short address mode or full address mode. In short address mode, channels 0A and 0B are used as independent channels. 0: Short address mode 1: Full address mode
13, 12	—	—	R/W	Reserved The write value should always be 0.

- Full Address Mode

Bit	Bit Name	Initial Value	R/W	Description
15	FAE1	0	R/W	Full Address Enable 1 Specifies whether channel 1 is to be used in short address mode or full address mode. In full address mode, channels 1A and 1B are used together as a single channel. 0: Short address mode 1: Full address mode
14	FAE0	0	R/W	Full Address Enable 0 Specifies whether channel 0 is to be used in short address mode or full address mode. In full address mode, channels 0A and 0B are used together as a single channel. 0: Short address mode 1: Full address mode
13,12	—	All 0	R/W	Reserved Although these bits are readable/writable, only 0 should be written to.

7.4.11 Relation between the DMAC and External Bus Requests

There can be no break between a DMA cycle read and a DMA cycle write. This means that an external bus release cycle is not generated between the external read and external write in a DMA cycle.

In the case of successive read and write cycles, such as in burst transfer or block transfer, an external bus released state may be inserted after a write cycle.

When DMA cycle reads or writes are accesses to on-chip memory or internal I/O registers, these DMA cycles can be executed at the same time as refresh cycles or external bus release. However, simultaneous operation may not be possible when a write buffer is used.

7.4.12 NMI Interrupts and DMAC

When an NMI interrupt is requested, burst mode transfer in full address mode is interrupted. An NMI interrupt does not affect the operation of the DMAC in other modes.

In full address mode, transfer is enabled for a channel when both the DTE bit and the DTME bit are set to 1. With burst mode setting, the DTME bit is cleared when an NMI interrupt is requested.

If the DTME bit is cleared during burst mode transfer, the DMAC discontinues transfer on completion of the 1-byte or 1-word transfer in progress, then releases the bus, which passes to the CPU.

The channel on which transfer was interrupted can be restarted by setting the DTME bit to 1 again. Figure 7.21 shows the procedure for continuing transfer when it has been interrupted by an NMI interrupt on a channel designated for burst mode transfer.

8.1.2 Port 1 Data Register (P1DR)

P1DR stores output data for the port 1 pins.

Bit	Bit Name	Initial Value	R/W	Description
7	P17DR	0	R/W	Store output data for a pin that functions as a general output port.
6	P16DR	0	R/W	
5	P15DR	0	R/W	
4	P14DR	0	R/W	
3	P13DR	0	R/W	
2	P12DR	0	R/W	
1	P11DR	0	R/W	
0	P10DR	0	R/W	

8.1.3 Port 1 Register (PORT1)

PORT1 indicates the pin states of the port 1.

Bit	Bit Name	Initial Value	R/W	Description
7	P17	—*	R	If the port 1 is read while P1DDR bits are set to 1, the P1DR value is read. If the port 1 is read while P1DDR bits are cleared to 0, the pin states are read.
6	P16	—*	R	
5	P15	—*	R	
4	P14	—*	R	
3	P13	—*	R	
2	P12	—*	R	
1	P11	—*	R	
0	P10	—*	R	

Note: * Determined by the states of pins P17 to P10.

8.2.4 Port 3 Open-Drain Control Register (P3ODR)

P3ODR controls the PMOS on/off state for each port 3 pin.

Bit	Bit Name	Initial Value	R/W	Description
7	—	Undefined	—	Reserved This bit is undefined and cannot be modified.
6	P36ODR	0	R/W	Setting a P3ODR bit to 1 makes the corresponding port 3 pin an NMOS open-drain output pin, while clearing the bit to 0 makes the pin a CMOS output pin.
5 to 3	—	Undefined	—	Reserved These bits are undefined and cannot be modified.
2	P32ODR	0	R/W	Setting a P3ODR bit to 1 makes the corresponding port 3 pin an NMOS open-drain output pin, while clearing the bit to 0 makes the pin a CMOS output pin.
1	P31ODR	0	R/W	
0	P30ODR	0	R/W	

8.2.5 Pin Functions

Port 3 pins also function as SCI I/O pins and external interrupt input ($\overline{\text{IRQ4}}$) pins. The correspondence between the register specification and the pin functions is shown below. The P36 pin must be used as the D+ pull-up control output pin of the USB. For details, refer to section 14, Universal Serial Bus (USB).

Table 8.19 P36 Pin Function

P36DDR	0	1
Pin Function	P36 input pin	P36 output pin (D+ pull-up control output pin of USB)

8.9.4 Port D Pull-Up MOS Control Register (PDPCR)

PDPCR controls the on/off state of the port D input pull-up MOS.

Bit	Bit Name	Initial Value	R/W	Description
7	PD7PCR	0	R/W	When a pin functions as an input port, setting the corresponding bit to 1 turns on the input pull-up MOS for that pin.
6	PD6PCR	0	R/W	
5	PD5PCR	0	R/W	
4	PD4PCR	0	R/W	
3	PD3PCR	0	R/W	
2	PD2PCR	0	R/W	
1	PD1PCR	0	R/W	
0	PD0PCR	0	R/W	

8.9.5 Pin Functions

Port D pins also function as data bus (D15 to D8) I/O pins. The correspondence between the register specification and the pin functions is shown below.

Table 8.55 PD7 Pin Function

Operating Mode	Modes 4 to 6	Mode 7	
PD7DDR	—	0	1
Pin Function	D15 input/output pin	PD7 input pin	PD7 output pin

Table 8.56 PD6 Pin Function

Operating Mode	Modes 4 to 6	Mode 7	
PD6DDR	—	0	1
Pin Function	D14 input/output pin	PD6 input pin	PD6 output pin

Table 8.57 PD5 Pin Function

Operating Mode	Modes 4 to 6	Mode 7	
PD5DDR	—	0	1
Pin Function	D13 input/output pin	PD5 input pin	PD5 output pin

Table 9.16 TIOR_2 (channel 2)

				Description	
Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**TGRA_2**	
IOA3	**IOA2**	**IOA1**	**IOA0**	**Function**	**TIOCA2 Pin Function**
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 output 0 output at compare match
		1	0		Initial output is 0 output 1 output at compare match
			1		Initial output is 0 output Toggle output at compare match
	1	0	0		Output disabled
			1		Initial output is 1 output 0 output at compare match
		1	0		Initial output is 1 output 1 output at compare match
			1		Initial output is 1 output Toggle output at compare match
1	×	0	0	Input capture register	Capture input source is TIOCA2 pin Input capture at rising edge
			1		Capture input source is TIOCA2 pin Input capture at falling edge
		1	×		Capture input source is TIOCA2 pin Input capture at both edges

Legend:

×: Don’t care

Contention between TGR Write and Compare Match: If a compare match occurs in the T_2 state of a TGR write cycle, the TGR write takes precedence and the compare match signal is inhibited. A compare match does not occur even if the same value as before is written. Figure 9.47 shows the timing in this case.

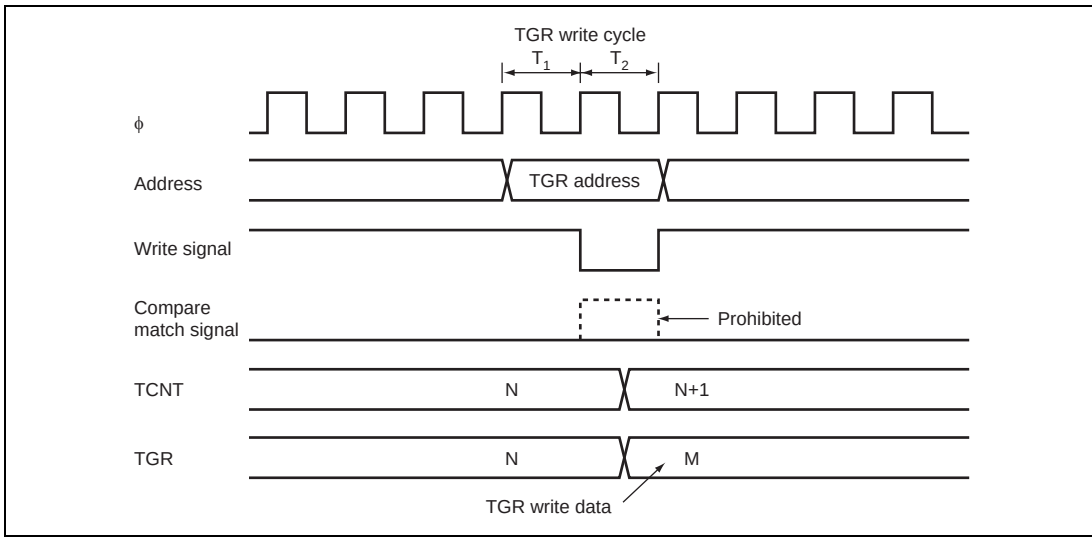

Figure 9.47 Contention between TGR Write and Compare Match

10.3.2 Timing of Setting of Watchdog Timer Overflow Flag (WOVF)

With WDT, the WOVF bit in RSTCSR is set to 1 if TCNT overflows in watchdog timer mode. If TCNT overflows while the RSTE bit in RSTCSR is set to 1, an internal reset signal is generated for the entire chip. This timing is illustrated in figure 10.3.

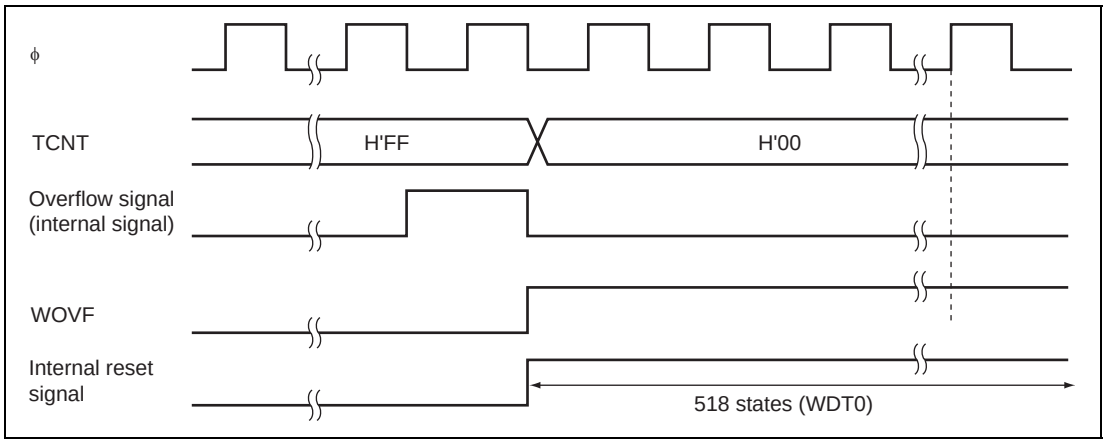

Figure 10.3 Timing of WOVF Setting

10.3.3 Interval Timer Mode

To use the WDT as an interval timer, clear bit WT/$\overline{IT}$ in TCSR to 0 and set bit TME to 1. When the interval timer is operating, an interval timer interrupt (WOVI) is generated each time the TCNT overflows. Therefore, an interrupt can be generated at intervals.

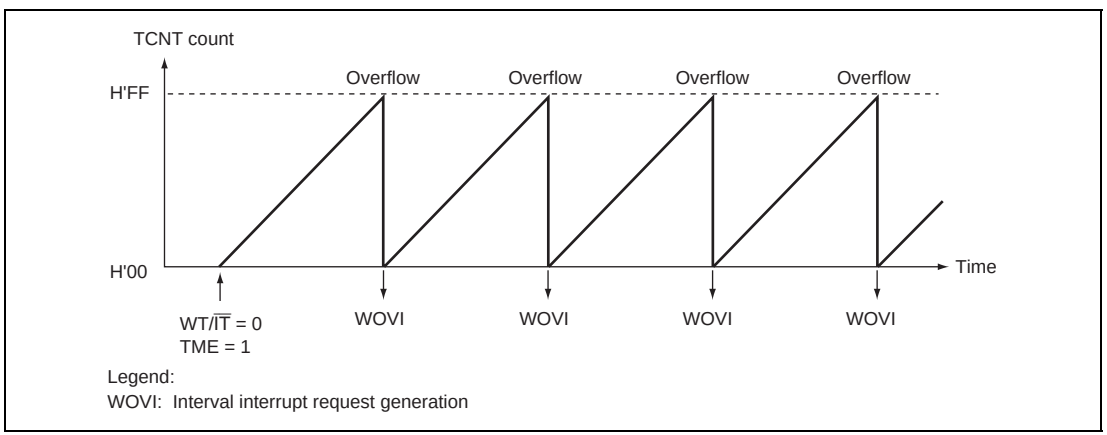

Figure 10.4 Operation in Interval Timer Mode

12.1.1 Block Diagram

Figure 12.1 shows the block diagram of the SCI_0. Figure 12.2 shows the block diagram of the SCI_2.

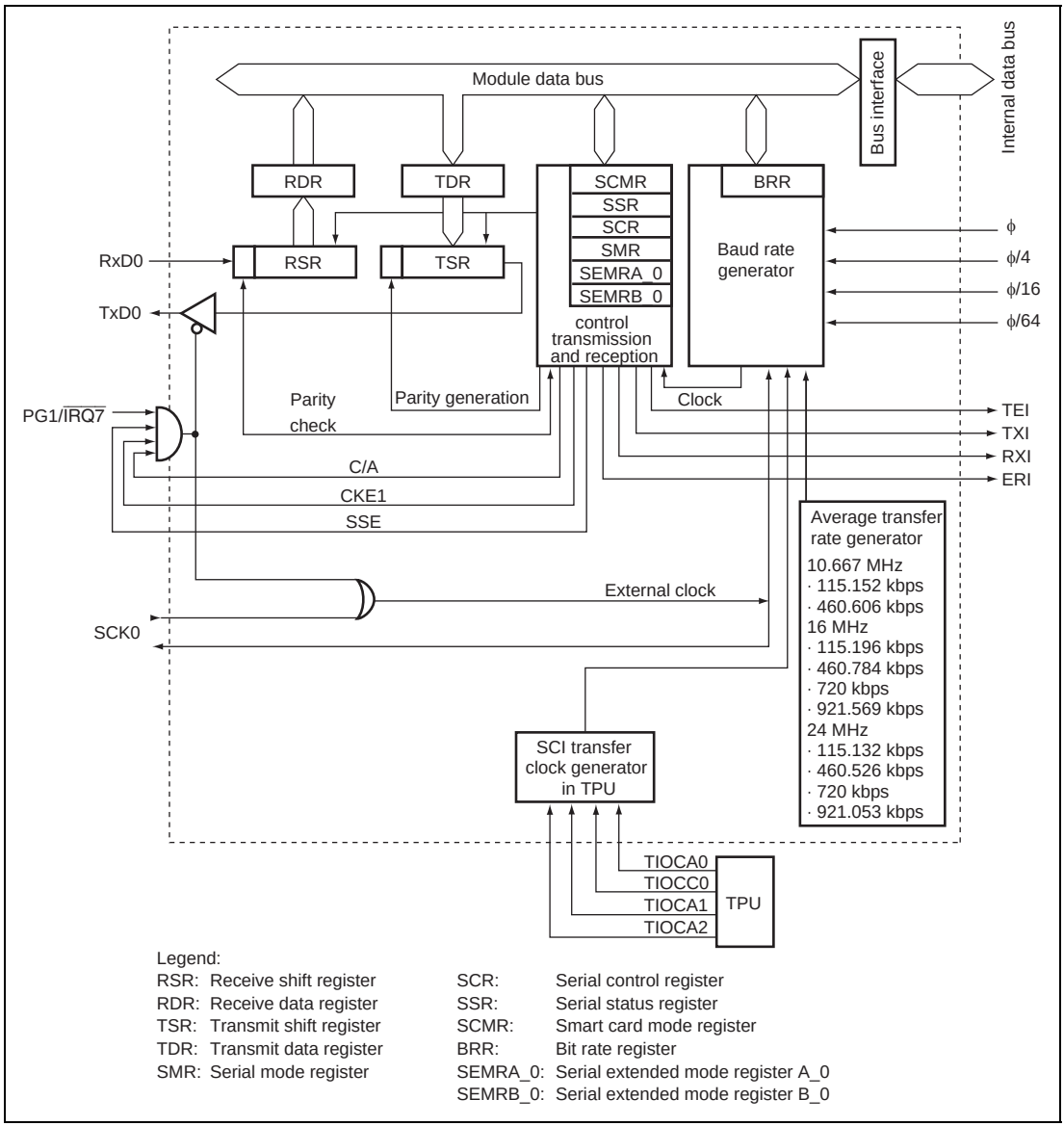

Figure 12.1 Block Diagram of SCI_0

- Smart Card Interface Mode (When SMIF in SCMR is 1)

Bit	Bit Name	Initial Value	R/W	Description
7	GM	0	R/W	GSM Mode Setting this bit to 1 allows GSM mode operation. In GSM mode, the TEND set timing is put forward to 11.0 etu from the start and the clock output control function is appended. For details, see section 12.7.9, Clock Output Control. 0: Normal smart card interface mode operation (initial value) (1) The TEND flag is generated 12.5 etu (11.5 etu in the block transfer mode) after the beginning of the start bit. (2) Clock output on/off control only. 1: GSM mode operation in smart card interface mode (1) The TEND flag is generated 11.0 etu after the beginning of the start bit. (2) In addition to clock output on/off control, high/how fixed control is supported (set using SCR).
6	BLK	0	R/W	Setting this bit to 1 allows block transfer mode operation. For details, see section 12.7.4, Block Transfer Mode. 0: Normal smart card interface mode operation (initial value) (1) Error signal transmission, detection, and automatic data retransmission are performed. (2) The TXI interrupt is generated by the TEND flag. (3) The TEND flag is set 12.5 etu (11.0 etu in the GSM mode) after transmission starts. 1: Operation in block transfer mode (1) Error signal transmission, detection, and automatic data retransmission are not performed. (2) The TXI interrupt is generated by the TDRE flag. (3) The TEND flag is set 11.5 etu (11.0 etu in the GSM mode) after transmission starts.

12.8 SCI Select Function (Clocked Synchronous Mode)

The SCI_0 supports the SCI select function which allows clock synchronous communication between master LSI and one of multiple slave LSI. Figure 12.36 shows an example of communication using the SCI select function. Figure 12.37 shows the operation.

The master LSI can communicate with slave LSI_A by bringing $\overline{\text{SEL\_A}}$ and $\overline{\text{SEL\_B}}$ signals low and high, respectively. In this case, the TxD0_B pin of the slave LSI_B is brought high-impedance state and the internal SCK0_A signal is fixed high. This halts the communication operation of slave LSI_B. The master LSI can communicate with slave LSI_B by bringing the $\overline{\text{SEL\_A}}$ and $\overline{\text{SEL\_B}}$ signals high and low, respectively.

The slave LSI detects the selection by receiving the low level input from the $\overline{\text{IRQ7}}$ pin and immediately executes data transmission/reception processing.

Note: The selection signals ($\overline{\text{SEL\_A}}$ and $\overline{\text{SEL\_B}}$) of the LSI must be switched while the serial clock (M_SCK) is high after the end bit of the transmit data has been send. Note that one selection signal can be brought low at the same time.

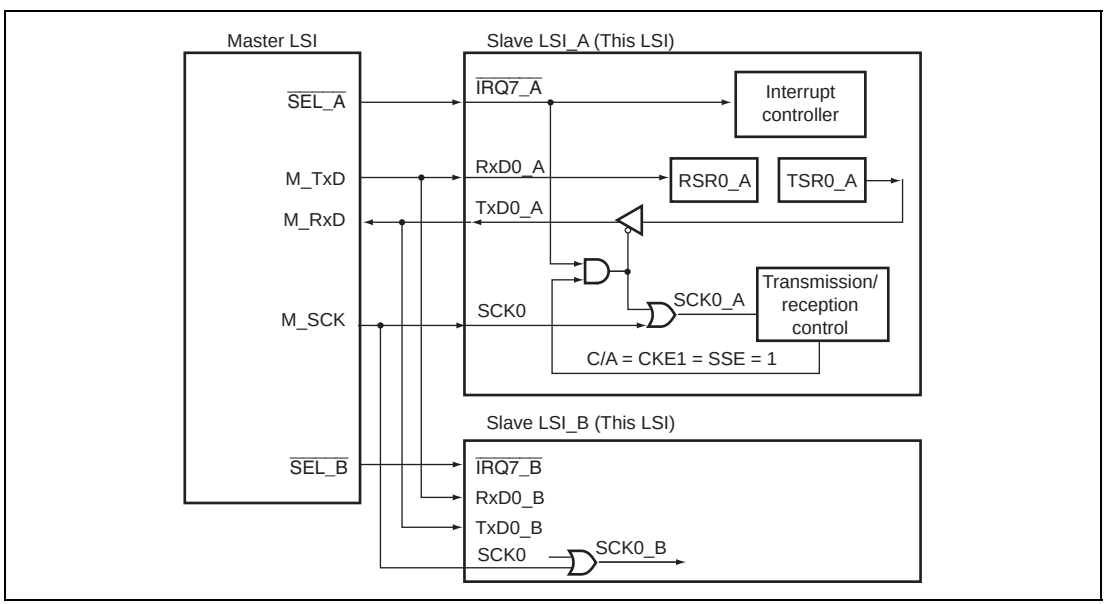

Figure 12.36 Example of Communication Using the SCI Select Function

15.2 Input/Output Pins

Table 15.1 summarizes the input pins used by the A/D converter. The AN0 to AN3 and AN14 to AN15 pins are analog input pins. The VCC and VSS pins are the power supply pins for the analog block in the A/D converter. The Vref pin is the reference voltage pin for the A/D conversion.

Table 15.1 Pin Configuration

Pin Name	Symbol	I/O	Function
Power supply pin	VCC	Input	Analog block power supply and reference voltage (also used for digital block)
Ground pin	VSS	Input	Analog block ground and reference voltage (also used for digital block)
Reference voltage pin	Vref	Input	Reference voltage pin for A/D conversion
Analog input pin 0	AN0	Input	Analog input pins
Analog input pin 1	AN1	Input	
Analog input pin 2	AN2	Input	
Analog input pin 3	AN3	Input	
Analog input pin 14	AN14	Input	
Analog input pin 15	AN15	Input	
A/D external trigger input pin	$\overline{\text{ADTRG}}$	Input	External trigger input pin for starting A/D conversion

15.3 Register Descriptions

The A/D converter has the following registers.

- A/D data register A (ADDRA)
- A/D data register B (ADDRB)
- A/D data register C (ADDRC)
- A/D data register D (ADDRD)
- A/D control/status register (ADCSR)
- A/D control register (ADCR)

19.2.2 Inputting External Clock

An external clock signal can be input as shown in an example in figure 19.4. If the XTAL pin is left open, make sure that stray capacitance is no more than 10 pF. When complementary clock input to XTAL pin, the external clock input should be fixed high in standby mode, subactive mode, subsleep mode, or watch mode.

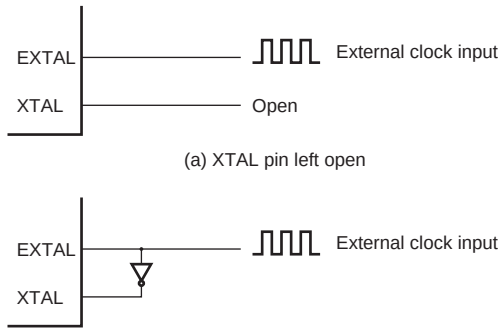

Figure 19.4 External Clock Input (Examples)

Table 19.3 shows the input conditions for the external clock.

Table 19.3 External Clock Input Conditions

		VCC= 2.4 to 3.6V		VCC = 2.7 to 3.6V		VCC = 3.0 to 3.6V			Test
Item	Symbol	min	max	Min	max	min	max	Unit	Conditions
External clock input low pulse width	t_{EXL}	65	—	25	—	15.5	—	ns	Figure 19.5
External clock input high pulse width	t_{EXH}	65	—	25	—	15.5	—	ns	
External clock rise time	t_{EXr}	—	15	—	6.25	—	5.25	ns	
External clock fall time	t_{EXf}	—	15	—	6.25	—	5.25	ns	
Clock low pulse width level	t_{CL}	0.35	0.65	0.4	0.6	0.4	0.6	tcyc	Figure 22.3
Clock high pulse width level	t_{CH}	0.35	0.65	0.4	0.6	0.4	0.6	tcyc	

The external clock input conditions when the duty adjustment circuit is not used are shown in table 19.4. When the duty adjustment circuit is not used, note that the maximum operating frequency depends on the external clock input waveform. For example, if $t_{EXL} = t_{EXH} = 20.8$ ns and $t_{EXr} = t_{EXf} = 5.25$ ns, the maximum operating frequency becomes 19.2 MHz depending on the clcok cycle time of 52.1 ns.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
TGRC_0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	TPU_0
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRD_0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TCR_1	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU_1
TMDR_1	—	—	—	—	MD3	MD2	MD1	MD0	
TIOR_1	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0	
TIER_1	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA	
TSR_1	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA	
TCNT_1	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRA_1	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRB_1	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TCR_2	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU_2
TMDR_2	—	—	—	—	MD3	MD2	MD1	MD0	
TIOR_2	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0	
TIER_2	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA	
TSR_2	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA	
TCNT_2	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRA_2	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRB_2	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
EXMDLSTP	—	—	—	—	—	—	RTCSTOP	USBSTOP1	SYSTEM