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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	24MHz
Connectivity	SCI, SmartCard, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	69
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2218br24v

Preface

This LSI is a microcomputer (MCU) made up of the H8S/2000 CPU with Renesas Technology's original architecture as its core, and the peripheral functions required to configure a system.

The H8S/2000 CPU has an internal 32-bit configuration, sixteen 16-bit general registers, and a simple and optimized instruction set for high-speed operation. The H8S/2000 CPU can handle a 16-Mbyte linear address space.

This LSI is equipped with ROM and RAM, a direct memory access controller (DMAC), a bus master, a 16-bit timer pulse unit (TPU), a watchdog timer (WDT), a realtime clock (RTC), a universal serial bus (USB), two types of serial communication interfaces (SCIs), an A/D converter, and I/O ports as on-chip peripheral modules for system configuration.

A single-power flash memory (F-ZTAT™*) version and masked ROM version are available for this LSI's ROM. The F-ZTAT version provides flexibility as it can be reprogrammed in no time to cope with all situations from the early stages of mass production to full-scale mass production. This is particularly applicable to application devices with specifications that will most probably change.

This manual describes this LSI's hardware.

Note: * F-ZTAT is a trademark of Renesas Technology, Corp.

Target Users: This manual was written for users who will be using the H8S/2218 Group and H8S/2212 Group in the design of application systems. Target users are expected to understand the fundamentals of electrical circuits, logical circuits, and microcomputers.

Objective: This manual was written to explain the hardware functions and electrical characteristics of the H8S/2218 Group and H8S/2212 Group to the target users. Refer to the H8S/2600 Series, H8S/2000 Series Software Manual for a detailed description of the instruction set.

Notes on reading this manual:

- In order to understand the overall functions of the chip
  Read the manual according to the contents. This manual can be roughly categorized into parts on the CPU, system control functions, peripheral functions and electrical characteristics.
- In order to understand the details of the CPU's functions
  Read the H8S/2600 Series, H8S/2000 Series Software Manual.

2.1.2 Differences from H8/300 CPU

In comparison to the H8/300 CPU, the H8S/2000 CPU has the following enhancements.

- More general registers and control registers
  - Eight 16-bit extended registers, and one 8-bit and two 32-bit control registers, have been added.
- Extended address space
  - Normal mode supports the same 64-kbyte address space as the H8/300 CPU.
  - Advanced mode supports a maximum 16-Mbyte address space.
- Enhanced addressing
  - The addressing modes have been enhanced to make effective use of the 16-Mbyte address space.
- Enhanced instructions
  - Addressing modes of bit-manipulation instructions have been enhanced.
  - Signed multiply and divide instructions have been added.
  - Two-bit shift instructions have been added.
  - Instructions for saving and restoring multiple registers have been added.
  - A test and set instruction has been added.
- Higher speed
  - Basic instructions execute twice as fast.

2.1.3 Differences from H8/300H CPU

In comparison to the H8/300H CPU, the H8S/2000 CPU has the following enhancements.

- Additional control register
  - One 8-bit control registers have been added.
- Enhanced instructions
  - Addressing modes of bit-manipulation instructions have been enhanced.
  - Two-bit shift instructions have been added.
  - Instructions for saving and restoring multiple registers have been added.
  - A test and set instruction has been added.
- Higher speed
  - Basic instructions execute twice as fast.

Instruction	Size*[1]	Function
NEG	B/W/L	0 – Rd → Rd Takes the two's complement (arithmetic complement) of data in a

Table 6.2 Bus Specifications for Each Area (Basic Bus Interface)

ABWCR	ASTCR	WCRH, WCRL		Bus Specifications (Basic Bus Interface)		
ABWn	ASTn	Wn1	Wn0	Bus Width	Number of Access States	Number of Program Wait States
0	0	—	—	16	2	0
	1	0	0		3	0
			1			1
		1	0			2
			1			3
1	0	—	—	8	2	0
	1	0	0		3	0
			1			1
		1	0			2
			1			3

6.4.3 Bus Interface for Each Area

The initial state of each area is basic bus interface, 3-state access space. The initial bus width is selected according to the operating mode. The bus specifications described here cover basic items only, and the sections on each memory interface (section 6.6, Basic Bus Interface and section 6.7, Burst ROM Interface) should be referred to for further details. Note that the ROM is always enabled and no external extended mode in the H8S/2212 Group.

Area 0: Area 0 includes on-chip ROM, and in ROM-disabled extended mode, all of area 0 is external space. In ROM-enabled extended mode, the space excluding on-chip ROM is external space.

When area 0 external space is accessed, the $\overline{CS0}$ signal can be output.

Either basic bus interface or burst ROM interface can be selected for area 0.

Areas 1 to 6: In external extended mode, all of areas 1 to 6 is external space. When area 1 to 5 external space is accessed, the $\overline{CS1}$ to $\overline{CS5}$ pin signals respectively can be output. Only the basic bus interface can be used for areas 1 to 5. Area 6 is only for the on-chip USB. For details, see section 14, Universal Serial Bus (USB).

Area 7: Area 7 includes the on-chip RAM and internal l/O registers. In external extended mode, the space excluding the reserved area (for details, see section 3.4, Memory Map in Each Operating Mode) the on-chip RAM and internal l/O registers except on-chip RTC, is external space. The on-chip RAM is enabled when the RAME bit in the system control register (SYSCR) is set to 1; when

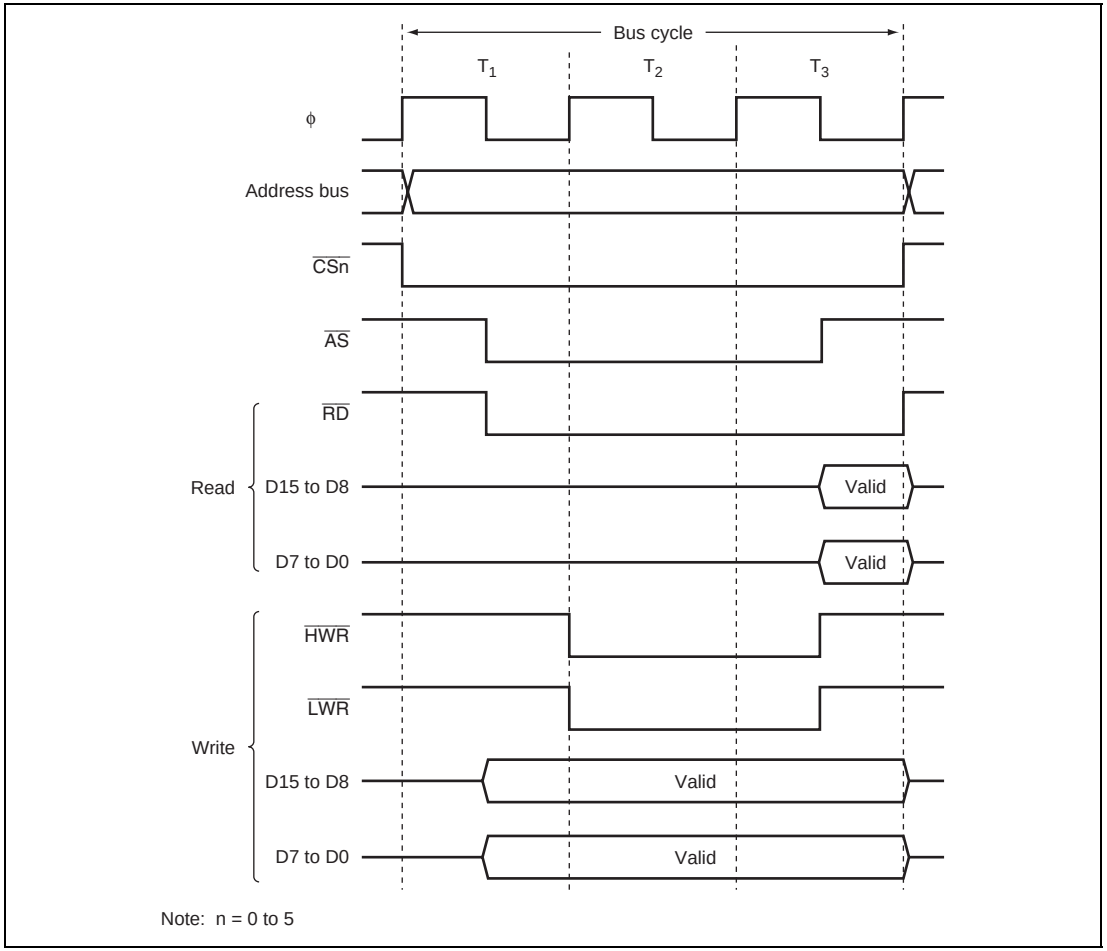


Figure 6.18 Bus Timing for 16-Bit 3-State Access Space (3) (Word Access)

Figure 6.19 shows an example of wait state insertion timing.

In the H8S/2212 Group, the WAITE bit in BCRH should not be set to 1.

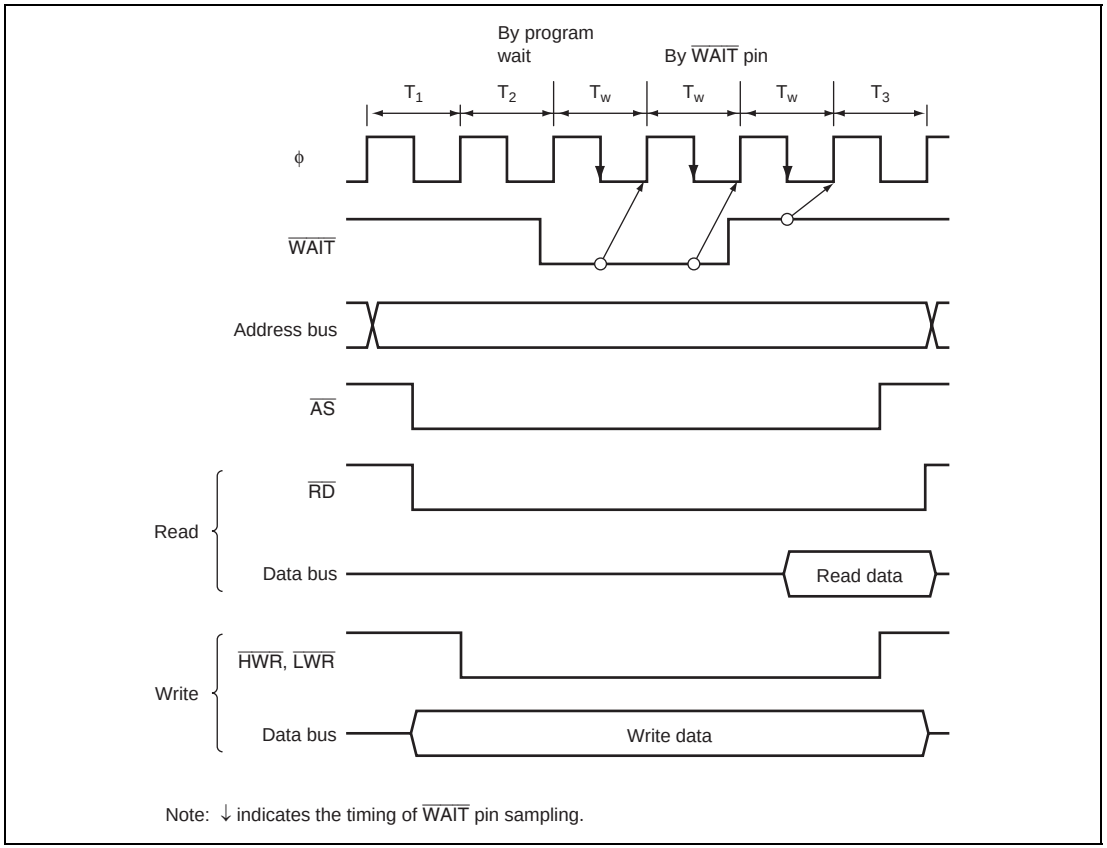


Figure 6.19 Example of Wait State Insertion Timing

Figure 7.11 illustrates operation in block transfer mode when MARA is designated as a block area.

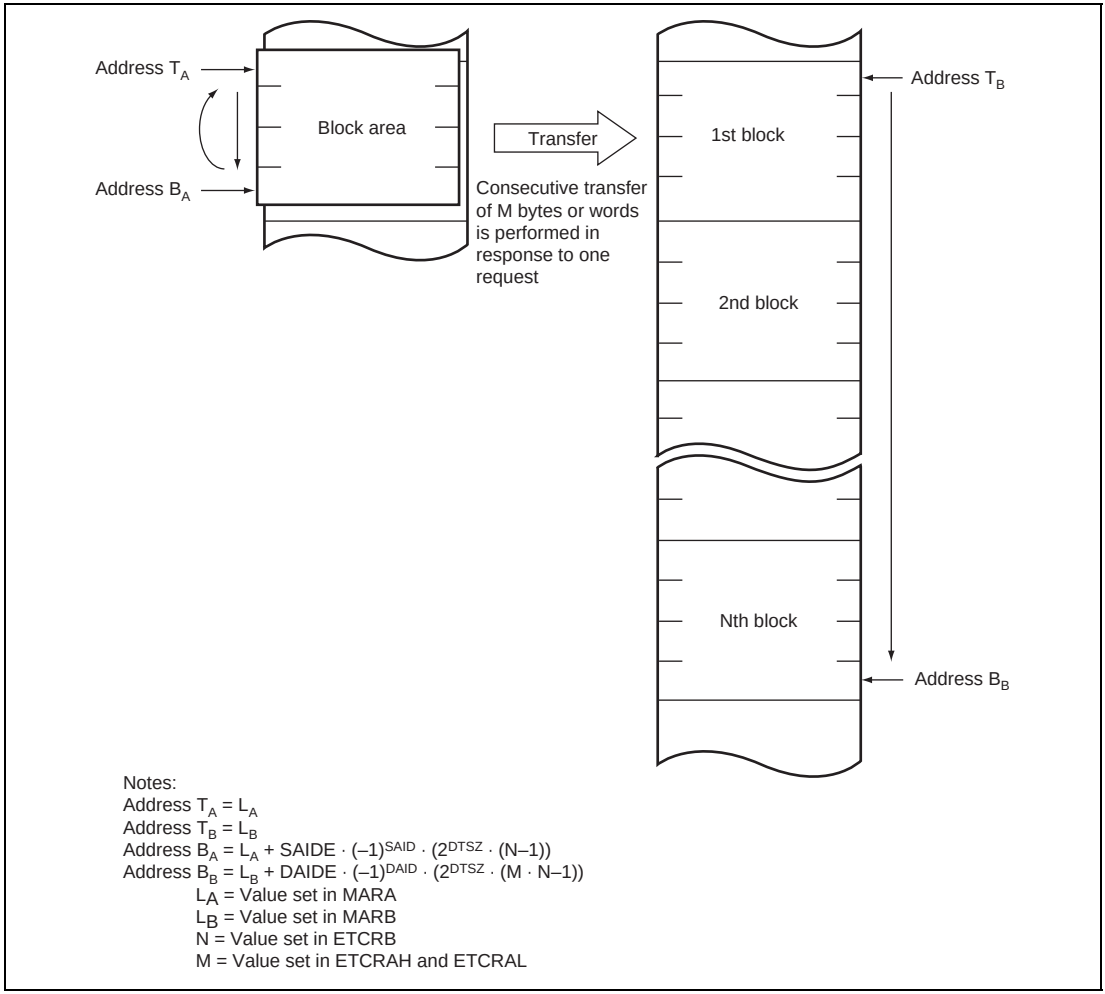


Figure 7.11 Operation in Block Transfer Mode (BLKDIR = 1)

ETCRAL is decremented by 1 each time a byte or word transfer is performed. In response to a single transfer request, burst transfer is performed until the value in ETCRAL reaches H'00. ETCRAL is then loaded with the value in ETCRAH. At this time, the value in the MAR register for which a block designation has been given by the BLKDIR bit in DMACRA is restored in accordance with the DTSZ, SAID/DAID, and SAIDE/DAIDE bits in DMACR.

ETCRB is decremented by 1 every block transfer, and when the count reaches H'0000 the DTE bit is cleared and transfer ends. If the DTIE bit is set to 1 at this point, an interrupt request is sent to the CPU. Figure 7.12 shows the operation flow in block transfer mode.

Activation by USB Request: The USB request ($\overline{\text{DREQ}}$ signal) is specified as a DMAC activation source. The USB request is generated by the level sense. In full-address normal mode, the USB request is carried out as follows.

While the $\overline{\text{DREQ}}$ signal is kept high, the DMAC waits for the transfer request. While the $\overline{\text{DREQ}}$ signal is kept low, the DMAC releases the bus each time a byte is transferred and the transfer is performed continuously. When the $\overline{\text{DREQ}}$ signal is driven high during the transfer, the transfer is halted and the DMAC waits for the transfer request.

Activation by Auto-Request: Auto-request activation is performed by register setting only, and transfer continues to the end. With auto-request activation, cycle steal mode or burst mode can be selected.

In cycle steal mode, the DMAC releases the bus to another bus master each time a byte or word is transferred. DMA and CPU cycles usually alternate. In burst mode, the DMAC keeps possession of the bus until the end of the transfer, and transfer is performed continuously.

7.4.10 DMAC Multi-Channel Operation

The DMAC channel priority order is: channel 0 > channel 1, and channel A > channel B. Table 7.9 summarizes the priority order for DMAC channels.

Table 7.9 DMAC Channel Priority Order

Short Address Mode	Full Address Mode	Priority
Channel 0A	Channel 0	High
Channel 0B		
Channel 1A	Channel 1	
Channel 1B		Low

If transfer requests are issued simultaneously for more than one channel, or if a transfer request for another channel is issued during a transfer, when the bus is released the DMAC selects the highest-priority channel from among those issuing a request according to the priority order shown in table 7.9. During burst transfer, or when one block is being transferred in block transfer, the channel will not be changed until the end of the transfer. Figure 7.20 shows a transfer example in which transfer requests are issued simultaneously for channels 0A, 0B, and 1.

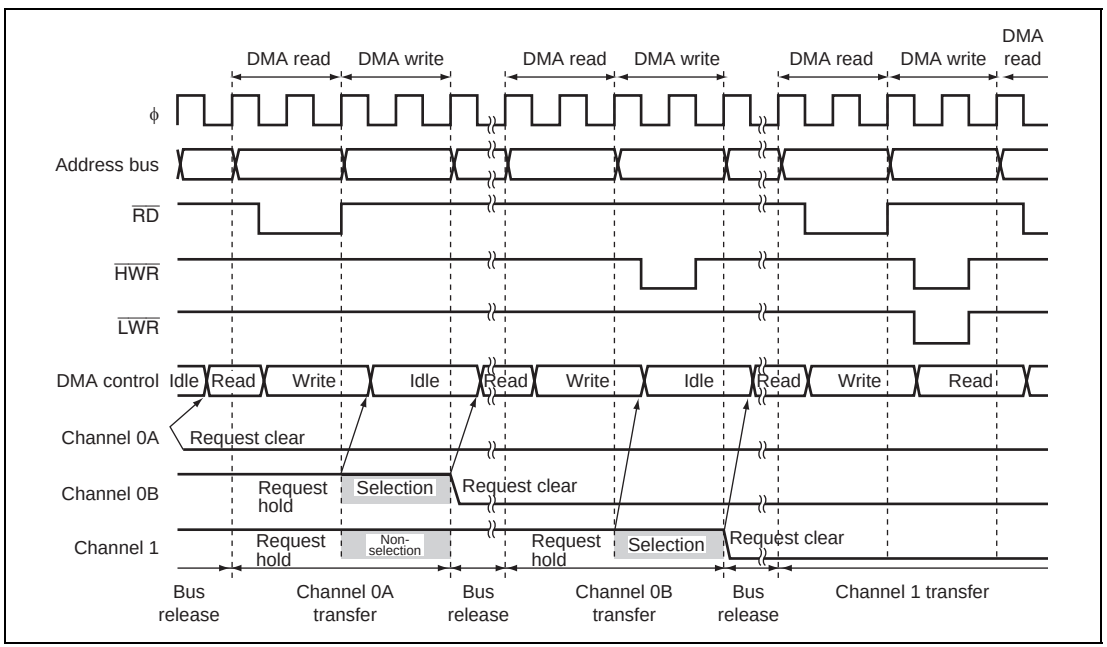


Figure 7.20 Example of Multi-Channel Transfer

Table 8.87 PF1 Pin Function

Operating Mode	Modes 4 to 6			Mode 7	
BRLE	0		1	—	
PF1DDR	0	1	—	0	1
Pin Function	PF1 input pin	PF1 output pin	$\overline{\text{BACK}}$ output pin	PF1 input pin	PF1 output pin

Table 8.88 PF0 Pin Function

Operating Mode	Modes 4 to 6			Mode 7	
BRLE	0		1	—	
PF0DDR	0	1	—	0	1
Pin Function	PF0 input pin	PF0 output pin	$\overline{\text{BREQ}}$ input pin	PF0 input pin	PF0 output pin
	$\overline{\text{IRQ2}}$ input pin*				

Note: * When this pin is used as an external interrupt input pin, this pin must not be used as an I/O pin for another function.

Pin Functions of H8S/2212 Group

The port F is a 3-bit I/O port. Port F pins also function as external interrupt input ($\overline{\text{IRQ2}}$, $\overline{\text{IRQ3}}$) pins and system clock output (ϕ) pins. The correspondence between the register specification and the pin functions is shown below.

Table 8.89 PF7 Pin Function

PF7DDR	0	1			
PF7OUT2 to PF7OUT0	—	B'000	B'001	B'010	B'011
Pin Function	PF7 input pin	ϕ output pin	ϕ/2 output pin	ϕ/3 output pin	ϕ/4 output pin

11.3.8 Extended Module Stop Register (EXMDLSTP)

EXMDLSTP controls the clock supply of the RTC and USB.

Note: When reading pin states using the port D register (PORTD), after accessing EXMDLSTP (address range: H'FFFF40 to H'FFFF5F), you must perform a dummy read to the external address space (such as H'FFEF00 to H'FF7FF) outside the range H'FFFF40 to H'FFFF5F before reading PORTD.

Bit	Bit Name	Initial Value	R/W	Module
7 to 2	—	Undefined	—	Reserved These bits are always read as undefined values. These bits should not to be modified.
1	RTCSTOP	0	R/W	RTC Module Stop 0: RTC module stop cancelled 1: RTC module stop
0	USBSTOP1	0	R/W	USB Module Stop 0: USB module stop partly cancelled 1: USB module completely stop

Bit	Bit Name	Initial Value	R/W	Description
5	UCKS3	0	R/W	USB Operation Clock Select 3 to 0
4	UCKS2			These bits control the on-chip PLL, which generates the USB operation clock (48 MHz). When UCKS3 to UCKS0 are 0000, the PLL circuit stops and thus the USB operation clock must be selected according to the clock source.
3	UCKS1			
2	UCKS0			
				The on-chip PLL circuit starts operating after the USB module stop 2 bit has been cancelled. In addition, the USB operation clock is supplied to the UDC core after the USB operating clock stabilization time has been passed. The completion timing of the USB operating clock stabilization time can be detected by the CK48READY flag in UIFR3.
				UCKS0 to UCKS3 muse be written while the USB module stop 2 bit (MSTPB0) is 1.
				0000: USB operation clock stops (PLL stops)
				0001: Reserved
				001×: Reserved
				010×: Reserved
				0110: Uses a clock (48 MHz) generated by doubling the 24-MHz main oscillation by the PLL.
				0111: Uses a clock (48 MHz) generated by tripling the 16-MHz main oscillation by the PLL.
				1×××: Reserved
				The USB operating clock stabilization time is 2 ms.
				Legend:
				×: Don't care

14.3.2 USB DMAC Transfer Request Register (UDMAR)

UDMAR is set when data transfer by means of a USB request of the on-chip DMAC is performed for data registers UEDR1 and UEDR2 corresponding to EP1 and EP2 respectively used for Bulk transfer. For the DMAC transfer, set $\overline{\text{DREQ0}}$ and $\overline{\text{DREQ1}}$ separately. If $\overline{\text{DREQ0}}$ and $\overline{\text{DREQ1}}$ usage overlaps, the USB cannot operate correctly. For details on DMAC transfer, refer to section 14.6, DMA Transfer Specifications.

Note: As the $\overline{\text{DREQ}}$ signal is not used in the data transfer by auto request of the on-chip DMAC, set UDMAR to H'00.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
3	EP2T1	0	R/W	EP2 DMAC Transfer Request Select 1, 0
2	EP2T0			00: Does not request EP2 DMAC transfer
				01: Reserved
				10: Requests EP2 DMAC transfer by $\overline{\text{DREQ0}}$
				11: Requests EP2 DMAC transfer by $\overline{\text{DREQ1}}$
1	EP1T1	0	R/W	EP1 DMAC Transfer Request Select 1, 0
0	EP1T0			00: Does not request EP1 DMAC transfer
				01: Reserved
				10: Requests EP1 DMAC transfer by $\overline{\text{DREQ0}}$
				11: Requests EP1 DMAC transfer by $\overline{\text{DREQ1}}$

15.5 Operation

The A/D converter operates by successive approximation with 10-bit resolution. It has two operating modes; single mode and scan mode. When changing the operating mode or analog input channel, in order to prevent incorrect operation, first clear the bit ADST to 0 in ADCSR. The ADST bit can be set at the same time as the operating mode or analog input channel is changed.

15.5.1 Single Mode

In single mode, A/D conversion is to be performed only once on the specified single channel. The operations are as follows.

1. A/D conversion is started when the ADST bit is set to 1, according to software or external trigger input.
2. When A/D conversion is completed, the result is transferred to the corresponding A/D data register to the channel.
3. On completion of conversion, the ADF bit in ADCSR is set to 1. If the ADIE bit is set to 1 at this time, an ADI interrupt request is generated.
4. The ADST bit remains set to 1 during A/D conversion. When A/D conversion ends, the ADST bit is automatically cleared to 0 and the A/D converter enters the wait state.

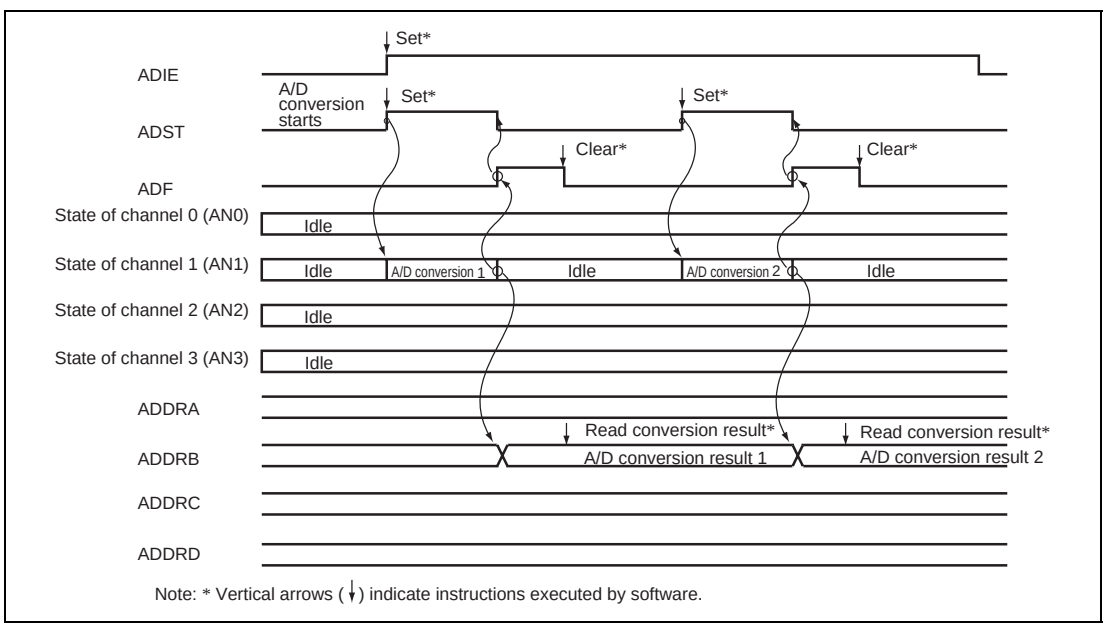


Figure 15.3 A/D Conversion Timing (Single-Chip Mode, Channel 1 Selected)

Bit	Bit Name	Initial Value	R/W	Description
2	PV1	0	R/W	Program-Verify When this bit is set to 1, the flash memory transits to program-verify mode. When it is cleared to 0, program-verify mode is cancelled. [Setting condition] When FWE = 1 and SWE1 = 1
1	E1	0	R/W	Erase When this bit is set to 1 while the SWE1 and ESU1 bits are 1, the flash memory transits to erase mode. When it is cleared to 0, erase mode is cancelled. [Setting condition] When FWE = 1, SWE1 = 1, and ESU1 = 1
0	P1	0	R/W	Program When this bit is set to 1 while the SWE1 and PSU1 bits are 1, the flash memory transits to program mode. When it is cleared to 0, program mode is cancelled. [Setting condition] When FWE = 1, SWE1 = 1, and PSU1 = 1

Note: * Set according to the FWE pin state.

17.5.2 Flash Memory Control Register 2 (FLMCR2)

FLMCR2 is a register that displays the state of flash memory programming/erasing. FLMCR2 is a read-only register, and should not be written to.

Bit	Bit Name	Initial Value	R/W	Description
7	FLER	0	R	Indicates that an error has occurred during an operation on flash memory (programming or erasing). When FLER is set to 1, flash memory goes to the error-protection state. See section 17.9.3, Error Protection, for details.
6 to 0	—	All 0	—	Reserved These bits are always read as 0.

17.12 Power-Down States for Flash Memory

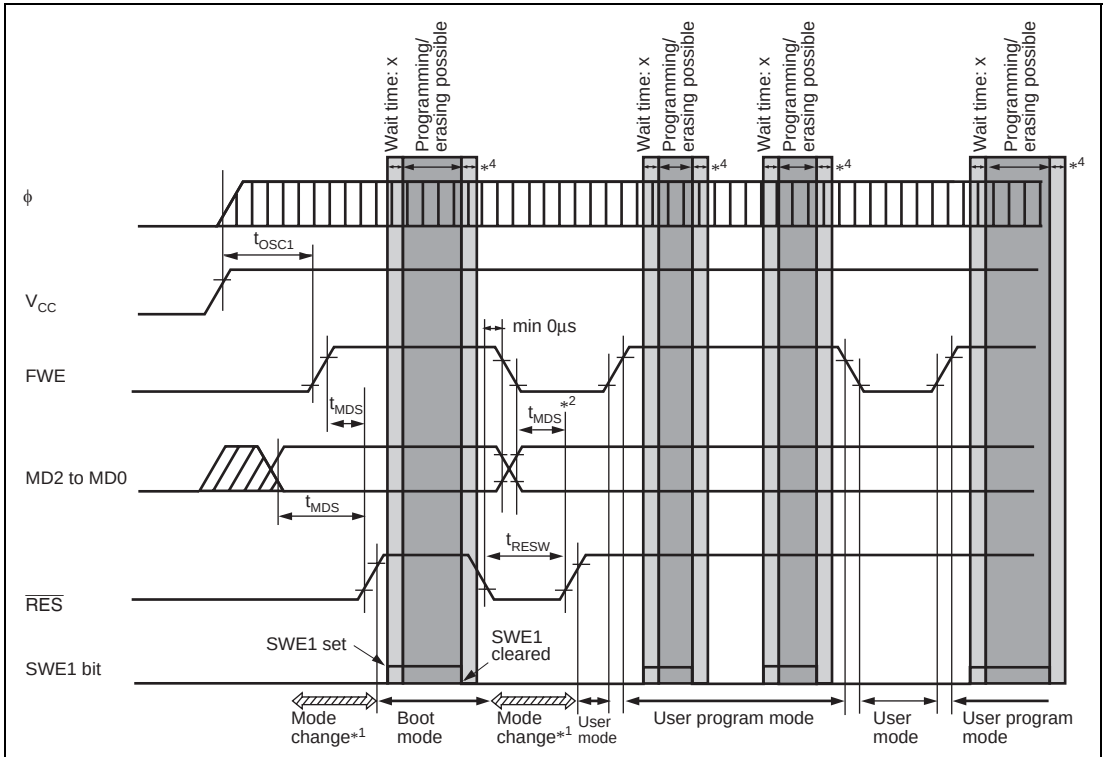
In user mode, the flash memory will operate in either of the following states:

- Normal operating mode
  The flash memory can be read and written to.
- Standby mode
  All flash memory circuits are halted.
- Power-down state
  The flash memory can be read when part of the power supply circuit is halted and the LSI operates by subclocks.

Table 17.8 shows the correspondence between the operating modes of this LSI and the flash memory. When the flash memory returns to normal operation from a power-down state, a power supply circuit stabilization period is needed. When the flash memory returns to its normal operating state from watch mode or standby mode, bits STS2 to STS0 in SBYCR must be set to provide a wait time of at least 100 μs; when returns from flash memory module stop mode, the software wait state should be set.

Table 17.8 Flash Memory Operating States

LSI Operating State	Flash Memory Operating State
Active mode Sleep mode	Normal operating mode
Watch mode Standby mode Flash memory module stop mode	Standby mode (Before entering to the normal operation mode, wait time of at least 100 μs is required.)
Subactive mode Subsleep mode	Power-down mode (read only)



Notes: 1. When entering boot mode or making a transition from boot mode to another mode, mode switching must be carried out by means of $\overline{RES}$ input
2. When making a transition from boot mode to another mode, a mode programming setup time t_{MDS} (min) of 200 ns is necessary with respect to $\overline{RES}$ clearance timing.
3. See section 22.7, Flash Memory Characteristics.
4. Wait time: θ.

Figure 17.18 Mode Transition Timing
(Example: Boot Mode → User Mode ↔ User Program Mode)

22.3 DC Characteristics

Table 22.2 lists the DC characteristics. Table 22.3 lists the permissible output currents.

Table 22.2 DC Characteristics

Condition A: V_{CC} = PLL V_{CC} = Dr V_{CC} = 2.4 V to 3.6 V, Vref = 2.4 V to V_{CC}, V_{SS} = PLLV_{SS} = Dr V_{SS} = 0 V, f = 32.768 kHz, 6 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = PLL V_{CC} = Dr V_{CC} = 2.7 V to 3.6 V, Vref = 2.7 V to V_{CC}, V_{SS} = PLLV_{SS} = Dr V_{SS} = 0 V, f = 32.768 kHz, 6 MHz to 16 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = PLL V_{CC} = Dr V_{CC} = 3.0 V to 3.6 V, Vref = 3.0 V to V_{CC}, V_{SS} = PLLV_{SS} = Dr V_{SS} = 0 V, f = 32.768 kHz, 6 MHz to 24 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition D: V_{CC} = PLL V_{CC} = Dr V_{CC} = 3.0 V to 3.6 V, Vref = 3.0 V to V_{CC}, V_{SS} = PLLV_{SS} = Dr V_{SS} = 0 V, f = 32.768 kHz, 16 MHz to 24 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	$\overline{IRQ0}$ to $\overline{IRQ4}$	V_T^-	$V_{CC} \times 0.2$	—	—	V	
	$\overline{IRQ7}$	V_T^+	—	—	$V_{CC} \times 0.8$	V	
		$V_T^+ - V_T^-$	$V_{CC} \times 0.05$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD2 to MD0, $\overline{TRST}$, TCK, TMS, TDI, EMLE, VBUS, $\overline{UBPM}$, FWE*[4]	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	EXTAL, ports 1, 3, 4, 7, 9, and A to G		$V_{CC} \times 0.8$	—	V_{CC} + 0.3	V	

3. Block erase time (Shows the total period for which the E1-bit FLMCR1 is set. It does not include the erase verification time.)
4. Maximum programming time value

   t_p (max.) = Wait time after P1 bit set (z) × maximum programming count (N1 + N2)

   = (Z0 + Z2) × 6 + Z1 × 994
5. Maximum erasure time value

   t_E (max.) = Wait time after E1 bit set (z) × maximum erasure count (N)
6. Minimum times that guarantee all characteristics after programming. (The guaranteed range is 1 to the minimum value.)
7. Reference value when the temperature is 25°C. (It is reference that reprogramming is normally enabled up to this value.)
8. Data hold characteristics when reprogramming is performed within the range of specifications including the minimum value.

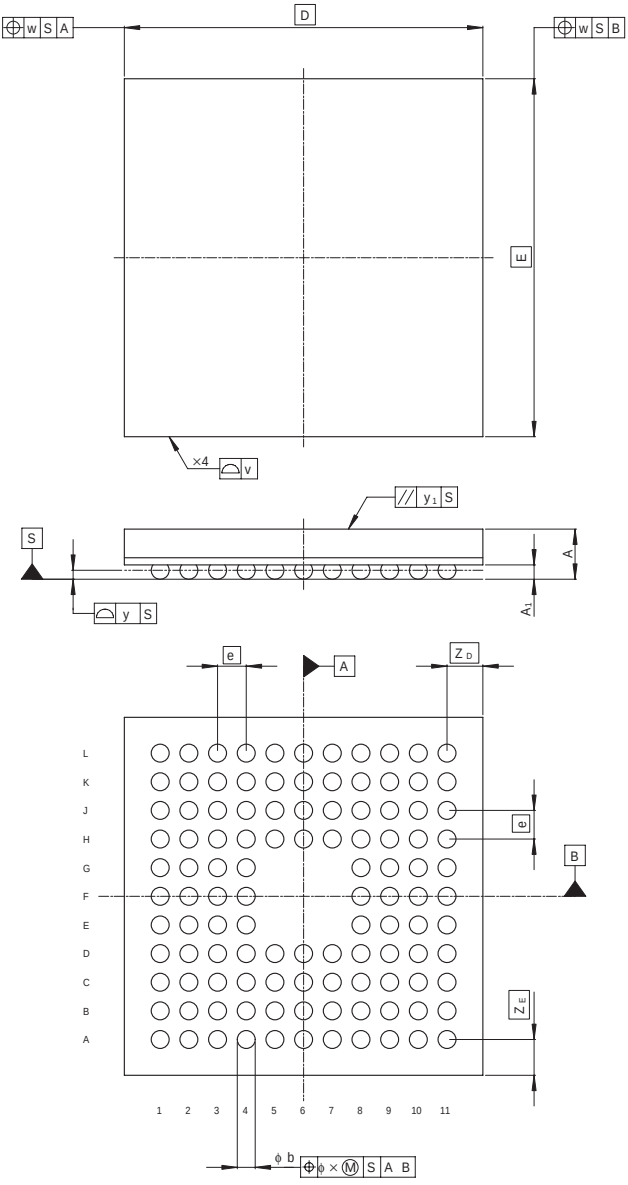
22.8 Usage Note

General Notice during Design for Printed Circuit Board: Measures for radiation noise caused by the transient current in this LSI should be taken into consideration. The examples of the measures are shown below.

- To use a multilayer printed circuit board which includes layers for Vcc and GND.
- To mount by-pass capacitors (approximately 0.1 μF) between the Vcc and GND (Vss) pins, and the PLLVcc and PLLGND pins, of this LSI.

Characteristics of F-ZTAT and Masked ROM Versions: Though the F-ZTAT version and the masked ROM version satisfy electrical characteristics described in this manual, the actual value of electrical characteristics, operating margin, and noise margin may differ due to the differences of production process, on-chip ROM, and layout patterning.
When the system has been evaluated with the F-ZTAT version, the equivalent evaluation should be implemented to the masked ROM version when shifted to the masked ROM version.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA112-10x10-0.80	PLBG0112GA-A	BP-112/BP-112V	0.3g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.00	—
E	—	10.00	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	1.00	—
Z_E	—	1.00	—

Figure C.2 BP-112 and BP-112V Package Dimensions