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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	24MHz
Connectivity	SCI, SmartCard, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	69
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2218cubr24v

Configuration of This Manual

This manual comprises the following items:

1. General Precautions on Handling of Product
2. Configuration of This Manual
3. Preface
4. Main Revisions for This Edition (only for revised versions)

The list of revisions is a summary of points that have been revised or added to earlier versions. This does not include all of the revised contents. For details, see the actual locations in this manual.

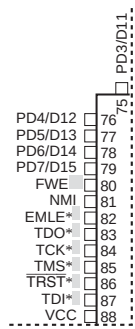
5. Contents
6. Overview
7. Description of Functional Modules
   - CPU and System-Control Modules
   - On-Chip Peripheral Modules

     The configuration of the functional description of each module differs according to the module. However, the generic style includes the following items:

   i) Feature
   ii) Input/Output Pin
   iii) Register Description
   iv) Operation
   v) Usage Note

When designing an application system that includes this LSI, take notes into account. Each section includes notes in relation to the descriptions given, and usage notes are given, as required, as the final part of each section.

8. List of Registers
9. Electrical Characteristics
10. Appendix
11. Index

Item	Page	Revision (See Manual for Details)
1.2 Internal Block Diagram Figure 1.4 Internal Block Diagram of HD6432211, HD6432210 and HD6432210S	6	Note amended 1. The FWE pin is provided only in the flash memory version.
1.3 Pin Arrangements	7	Description amended The pin arrangements of the HD64F2218, HD64F2218U, HD64F2218CU and HD64F2217CU are shown in figures 1.5 and 1.6. The pin arrangements of the HD6432217 are shown in figures 1.7 and 1.8. The pin arrangements of the HD64F2212, HD64F2212U, HD64F2212CU, HD64F2211, HD64F2211U, HD64F2211CU and HD64F2210CU are shown in figures 1.9 and 1.11.
Figure 1.5 Pin Arrangements of HD64F2218, HD64F2218U, HD64F2218CU and HD64F2217CU (TFP-100G, TFP-100GV)		Title and figure amended  Note *1 shown below deleted Notes: 1. The FWE pin is provided only in the HD64F2218, andHD64F2218U.

6.3.2 Access State Control Register (ASTCR)

ASTCR designates each area as either a 2-state access space or a 3-state access space.

ASTCR sets the number of access states for the external memory space. The number of access states for on-chip memory and internal I/O registers except for the on-chip USB is fixed regardless of the settings in ASTCR.

Bit	Bit Name	Initial Value	R/W	Description
7	AST7*	1	R/W	Area 7 to 0 Access State Control:
6	AST6*	1	R/W	These bits select whether the corresponding area is to be designated as a 2-state access space or a 3-state access space. Wait state insertion is enabled or disabled at the same time.
5	AST5	1	R/W	
4	AST4	1	R/W	
3	AST3	1	R/W	0: Area n is designated for 2-state access Wait state insertion in area n external space is disabled
2	AST2	1	R/W	
1	AST1	1	R/W	
0	AST0	1	R/W	1: Area n is designated for 3-state access Wait state insertion in area n external space is enabled
				Legend: n = 7 to 0

Note: * The on-chip USB and on-chip RTC are allocated to area 6 and area 7, respectively. Therefore, these bits should be set to 1.

6.3.5 Bus Control Register L (BCRL)

BCRL performs selection of the external bus-released state protocol, and enabling or disabling of $\overline{\text{WAIT}}$ pin input.

The functions selected by this register are available only in the H8S/2218 Group. This register should not be modified in the H8S/2212 Group.

Bit	Bit Name	Initial Value	R/W	Description
7	BRLE*	0	R/W	Bus Release Enable Enables or disables external bus release. 0: External bus release is disabled. $\overline{\text{BREQ}}$ and $\overline{\text{BACK}}$ can be used as I/O ports. 1: External bus release is enabled.
6	–	0	R/W	Reserved The write value should always be 0.
5	–	0	–	Reserved This bit is always read as 0 and cannot be modified.
4	–	0	R/W	Reserved The write value should always be 0.
3	–	1	R/W	Reserved The write value should always be 1.
2, 1	–	All 0	R/W	Reserved The write value should always be 0.
0	WAITE*	0	R/W	WAIT Pin Enable Selects enabling or disabling of wait input by the $\overline{\text{WAIT}}$ pin. 0: Wait input by $\overline{\text{WAIT}}$ pin disabled. $\overline{\text{WAIT}}$ pin can be used as I/O port. 1: Wait input by $\overline{\text{WAIT}}$ pin enabled.

Note: * These bits should be set to 0 in the H8S/2212 Group.

Bit	Bit Name	Initial Value	R/W	Description
				Data Transfer Interrupt Enable B Enables or disables an interrupt to the CPU when transfer is interrupted. If the DTIEB bit is set to 1 when DTME = 0, the DMAC regards this as indicating a break in the transfer, and issues a transfer break interrupt request to the CPU. A transfer break interrupt can be canceled either by clearing the DTIEB bit to 0 in the interrupt handling routine, or by performing processing to continue transfer by setting the DTME bit to 1.
3	DTIE1B	0	R/W	Data Transfer Interrupt Enable 1B Enables or disables the channel 1 transfer break interrupt. 0: Transfer break interrupt disabled 1: Transfer break interrupt enabled
				Data Transfer End Interrupt Enable A Enables or disables an interrupt to the CPU when transfer ends. If the DTIEA bit is set to 1 when DTE = 0, the DMAC regards this as indicating the end of a transfer, and issues a transfer end interrupt request to the CPU. A transfer end interrupt can be canceled either by clearing the DTIEA bit to 0 in the interrupt handling routine, or by performing processing to continue transfer by setting the DTE bit to 1.
2	DTIE1A	0	R/W	Data Transfer End Interrupt Enable 1A Enables or disables the channel 1 transfer end interrupt. 0: Transfer end interrupt disabled 1: Transfer end interrupt enabled
1	DTIE0B	0	R/W	Data Transfer Interrupt Enable 0B Enables or disables the channel 0 transfer break interrupt. 0: Transfer break interrupt disabled 1: Transfer break interrupt enabled
0	DTIE0A	0	R/W	Data Transfer End Interrupt Enable 0A Enables or disables the channel 0 transfer end interrupt. 0: Transfer end interrupt disabled 1: Transfer end interrupt enabled

7.4.11 Relation between the DMAC and External Bus Requests

There can be no break between a DMA cycle read and a DMA cycle write. This means that an external bus release cycle is not generated between the external read and external write in a DMA cycle.

In the case of successive read and write cycles, such as in burst transfer or block transfer, an external bus released state may be inserted after a write cycle.

When DMA cycle reads or writes are accesses to on-chip memory or internal I/O registers, these DMA cycles can be executed at the same time as refresh cycles or external bus release. However, simultaneous operation may not be possible when a write buffer is used.

7.4.12 NMI Interrupts and DMAC

When an NMI interrupt is requested, burst mode transfer in full address mode is interrupted. An NMI interrupt does not affect the operation of the DMAC in other modes.

In full address mode, transfer is enabled for a channel when both the DTE bit and the DTME bit are set to 1. With burst mode setting, the DTME bit is cleared when an NMI interrupt is requested.

If the DTME bit is cleared during burst mode transfer, the DMAC discontinues transfer on completion of the 1-byte or 1-word transfer in progress, then releases the bus, which passes to the CPU.

The channel on which transfer was interrupted can be restarted by setting the DTME bit to 1 again. Figure 7.21 shows the procedure for continuing transfer when it has been interrupted by an NMI interrupt on a channel designated for burst mode transfer.

8.7.4 Port B Pull-Up MOS Control Register (PBPCR)

PBPCR controls the on/off state of the port B input pull-up MOS. PBPCR is valid for port input pins.

Bit	Bit Name	Initial Value	R/W	Description
7	PB7PCR	0	R/W	When a pin functions as an input port, setting the corresponding bit to 1 turns on the input pull-up MOS for that pin.
6	PB6PCR	0	R/W	
5	PB5PCR	0	R/W	
4	PB4PCR	0	R/W	
3	PB3PCR	0	R/W	
2	PB2PCR	0	R/W	
1	PB1PCR	0	R/W	
0	PB0PCR	0	R/W	

Status Flag Clearing Timing: After a status flag is read as 1 by the CPU, it is cleared by writing 0 to it. When the DMAC is activated, the flag is cleared automatically. Figure 9.42 shows the timing for status flag clearing by the CPU, and figure 9.43 shows the timing for status flag clearing by the DMAC.

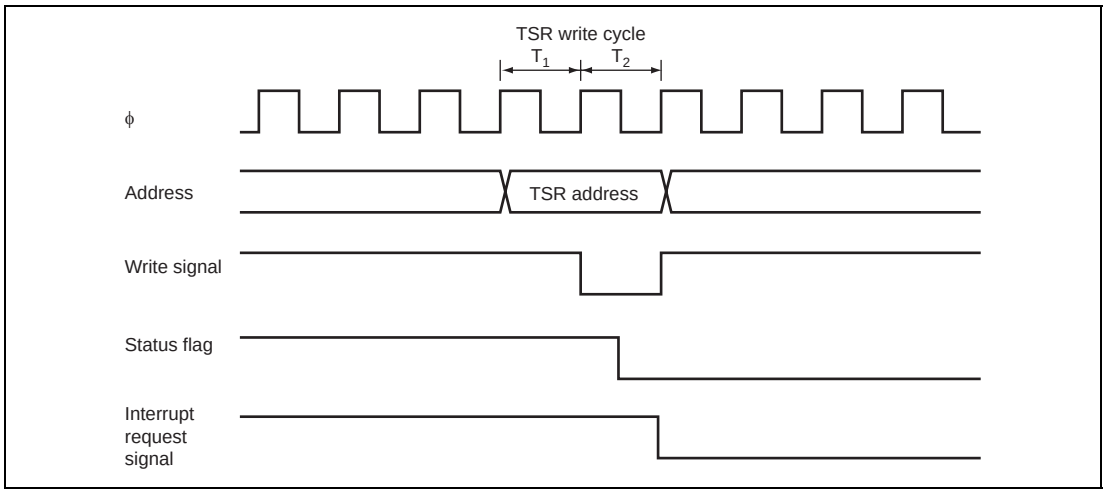


Figure 9.42 Timing for Status Flag Clearing by CPU

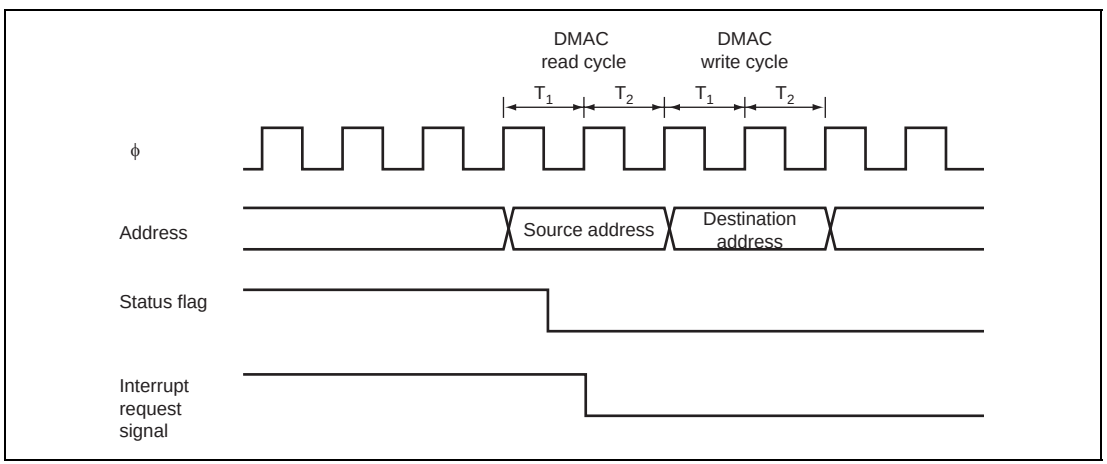


Figure 9.43 Timing for Status Flag Clearing by DMAC Activation

11.2 Input/Output Pin

Table 11.1 shows the RTC input/output pin.

Table 11.1 Pin Configuration

Name	Abbreviation	I/O	Function
Clock output	TMOW	Output	RTC divided clock output

11.3 Register Descriptions

The RTC has the following registers.

- Second data register (RSECDR)
- Minute data register (RMINDR)
- Hour data register (RHRDR)
- Day-of-week data register (RWKDR)
- RTC control register 1 (RTCCR1)
- RTC control register 2 (RTCCR2)
- Clock source select register (RTCCSR)
- Extended module stop register (EXMDLSTP)

11.3.1 Second Data Register (RSECDR)

RSECDR counts the BCD-coded second value. This register is initialized to H'00 by a $\overline{\text{STBY}}$ input or the RST bit in RTCCR1, but not initialized by a $\overline{\text{RES}}$ input. The setting range is decimal 00 to 59. For more information on reading seconds, minutes, hours, and day-of-week, see section 11.4.2, Time Data Reading Procedure.

- Smart Card Interface Mode (When SMIF in SCMR is 1)

Bit	Bit Name	Initial Value	R/W	Description
7	GM	0	R/W	GSM Mode Setting this bit to 1 allows GSM mode operation. In GSM mode, the TEND set timing is put forward to 11.0 etu from the start and the clock output control function is appended. For details, see section 12.7.9, Clock Output Control. 0: Normal smart card interface mode operation (initial value) (1) The TEND flag is generated 12.5 etu (11.5 etu in the block transfer mode) after the beginning of the start bit. (2) Clock output on/off control only. 1: GSM mode operation in smart card interface mode (1) The TEND flag is generated 11.0 etu after the beginning of the start bit. (2) In addition to clock output on/off control, high/how fixed control is supported (set using SCR).
6	BLK	0	R/W	Setting this bit to 1 allows block transfer mode operation. For details, see section 12.7.4, Block Transfer Mode. 0: Normal smart card interface mode operation (initial value) (1) Error signal transmission, detection, and automatic data retransmission are performed. (2) The TXI interrupt is generated by the TEND flag. (3) The TEND flag is set 12.5 etu (11.0 etu in the GSM mode) after transmission starts. 1: Operation in block transfer mode (1) Error signal transmission, detection, and automatic data retransmission are not performed. (2) The TXI interrupt is generated by the TDRE flag. (3) The TEND flag is set 11.5 etu (11.0 etu in the GSM mode) after transmission starts.

Bit	Bit Name	Initial Value	R/W	Description
7	ACS3	0	R/W	Asynchronous Clock Source Select Selects the clock source in asynchronous mode depending on the combination with the ACS2 to ACS0 (bits 2 to 0 in SEMRA_0). For details, see section 12.3.9, Serial Extended Mode Register A_0 (SEMRA_0).
6 to 4	—	Undefined	—	Reserved The write value should always be 0.
3	TIOCA2E	1	R/W	TIOCA2 Output Enable Controls the TIOCA2 output on the P16 pin. When the TIOCA2 in TPU is output to generate the transfer clock, P16 is used as other function pin by setting this bit to 0. 0: Disables output of TIOCA2 in TPU 1: Enables output of TIOCA2 in TPU
2	TIOCA1E	1	R/W	TIOCA1 Output Enable Controls the TIOCA1 output on the P14 pin. When the TIOCA1 in TPU is output to generate the transfer clock, P14 is used as other function pin by setting this bit to 0. 0: Disables output of TIOCA1 in TPU 1: Enables output TIOCA1 in TPU
1	TIOCC0E	1	R/W	TIOCC0 Output Enable Controls the TIOCC0 output on the P12 pin. When the TIOCC0 in TPU is output to generate the transfer clock, P12 is used as other function pin by setting this bit to 0. 0: Disables output of TIOCC0 in TPU 1: Enables output of TIOCC0 in TPU
0	TIOCA0E	1	R/W	TIOCA0 Output Enable Controls the TIOCA0 output on the P10 pin. When the TIOCA0 in TPU is output to generate the transfer clock, P10 is used as other function pin by setting this bit to 0. 0: Disables output of TIOCA0 in TPU 1: Enables output of TIOCA0 in TPU

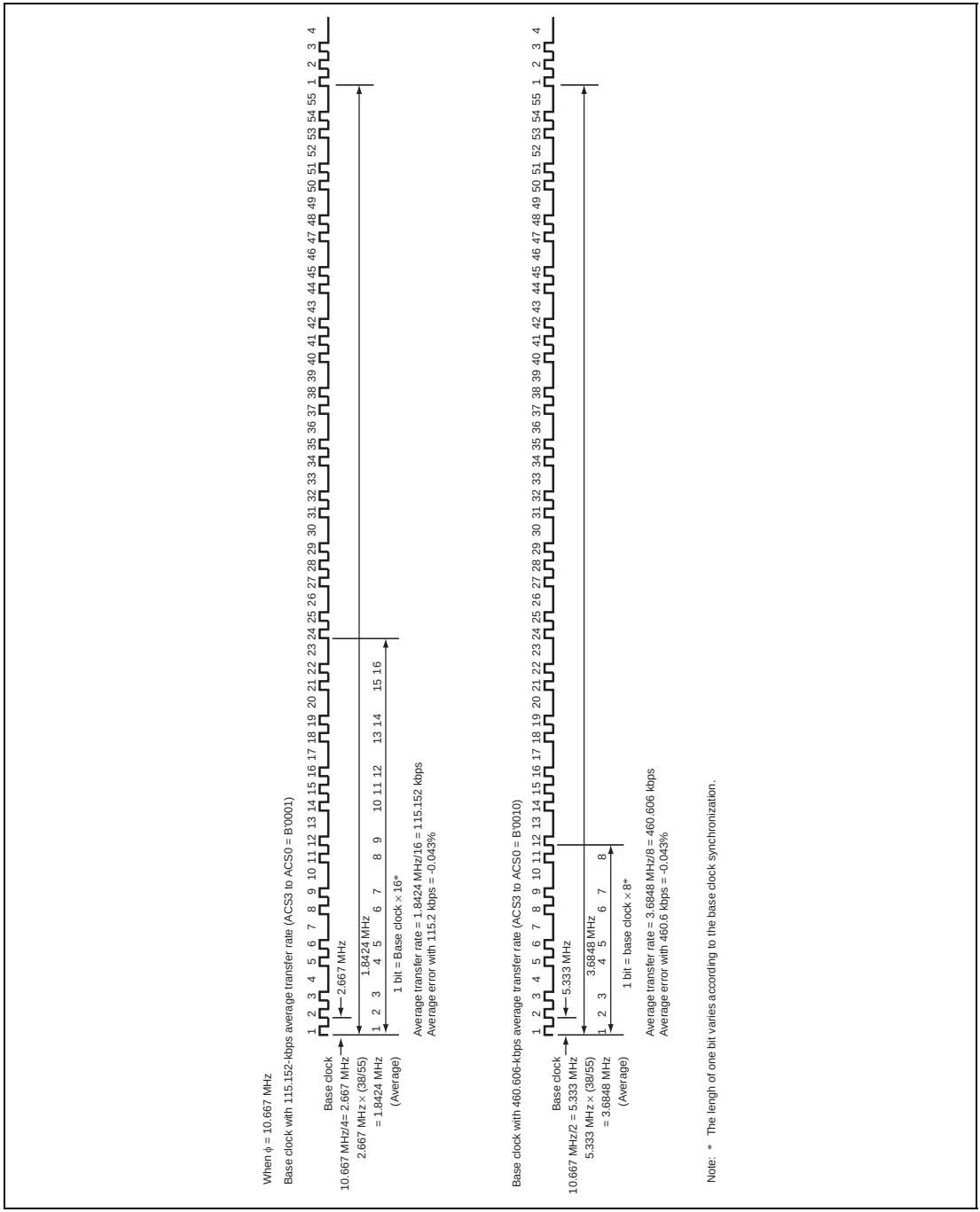


Figure 12.3 Examples of Base Clock when Average Transfer Rate Is Selected (1)

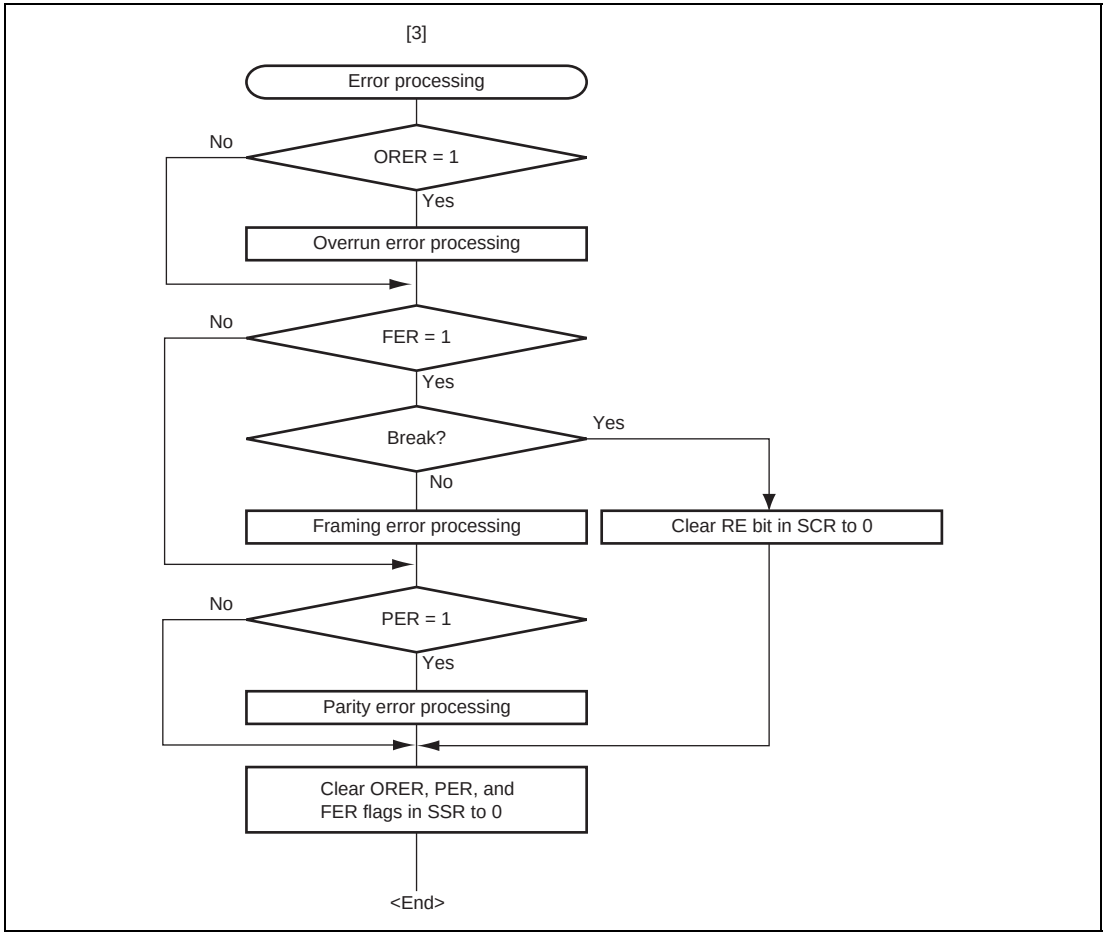


Figure 12.12 Sample Serial Data Reception Flowchart (2)

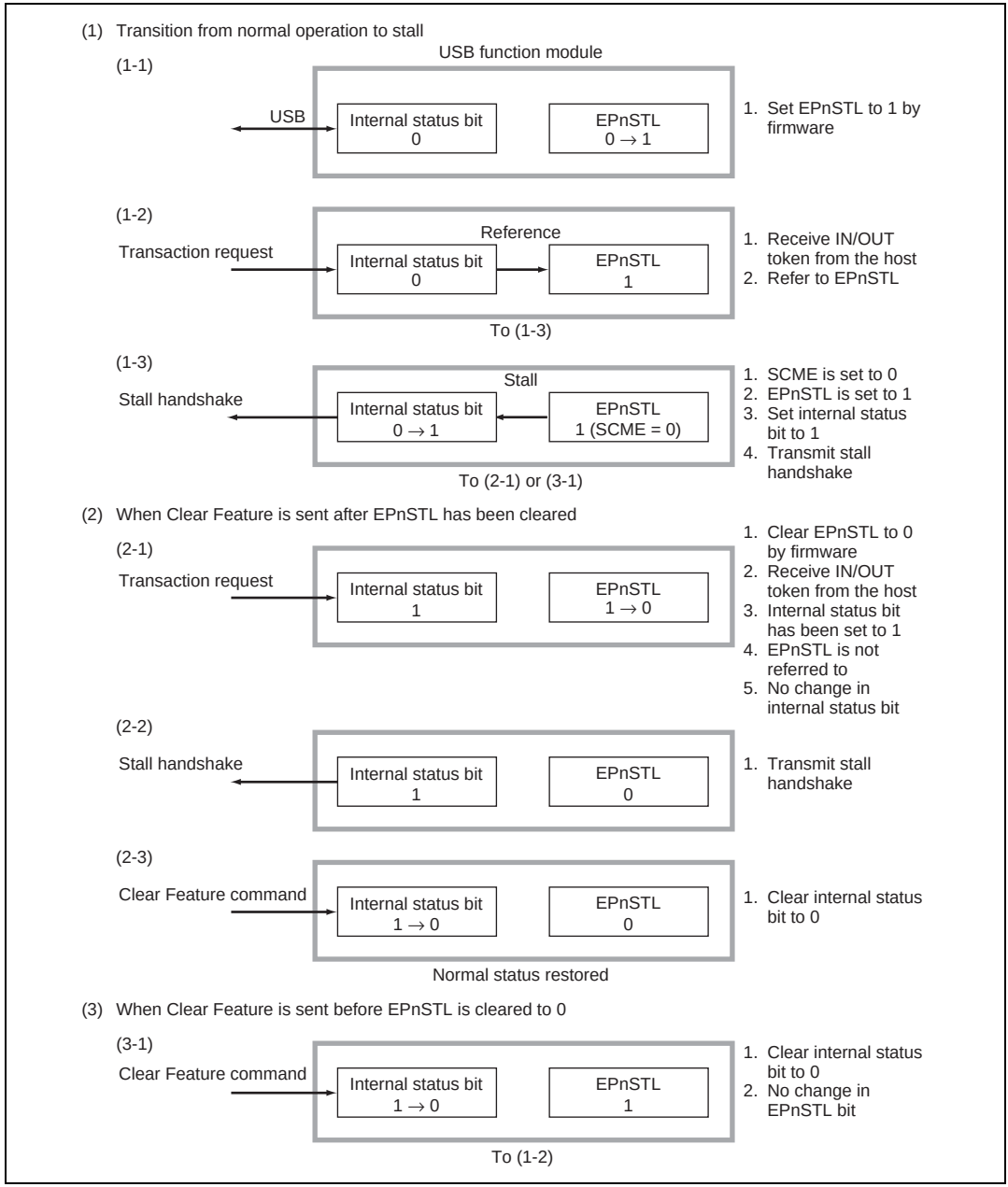


Figure 14.20 Forcible Stall by Firmware

Section 15 A/D Converter

This LSI includes a successive approximation type 10-bit A/D converter that allows up to six analog input channels to be selected. The block diagram of the A/D converter is shown in figure 15.1.

15.1 Features

- 10-bit resolution
- Six input channels
- Conversion time: 8.1 µs per channel (at 16-MHz operation), 10.7 µs per channel (at 24-MHz operation), 21.8 µs per channel (at 6-MHz operation)
- Two operating modes
  - Single mode: Single-channel A/D conversion
  - Scan mode: Continuous A/D conversion on 1 to 4 channels
- Four data registers
  - Conversion results are held in a 16-bit data register for each channel
- Sample and hold function
- Three methods conversion start
  - Software
  - Timer (TPU) conversion start trigger
  - External trigger signal ($\overline{\text{ADTRG}}$)
- Interrupt request
  - An A/D conversion end interrupt request (ADI) can be generated
- Module stop mode can be set
- Settable analog conversion voltage range

  Analog conversion voltage range settable using the reference voltage pin (Vref) as the reference voltage

19.9 Usage Notes

19.9.1 Note on Crystal Resonator

Since various characteristics related to the crystal resonator are closely linked to the user's board design, thorough evaluation is necessary on the user's part, using the resonator connection examples shown in this section as a guide. As the resonator circuit ratings will depend on the floating capacitance of the resonator and the mounting circuit, the ratings should be determined in consultation with the resonator manufacturer. The design must ensure that a voltage exceeding the maximum rating is not applied to the oscillator pin.

19.9.2 Note on Board Design

When designing the board, place the crystal resonator and its load capacitors as close as possible to the XTAL or OSC1 and EXTAL or OSC2 pins. Other signal lines should be routed away from the oscillator circuit to prevent induction from interfering with correct oscillation. See figure 19.10.

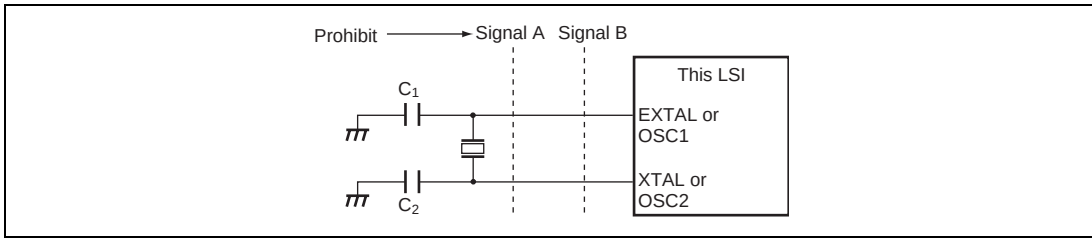


Figure 19.10 Note on Board Design of Oscillator Circuit

19.9.3 Note on Switchover of External Clock

When two or more external clocks (e.g. 16 MHz and 13 MHz) are used as the system clock, switchover of the input clock should be carried out in software standby mode.

An example of an external clock switching circuit is shown in figure 19.11, and an example of the external clock switchover timing in figure 19.12.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
UISR1	—	—	—	—	—	EP2 READYS	EP1TRS	EP1 EMPTYS	USB
UISR3	CK48 READYS	SOFS	SETCS	—	—	—	—	VBUSiS	
UDSR	—	—	—	—	—	EP1DE	EP3DE	EP0iDE	
UCVR	—	—	CNFV0	—	—	—	—	—	
UTSTR0	PTSTE	—	—	—	SUSPEND	$\overline{OE}$	FSE0	VPO	
UTSTR1	VBUS	$\overline{UBPM}$	—	—	—	RCV	VP	VM	
UTSTR2	—	—	—	—	—	—	—	—	
UTSTRB	—	—	—	—	—	—	—	—	
UTSTRC	—	—	—	—	—	—	—	—	
UTSTRD	—	—	—	—	—	—	—	—	
UTSTRE	—	—	—	—	—	—	—	—	
UTSTRF	—	—	—	—	—	—	—	—	
SCRX	—	—	—	—	FLSHE	—	—	—	FLASH
SBYCR	SSBY	STS2	STS1	STS0	OPE	—	—	—	SYSTEM
SYSCR	—	—	INTM1	INTM0	NMIEG	MRESE	—	RAME	
SCKCR	PSTOP	—	—	—	—	SCK2	SCK1	SCK0	
MDCR	—	—	—	—	FWE	MDS2	MDS1	MDS0	
MSTPCRA	MSTPA7	MSTPA6	MSTPA5	MSTPA4	MSTPA3	MSTPA2	MSTPA1	MSTPA0	
MSTPCRB	MSTPB7	MSTPB6	MSTPB5	MSTPB4	MSTPB3	MSTPB2	MSTPB1	MSTPB0	
MSTPCRC	MSTPC7	MSTPC6	MSTPC5	MSTPC4	MSTPC3	MSTPC2	MSTPC1	MSTPC0	
PFCR	—	—	—	—	AE3	AE2	AE1	AE0	BSC
LPWRCR	DTON	LSON	NESEL	SUBSTP	RFCUT	—	STC1	STC0	SYSTEM
OUTCR	—	—	—	—	—	PF7OUT2	PF7OUT1	PF7OUT0	PORT
SEMRA_0	SSE	TCS2	TCS1	TCS0	ABCS	ACS2	ACS1	ACS0	SCI_0
SEMRB_0	ACS3	—	—	—	TIOCA2E	TIOCA1E	TIOCC0E	TIOCA0E	
ISCRH	IRQ7SCB	IRQ7SCA	IRQ6SCB	IRQ6SCA	IRQ5SCB	IRQ5SCA	IRQ4SCB	IRQ4SCA	INT
ISCRL	IRQ3SCB	IRQ3SCA	IRQ2SCB	IRQ2SCA	IRQ1SCB	IRQ1SCA	IRQ0SCB	IRQ0SCA	
IER	IRQ7E	IRQ6E	IRQ5E	IRQ4E	IRQ3E	IRQ2E	IRQ1E	IRQ0E	
ISR	IRQ7F	IRQ6F	IRQ5F	IRQ4F	IRQ3F	IRQ2F	IRQ1F	IRQ0F	

Register Name	Power-on Reset	Manual Reset	High-Speed	Medium-Speed	Sleep	Module Stop	Watch	Subactive	Subsleep	Software Standby	Hardware Standby	Module
UTSTR0	Initialized*	—	—	—	—	—	—	—	—	—	Initialized	USB
UTSTR1	Initialized*	—	—	—	—	—	—	—	—	—	Initialized	
UTSTR2	Initialized*	—	—	—	—	—	—	—	—	—	Initialized	
UTSTRB	Initialized*	—	—	—	—	—	—	—	—	—	Initialized	
UTSTRC	Initialized*	—	—	—	—	—	—	—	—	—	Initialized	
UTSTRD	Initialized*	—	—	—	—	—	—	—	—	—	Initialized	
UTSTRE	Initialized*	—	—	—	—	—	—	—	—	—	Initialized	
UTSTRF	Initialized*	—	—	—	—	—	—	—	—	—	Initialized	
SCRX	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	FLASH
SBYCR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	SYSTEM
SYSCR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
SCKCR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
MDCR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	
MSTPCRA	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
MSTPCRB	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
MSTPCRC	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
PFCR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	BSC
LPWRCR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	SYSTEM
OUTCR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	PORT
SEMRA_0	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	SCI_0
SEMRB_0	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
ISCRH	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	INT
ISCRL	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IER	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
ISR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
P1DDR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	PORT
P3DDR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	
P7DDR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	
PADDR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	
PBDDR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	
PCDDR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	