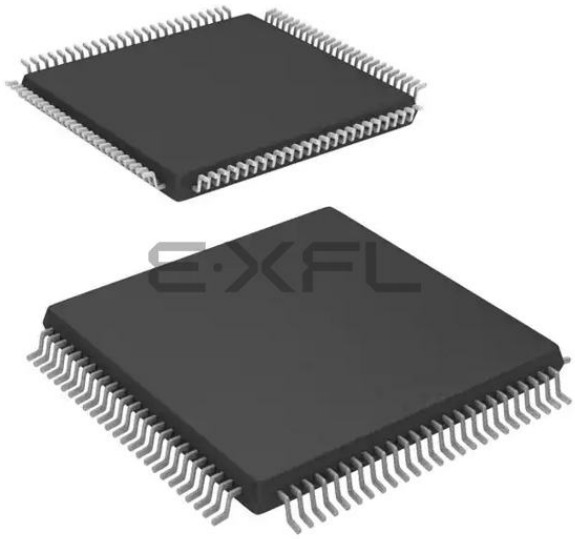

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	24MHz
Connectivity	SCI, SmartCard, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	69
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2218tf24v

Configuration of This Manual

This manual comprises the following items:

1. General Precautions on Handling of Product
2. Configuration of This Manual
3. Preface
4. Main Revisions for This Edition (only for revised versions)

The list of revisions is a summary of points that have been revised or added to earlier versions. This does not include all of the revised contents. For details, see the actual locations in this manual.

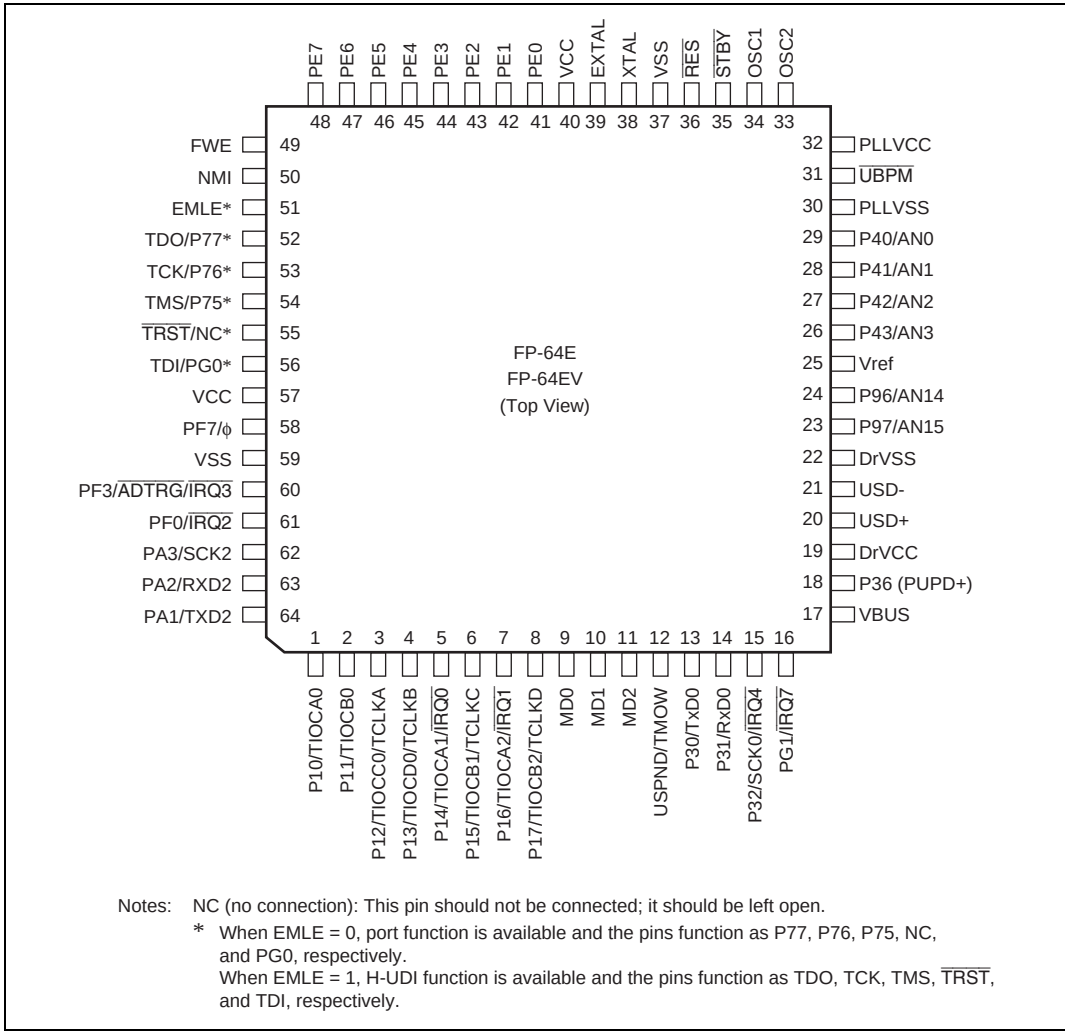
5. Contents
6. Overview
7. Description of Functional Modules
   - CPU and System-Control Modules
   - On-Chip Peripheral Modules

     The configuration of the functional description of each module differs according to the module. However, the generic style includes the following items:

   i) Feature
   ii) Input/Output Pin
   iii) Register Description
   iv) Operation
   v) Usage Note

When designing an application system that includes this LSI, take notes into account. Each section includes notes in relation to the descriptions given, and usage notes are given, as required, as the final part of each section.

8. List of Registers
9. Electrical Characteristics
10. Appendix
11. Index



Notes: NC (no connection): This pin should not be connected; it should be left open.

* When EMLE = 0, port function is available and the pins function as P77, P76, P75, NC, and PG0, respectively.
When EMLE = 1, H-UDI function is available and the pins function as TDO, TCK, TMS, $\overline{\text{TRST}}$, and TDI, respectively.

Figure 1.9 Pin Arrangements of HD64F2212, HD64F2212U, HD64F2212CU, HD64F2211, HD64F2211U, HD64F2211CU and HD64F2210CU (FP-64E, FP-64EV)

8-Bit 3-State Access Space (Except Area 6): Figure 6.11 shows the bus timing for an 8-bit 3-state access space in the H8S/2218 Group. When an 8-bit access space is accessed, the upper half (D15 to D8) of the data bus is used.

Wait states can be inserted.

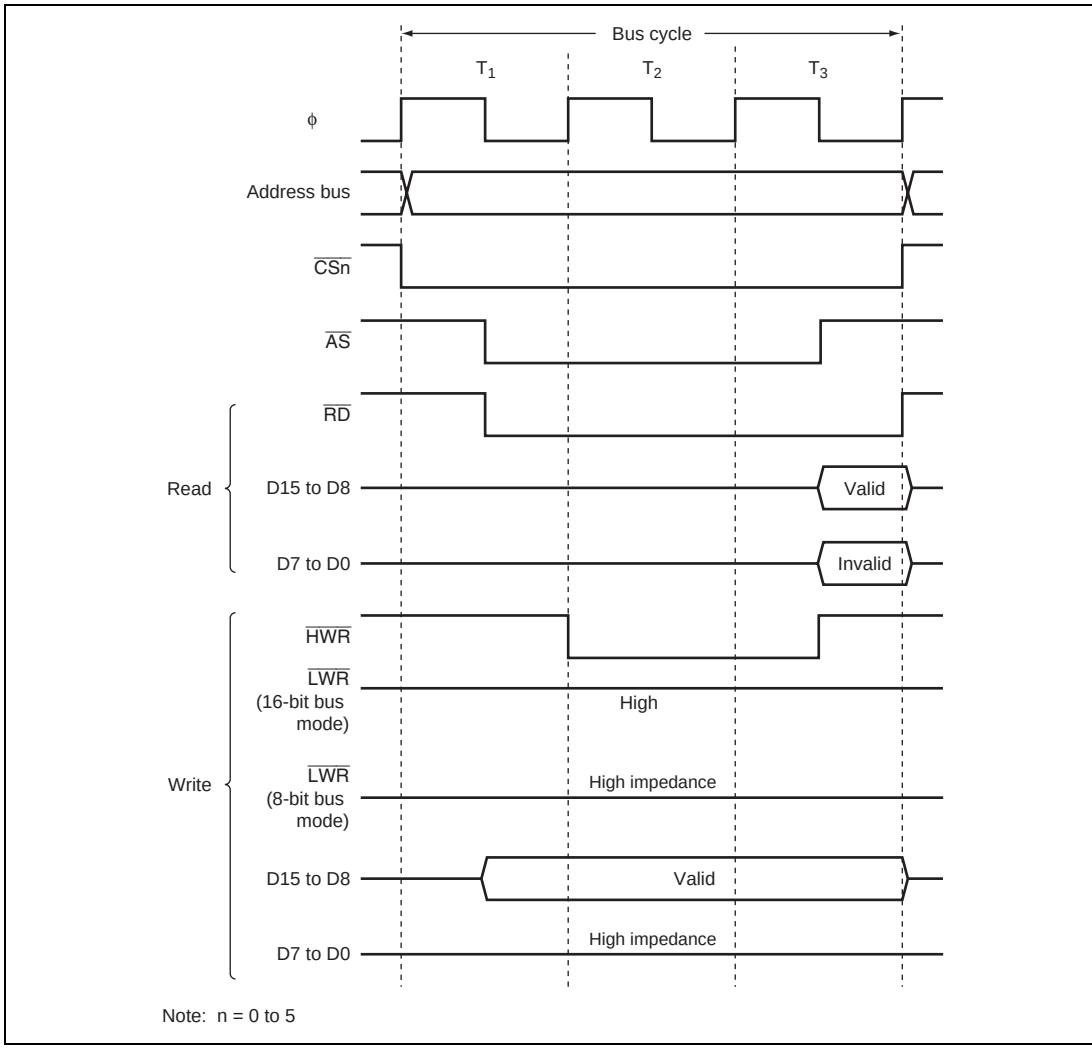


Figure 6.11 Bus Timing for 8-Bit 3-State Access Space (Except Area 6)

Figure 7.11 illustrates operation in block transfer mode when MARA is designated as a block area.

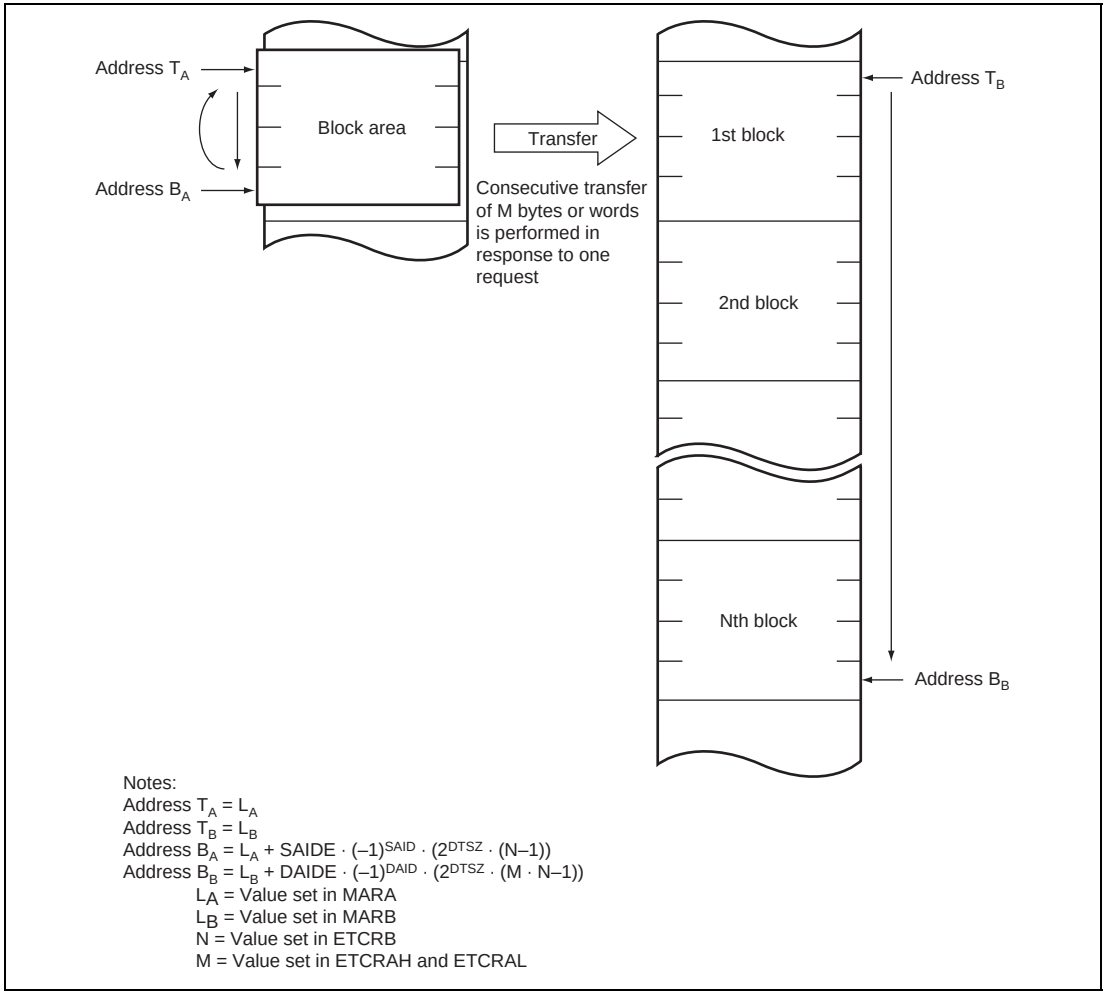


Figure 7.11 Operation in Block Transfer Mode (BLKDIR = 1)

ETCRAL is decremented by 1 each time a byte or word transfer is performed. In response to a single transfer request, burst transfer is performed until the value in ETCRAL reaches H'00. ETCRAL is then loaded with the value in ETCRAH. At this time, the value in the MAR register for which a block designation has been given by the BLKDIR bit in DMACRA is restored in accordance with the DTSZ, SAID/DAID, and SAIDE/DAIDE bits in DMACR.

ETCRB is decremented by 1 every block transfer, and when the count reaches H'0000 the DTE bit is cleared and transfer ends. If the DTIE bit is set to 1 at this point, an interrupt request is sent to the CPU. Figure 7.12 shows the operation flow in block transfer mode.

7.4.10 DMAC Multi-Channel Operation

The DMAC channel priority order is: channel 0 > channel 1, and channel A > channel B. Table 7.9 summarizes the priority order for DMAC channels.

Table 7.9 DMAC Channel Priority Order

Short Address Mode	Full Address Mode	Priority
Channel 0A	Channel 0	High
Channel 0B		
Channel 1A	Channel 1	
Channel 1B		Low

If transfer requests are issued simultaneously for more than one channel, or if a transfer request for another channel is issued during a transfer, when the bus is released the DMAC selects the highest-priority channel from among those issuing a request according to the priority order shown in table 7.9. During burst transfer, or when one block is being transferred in block transfer, the channel will not be changed until the end of the transfer. Figure 7.20 shows a transfer example in which transfer requests are issued simultaneously for channels 0A, 0B, and 1.

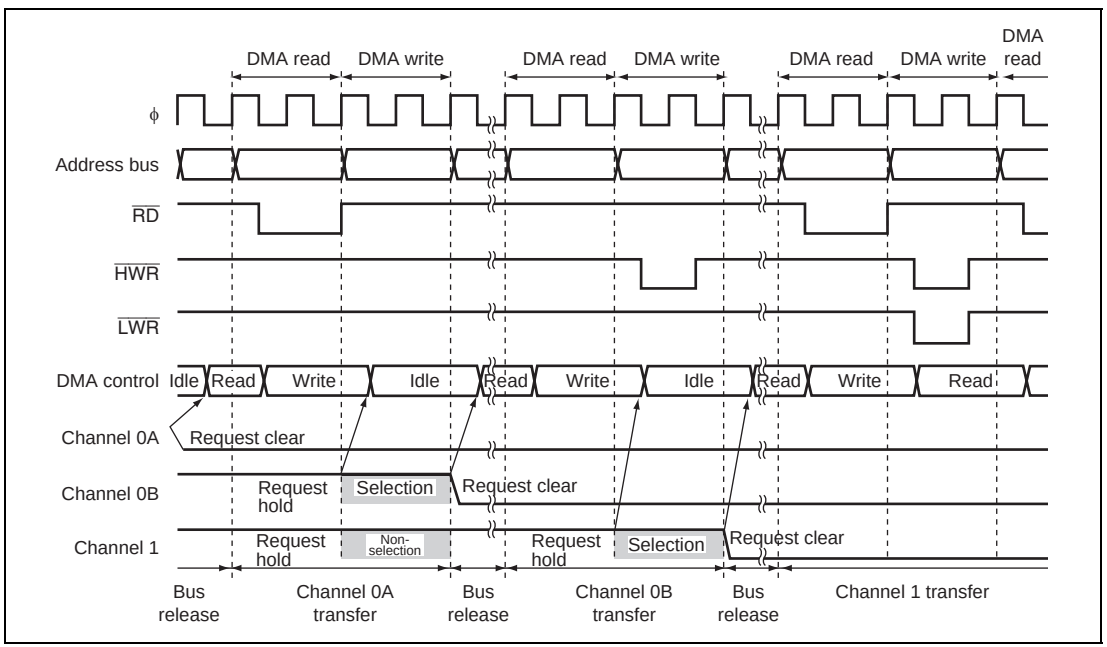


Figure 7.20 Example of Multi-Channel Transfer

8.8.4 Port C Pull-Up MOS Control Register (PCPCR)

PCPCR controls the on/off state of the port C input pull-up MOS.

Bit	Bit Name	Initial Value	R/W	Description
7	PC7PCR	0	R/W	When a pin functions as an input port, setting the corresponding bit to 1 turns on the input pull-up MOS for that pin.
6	PC6PCR	0	R/W	
5	PC5PCR	0	R/W	
4	PC4PCR	0	R/W	
3	PC3PCR	0	R/W	
2	PC2PCR	0	R/W	
1	PC1PCR	0	R/W	
0	PC0PCR	0	R/W	

8.8.5 Pin Functions

Port C pins also function as address bus (A7 to A0) output pins. The correspondence between the register specification and the pin functions is shown below.

Note: When using the RTC and USB with the emulator (E6000), set A7 to A0 as address bus output pins.

Table 8.46 PC7 Pin Function

Operating Mode	Modes 4 and 5	Mode 6		Mode 7	
PC7DDR	—	0	1	0	1
Pin Function	A7 output pin	PC7 input pin	A7 output pin	PC7 input pin	PC7 output pin

Table 8.47 PC6 Pin Function

Operating Mode	Modes 4 and 5	Mode 6		Mode 7	
PC6DDR	—	0	1	0	1
Pin Function	A6 output pin	PC6 input pin	A6 output pin	PC6 input pin	PC6 output pin

Table 8.70 PE1 Pin Function

Operating Mode	Modes 4 to 6			Mode 7	
Bus Mode	8-bit bus mode		16-bit bus mode	—	
PE1DDR	0	1	—	0	1
Pin Function	PE1 input pin	PE1 output pin	D1 input/output pin	PE1 input pin	PE1 output pin

Table 8.71 PE0 Pin Function

Operating Mode	Modes 4 to 6			Mode 7	
Bus Mode	8-bit bus mode		16-bit bus mode	—	
PE0DDR	0	1	—	0	1
Pin Function	PE0 input pin	PE0 output pin	D0 input/output pin	PE0 input pin	PE0 output pin

Pin Functions of H8S/2212 Group

The port E function as a general I/O port. The correspondence between the register specification and the pin function is shown below.

Table 8.72 PE7 Pin Function

PE7DDR	0	1
Pin Function	PE7 input pin	PE7 output pin

Table 8.73 PE6 Pin Function

PE6DDR	0	1
Pin Function	PE6 input pin	PE6 output pin

Table 8.74 PE5 Pin Function

PE5DDR	0	1
Pin Function	PE5 input pin	PE5 output pin

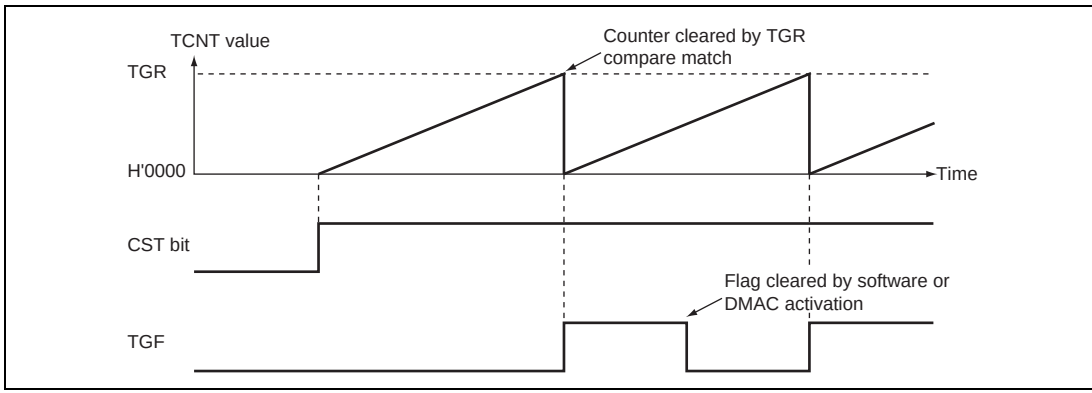


Figure 9.8 Periodic Counter Operation

Waveform Output by Compare Match: The TPU can perform 0, 1, or toggle output from the corresponding output pin using compare match.

1. Example of setting procedure for waveform output by compare match

   Figure 9.9 shows an example of the setting procedure for waveform output by compare match.

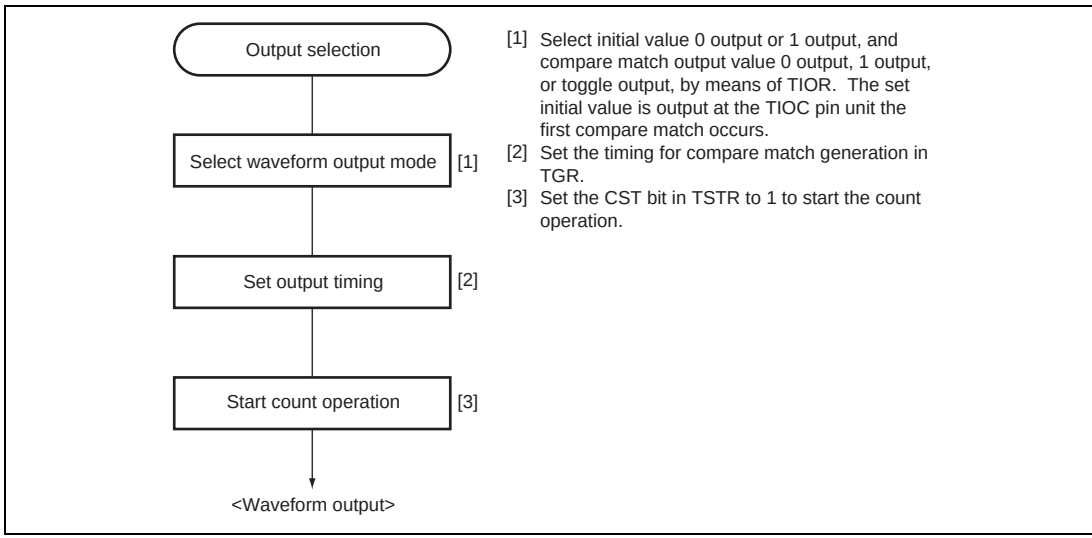


Figure 9.9 Example of Setting Procedure for Waveform Output by Compare Match

2. When TGR is an input capture register

   Figure 9.20 shows an operation example in which TGRA has been designated as an input capture register, and buffer operation has been designated for TGRA and TGRC. Counter clearing by TGRA input capture has been set for TCNT, and both rising and falling edges have been selected as the TIOCA pin input capture input edge. As buffer operation has been set, when the TCNT value is stored in TGRA upon occurrence of input capture A, the value previously stored in TGRA is simultaneously transferred to TGRC.

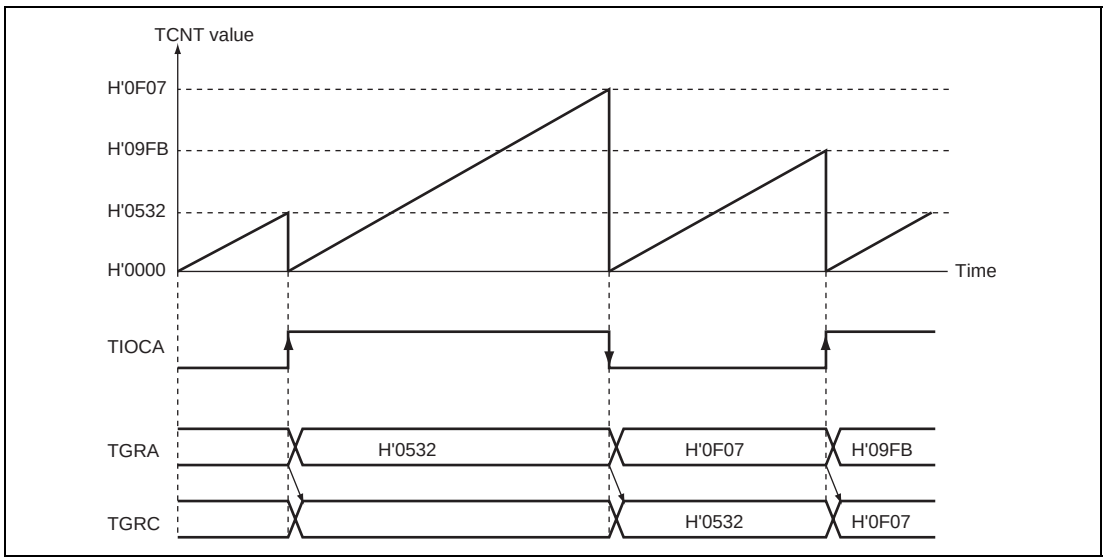


Figure 9.20 Example of Buffer Operation (2)

12.4.6 Serial Data Reception (Asynchronous Mode)

Figure 12.11 shows an example of operation for reception in asynchronous mode. In serial reception, the SCI operates as described below.

1. The SCI monitors the communication line. If a start bit is detected, the SCI performs internal synchronization, receives receive data in RSR, and checks the parity bit and stop bit.
2. If an overrun error occurs (when reception of the next data is completed while the RDRF flag is still set to 1), the ORER bit in SSR is set to 1. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated. Receive data is not transferred to RDR. The RDRF flag remains to be set to 1.
3. If a parity error is detected, the PER bit in SSR is set to 1 and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated.
4. If a framing error is detected (when the stop bit is 0), the FER bit in SSR is set to 1 and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated.
5. If reception is completed successfully, the RDRF bit in SSR is set to 1, and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an RXI interrupt request is generated. Continuous reception is possible because the RXI interrupt routine reads the receive data transferred to RDR before reception of the next receive data has been completed.

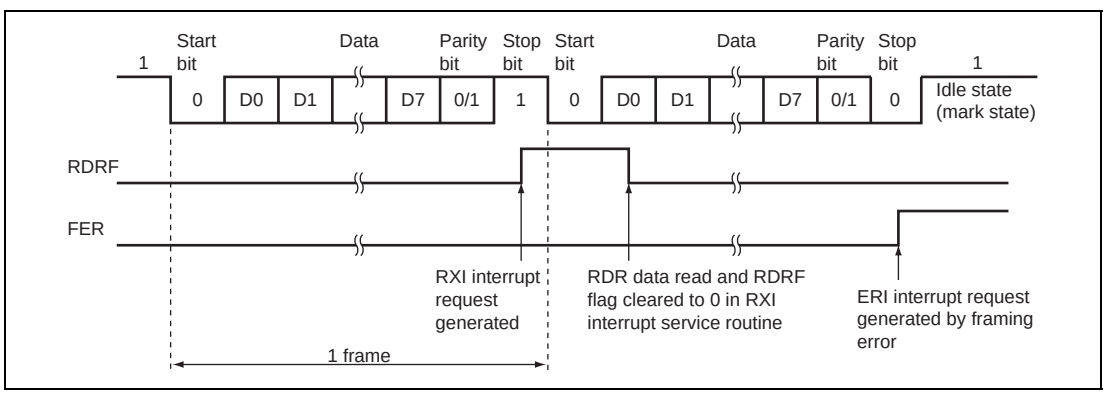


Figure 12.11 Example of SCI Operation in Reception (Example with 8-Bit Data, Parity, One Stop Bit)

Table 12.11 shows the states of the SSR status flags and receive data handling when a receive error is detected. If a receive error is detected, the RDRF flag retains its state before receiving data. Reception cannot be resumed while a receive error flag is set to 1. Accordingly, clear the ORER, FER, PER, and RDRF bits to 0 before resuming reception. Figure 12.12 shows a sample flow chart for serial data reception.

12.7.5 Receive Data Sampling Timing and Reception Margin

In Smart Card interface mode an internal clock generated by the on-chip baud rate generator can only be used as a transmission/reception clock. In this mode, the SCI operates on a basic clock with a frequency of 32, 64, 372, or 256 times the transfer rate (fixed to 16 times in normal asynchronous mode) as determined by bits BCP1 and BCP0. In reception, the SCI samples the falling edge of the start bit using the basic clock, and performs internal synchronization. As shown in figure 12.28, by sampling receive data at the rising-edge of the 16th, 32nd, 186th, or 128th pulse of the basic clock, data can be latched at the middle of the bit. The reception margin is given by the following formula.

$$M = \left| \left(0.5 - \frac{1}{2N}\right) - (L - 0.5)\,F - \frac{|\,D - 0.5\,|}{N}\,(1 + F) \right| \times 100\ [\%]$$

Where M: Reception margin (%)
N: Ratio of bit rate to clock (N = 32, 64, 372, and 256)
D: Clock duty (D = 0 to 1.0)
L: Frame length (L = 10)
F: Absolute value of clock frequency deviation

Assuming values of F = 0, D = 0.5 and N = 372 in the above formula, the reception margin formula is as follows.

$$M = (0.5 - 1/2 \times 372) \times 100\%$$
$$= 49.866\%$$

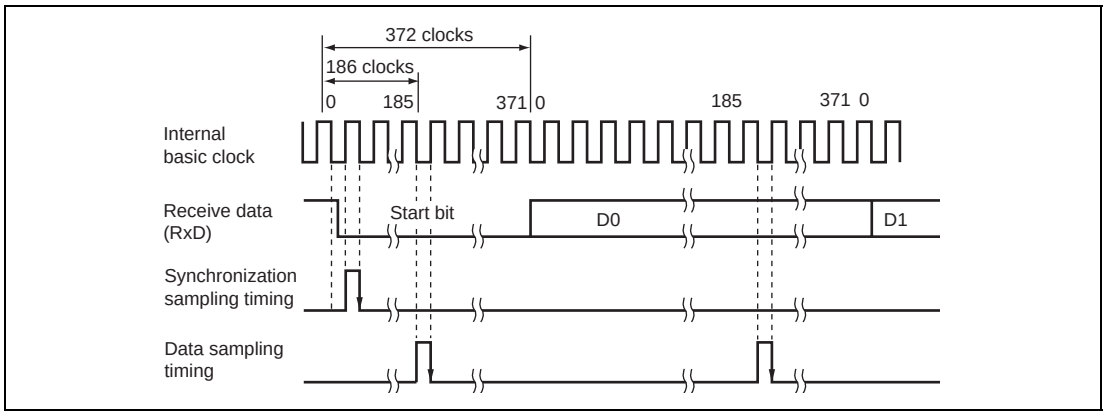


Figure 12.28 Receive Data Sampling Timing in Smart Card Mode (Using Clock of 372 Times the Transfer Rate)

12.7.7 Serial Data Transmission (Except for Block Transfer Mode)

As data transmission in Smart Card interface mode involves error signal sampling and retransmission processing, the operations are different from those in normal serial communication interface mode (except for block transfer mode). Figure 12.29 illustrates the retransfer operation when the SCI is in transmit mode.

1. If an error signal is sent back from the receiving end after transmission of one frame is complete, the ERS bit in SSR is set to 1. If the RIE bit in SCR is enabled at this time, an ERI interrupt request is generated. The ERS bit in SSR should be cleared to 0 by the time the next parity bit is sampled.
2. The TEND bit in SSR is not set for a frame in which an error signal indicating an abnormality is received. Data is retransferred from TDR to TSR, and retransmitted automatically.
3. If an error signal is not sent back from the receiving end, the ERS bit in SSR is not set. Transmission of one frame, including a retransfer, is judged to have been completed, and the TEND bit in SSR is set to 1. If the TIE bit in SCR is enabled at this time, a TXI interrupt request is generated. Writing transmit data to TDR transfers the next transmit data.

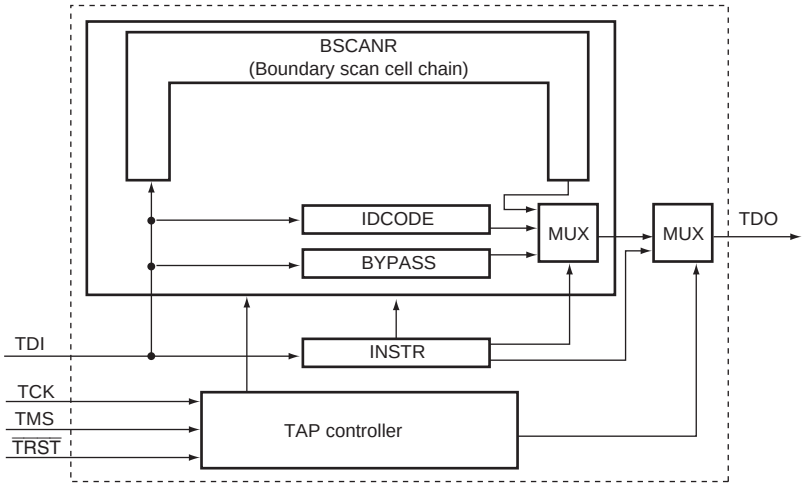
Figure 12.31 shows a flowchart for transmission. A sequence of transmit operations can be performed automatically by specifying the DMAC to be activated with a TXI interrupt source. In a transmit operation, the TDRE flag is set to 1 at the same time as the TEND flag in SSR is set, and a TXI interrupt will be generated if the TIE bit in SCR has been set to 1. If the TXI request is designated beforehand as a DMAC activation source, the DMAC will be activated by the TXI request, and transfer of the transmit data will be carried out. The TDRE and TEND flags are automatically cleared to 0 when data is transferred by the DMAC. In the event of an error, the SCI retransmits the same data automatically. During this period, the TEND flag remains cleared to 0 and the DMAC is not activated. Therefore, the SCI and DMAC will automatically transmit the specified number of bytes in the event of an error, including retransmission. However, the ERS flag is not cleared automatically when an error occurs, and so the RIE bit should be set to 1 beforehand so that an ERI request will be generated in the event of an error, and the ERS flag will be cleared. When using the DMAC for data transmission or reception, always make DMAC settings and enable the DMAC before making SCI settings. For details on DMAC settings, see section 7, DMA Controller (DMAC).

12.10.6 Operation in Case of Mode Transition

- Transmission

  Operation should be stopped (by clearing TE, TIE, and TEIE to 0) before making a module stop mode, software standby mode, watch mode, subactive mode, or subsleep mode transition. TSR, TDR, and SSR are reset. The output pin states in module stop mode, software standby mode, watch mode, subactive mode, or subsleep mode depend on the port settings, and becomes high-level output after the relevant mode is cleared. If a transition is made during transmission, the data being transmitted will be undefined. When transmitting without changing the transmit mode after the relevant mode is cleared, transmission can be started by setting TE to 1 again, and performing the following sequence:

  SSR read -> TDR write -> TDRE clearance. To transmit with a different transmit mode after clearing the relevant mode, the procedure must be started again from initialization. Figure 12.39 shows a sample flowchart for mode transition during transmission. Port pin states are shown in figures 12.40 and 12.41.



Legend:
BSCANR: Boundary scan register
IDCODE: IDCODE register
BYPASS: BYPASS register
INSTR: Instruction register
TAP: Test access port

Figure 13.1 Block Diagram of Boundary Scan Function

5. If a pin with pull-up function is SAMPLEed with pull-up function enabled, the corresponding IN register is set to 1. In this case, the corresponding Control register must be cleared to 0.
6. If a pin with open-drain function is SAMPLEed while its open-drain function is enabled and while the corresponding OUT register is set to 1, the corresponding Control register is cleared to 0 (the pin status is Hi-Z). If the pin is SAMPLEed while the corresponding OUT register is cleared to 0, the corresponding Control register is set to 1 (the pin status is 0).
7. If EXTEST, CLAMP, or HIGHZ state is entered, this LSI enters guarded mode such as hardware standby mode ($\overline{RES}$ = $\overline{STBY}$ = 0). Before entering normal operating mode from EXTEST, CLAMP, or HIGHZ state, specify $\overline{RES}$, $\overline{STBY}$, FWE, and MD2 to MD0 pin to the designated mode.
8. The EMLE pin must be cleared to 0. When the pin is set to 1, this chip functions as High-performance user debugging interface (H-UDI).

EMLE Pin	Chip State
0	Normal operation, boundary scan function
1	High-performance user debugging interface (H-UDI)

14.6 DMA Transfer Specifications

Two methods of USB request and auto request are available for the DMA transfer of USB data.

14.6.1 DMAC Transfer by USB Request

(1) Overview

Only normal mode in full address mode (cycle steal mode) supports the transfer by a USB request of the on-chip DMAC. Endpoints that can be transferred by the on-chip DMAC are EP1 and EP2 in Bulk transfer (corresponding registers are UEDR1 and UEDR2). In DMA transfer, the USB module must be accessed as an external device in area 6. The USB module cannot be accessed as a device with external ACK (single-address transfer cannot be performed). 0-byte data transfer to EP2 is ignored even if the DMA transfer is enabled by setting the EP2T1 bit in UDMAR to 1.

(2) On-Chip DMAC Settings

The on-chip DMAC must be specified as follows: A USB request ($\overline{\text{DREQ}}$ signal is used), activated by low-level input, byte size, full-address mode transfer, and the DTA bit in DMABCR = 1. After completing the DMA transfer of specified times, the DMAC automatically stops. Note, however, that the USB module keeps the $\overline{\text{DREQ}}$ signal low while data to be transferred by the on-chip DMAC remains regardless of the DMAC status.

(3) EP1 DMA Transfer

The EP1T1 bit in UDMAR enables the DMA transfer. The EP1T0 bit in UDMAR specifies the $\overline{\text{DREQ}}$ signal to be used by the DMA transfer. When 1 is written to the EP1T1 bit, the $\overline{\text{DREQ}}$ signal is driven low if at least one of EP1 data FIFOs is empty; the $\overline{\text{DREQ}}$ signal is driven high if both EP1 data FIFOs are full.

(a) EP1PKTE in UTRG0

When DMA transfer is performed on EP1 transmit data, the USB module automatically performs the same processing as writing 1 to EP1PKTE if one data FIFO (64 bytes) becomes full. Accordingly, to transfer data of integral multiples of 64 bytes, the user needs not to write 1 to EP1PKTE. To transfer data of less than 64 bytes, the user must write 1 to EP1PKTE using the DMA transfer end interrupt of the on-chip DMAC. If the user writes 1 to EP1PKTE in cases other than the case when data of less than 64 bytes is transferred, excess transfer occurs and correct operation cannot be guaranteed.

Figure 14.22 shows an example for transmitting 150 bytes of data from EP1 to the host. In this case, internal processing as the same as writing 1 to EP1PKTE is automatically performed twice. This kind of internal processing is performed when the currently selected data FIFO becomes full.

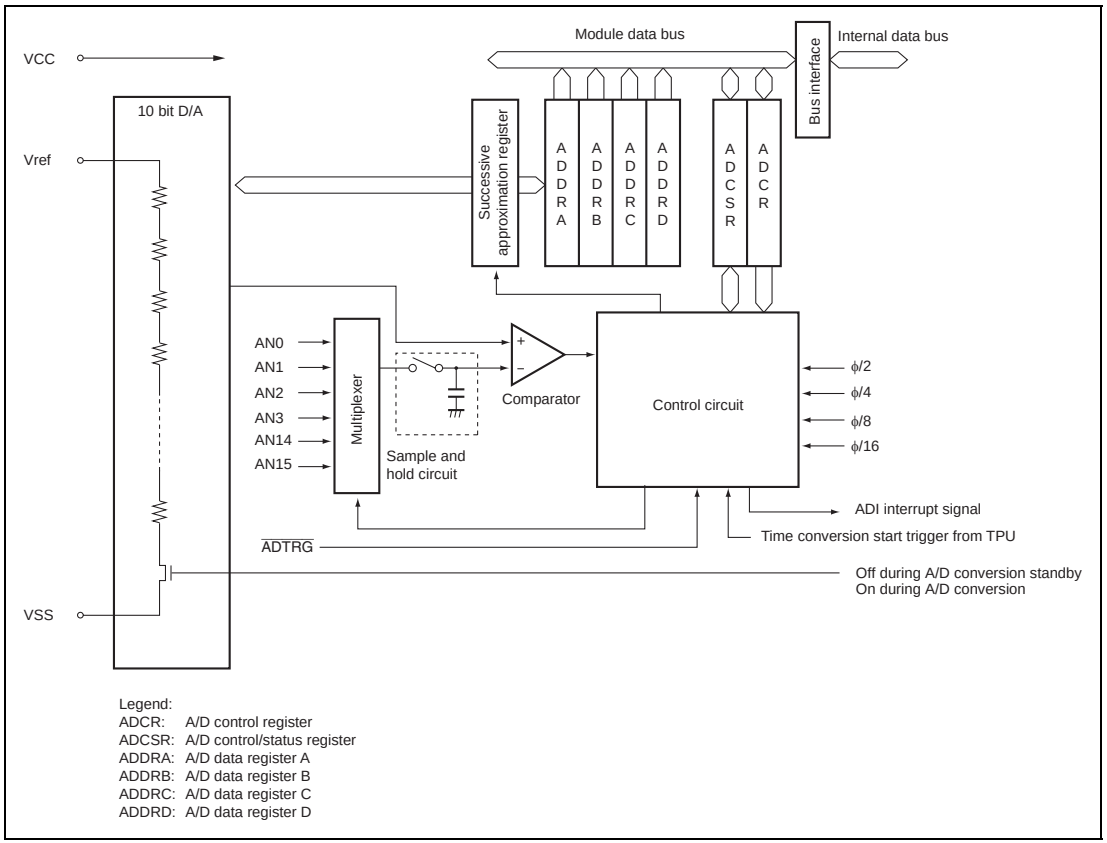


Figure 15.1 Block Diagram of A/D Converter

17.4 Input/Output Pins

The flash memory is controlled by means of the pins shown in table 17.2.

Table 17.2 Pin Configuration

Pin Name	I/O	Function	
$\overline{\text{RES}}$	Input	Reset	All
FWE	Input	Flash program/erase protection by hardware	
MD2, MD1, MD0	Input	Sets this LSI's operating mode	
PF3, PF0, P16, P14	Input	Sets this LSI's operating mode in programmer mode	
EMLE	Input	Emulator enable	
TxD2	Output	Serial transmit data output	HD64F2218, HD64F2212, HD64F2211
RxD2	Input	Serial receive data input	
USD+, USD−	Input/output	USB data input/output	HD64F2218U, HD64F2218CU, HD64F2217CU, HD64F2212U, HD64F2212CU, HD64F2211U
VBUS	Input	USB cable connect/cut detect	
$\overline{\text{UBPM}}$	Input	USB bus power mode/self power mode select	
USPND	Output	USB suspend output	
P36 (PUPD+)	Output	D+ pull-up control	

17.5 Register Descriptions

The flash memory has the following registers. For details on register addresses and register states during each processing, refer to section 21, List of Registers.

- Flash memory control register 1 (FLMCR1)
- Flash memory control register 2 (FLMCR2)
- Erase block register 1 (EBR1)
- Erase block register 2 (EBR2)
- RAM emulation register (RAMER)
- Serial control register X (SCRX)

The masked ROM version is not equipped with the above registers. Attempting to read them with produce an undetermined value, and writing to them is invalid.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
UISR1	—	—	—	—	—	EP2 READYS	EP1TRS	EP1 EMPTYS	USB
UISR3	CK48 READYS	SOFS	SETCS	—	—	—	—	VBUSiS	
UDSR	—	—	—	—	—	EP1DE	EP3DE	EP0iDE	
UCVR	—	—	CNFV0	—	—	—	—	—	
UTSTR0	PTSTE	—	—	—	SUSPEND	$\overline{OE}$	FSE0	VPO	
UTSTR1	VBUS	$\overline{UBPM}$	—	—	—	RCV	VP	VM	
UTSTR2	—	—	—	—	—	—	—	—	
UTSTRB	—	—	—	—	—	—	—	—	
UTSTRC	—	—	—	—	—	—	—	—	
UTSTRD	—	—	—	—	—	—	—	—	
UTSTRE	—	—	—	—	—	—	—	—	
UTSTRF	—	—	—	—	—	—	—	—	
SCRX	—	—	—	—	FLSHE	—	—	—	FLASH
SBYCR	SSBY	STS2	STS1	STS0	OPE	—	—	—	SYSTEM
SYSCR	—	—	INTM1	INTM0	NMIEG	MRESE	—	RAME	
SCKCR	PSTOP	—	—	—	—	SCK2	SCK1	SCK0	
MDCR	—	—	—	—	FWE	MDS2	MDS1	MDS0	
MSTPCRA	MSTPA7	MSTPA6	MSTPA5	MSTPA4	MSTPA3	MSTPA2	MSTPA1	MSTPA0	
MSTPCRB	MSTPB7	MSTPB6	MSTPB5	MSTPB4	MSTPB3	MSTPB2	MSTPB1	MSTPB0	
MSTPCRC	MSTPC7	MSTPC6	MSTPC5	MSTPC4	MSTPC3	MSTPC2	MSTPC1	MSTPC0	
PFCR	—	—	—	—	AE3	AE2	AE1	AE0	BSC
LPWRCR	DTON	LSON	NESEL	SUBSTP	RFCUT	—	STC1	STC0	SYSTEM
OUTCR	—	—	—	—	—	PF7OUT2	PF7OUT1	PF7OUT0	PORT
SEMRA_0	SSE	TCS2	TCS1	TCS0	ABCS	ACS2	ACS1	ACS0	SCI_0
SEMRB_0	ACS3	—	—	—	TIOCA2E	TIOCA1E	TIOCC0E	TIOCA0E	
ISCRH	IRQ7SCB	IRQ7SCA	IRQ6SCB	IRQ6SCA	IRQ5SCB	IRQ5SCA	IRQ4SCB	IRQ4SCA	INT
ISCRL	IRQ3SCB	IRQ3SCA	IRQ2SCB	IRQ2SCA	IRQ1SCB	IRQ1SCA	IRQ0SCB	IRQ0SCA	
IER	IRQ7E	IRQ6E	IRQ5E	IRQ4E	IRQ3E	IRQ2E	IRQ1E	IRQ0E	
ISR	IRQ7F	IRQ6F	IRQ5F	IRQ4F	IRQ3F	IRQ2F	IRQ1F	IRQ0F	

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Current dissipation*[1]	Normal operation (USB operates)	I_{CC}*[2]	—	30 V_{CC} = 3.3 V	45 V_{CC} = 3.6 V	mA	f = 16 MHz, When PLL3 is used
			—	41 V_{CC} = 3.3 V	60 V_{CC} = 3.6 V	mA	f = 24 MHz, When PLL2 is used
	Sleep mode		—	16 V_{CC} = 3.3 V	30 V_{CC} = 3.6 V	mA	f = 16 MHz, When USB and PLL are halted
			—	22 V_{CC} = 3.3 V	45 V_{CC} = 3.6 V	mA	f = 24 MHz, When USB and PLL are halted
	All modules other than flash memory stopped		—	16 V_{CC} = 3.3 V	—	mA	f = 16 MHz (reference value)
			—	24 V_{CC} = 3.3 V	—	mA	f = 24 MHz (reference value)
	Subactive mode		—	45	180	µA	Vcc = 3.3 V, EMLE = 0 When crystal resonator (32.768 kHz) is used
			—	30*[5]	—		
	Subsleep mode		—	35	100	µA	
			—	20*[5]	—		
	Watch mode		—	5	40	µA	
	Standby mode*[3]		—	1.0	10	µA	$T_a \leq 50°C$ 32.768 kHz RTC halted EMLE = 0
			—	—	50	µA	$50°C < T_a$ 32.768 kHz RTC halted EMLE = 0
Reference power supply current	During A/D conversion	AI_{CC}	—	1.3	2.5	mA	V_{ref} = 3.3 V
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: If the A/D converter is not used, the Vref pin should not be open. Even if the A/D converter is not used, connect the Vref pin to Vcc.