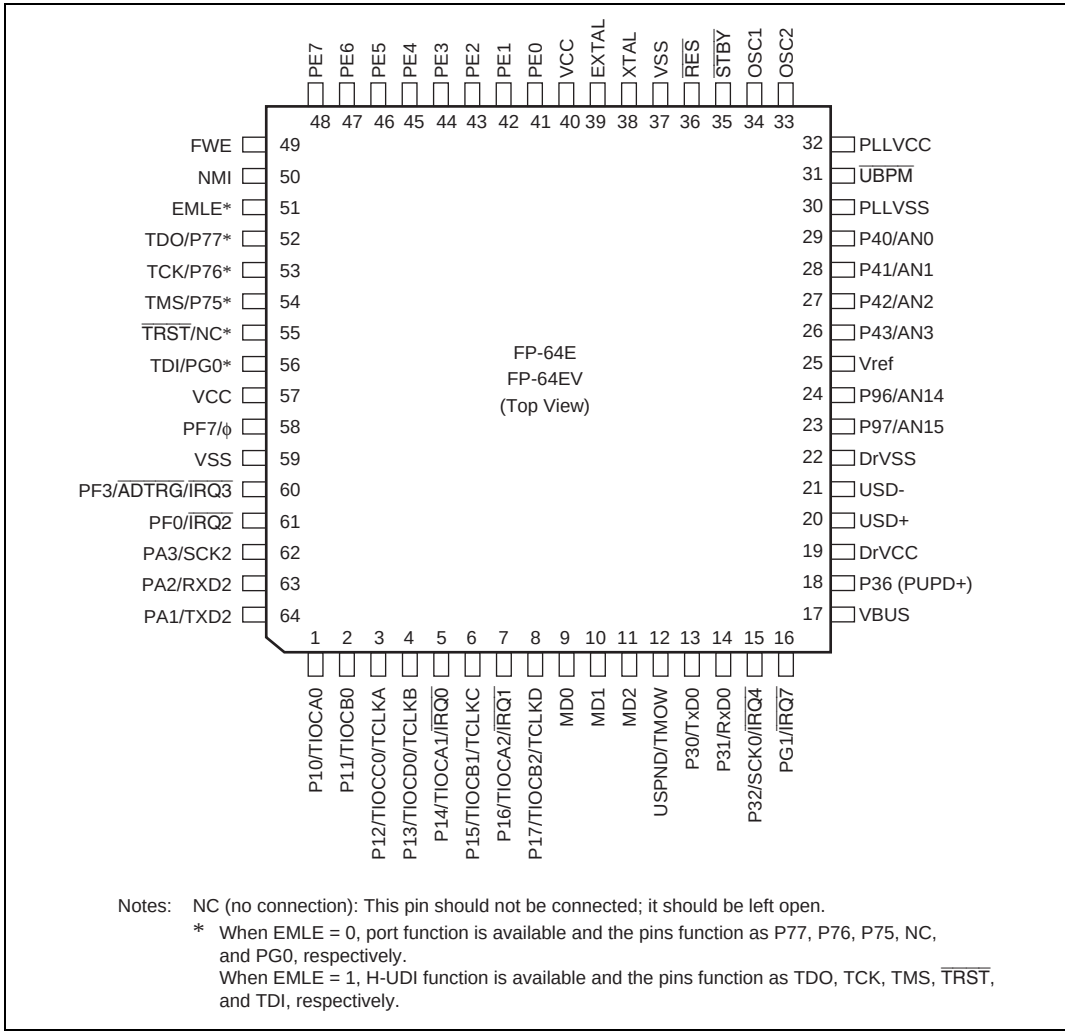
Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	24MHz
Connectivity	SCI, SmartCard, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	69
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2218ubr24v



Notes: NC (no connection): This pin should not be connected; it should be left open.

* When EMLE = 0, port function is available and the pins function as P77, P76, P75, NC, and PG0, respectively.
When EMLE = 1, H-UDI function is available and the pins function as TDO, TCK, TMS, $\overline{\text{TRST}}$, and TDI, respectively.

Figure 1.9 Pin Arrangements of HD64F2212, HD64F2212U, HD64F2212CU, HD64F2211, HD64F2211U, HD64F2211CU and HD64F2210CU (FP-64E, FP-64EV)

5.3.1 Interrupt Priority Registers A to G, J, K, M (IPRA to IPRG, IPRJ, IPRK, IPRM)

The IPR registers set priorities (levels 7 to 0) for interrupts other than NMI.

The correspondence between interrupt sources and IPR settings is shown in section 5.5, Interrupt Exception Handling Vector Table. Setting a value in the range from H'0 to H'7 in the 3-bit groups of bits 6 to 4 and 2 to 0 sets the priority of the corresponding interrupt.

Bit	Bit Name	Initial Value	R/W	Description
7	–	0	–	Reserved This bit is always read as 0 and cannot be modified.
6	IPR6	1	R/W	These bits set the priority of the corresponding interrupt source. 000: Priority level 0 (Lowest) 001: Priority level 1 010: Priority level 2 011: Priority level 3 100: Priority level 4 101: Priority level 5 110: Priority level 6 111: Priority level 7 (Highest)
5	IPR5	1	R/W	
4	IPR4	1	R/W	
3	–	0	–	Reserved This bit is always read as 0 and cannot be modified.
2	IPR2	1	R/W	These bits set the priority of the corresponding interrupt source. 000: Priority level 0 (Lowest) 001: Priority level 1 010: Priority level 2 011: Priority level 3 100: Priority level 4 101: Priority level 5 110: Priority level 6 111: Priority level 7 (Highest)
1	IPR1	1	R/W	
0	IPR0	1	R/W	

5.3.3 IRQ Sense Control Registers H and L (ISCRH, ISCRL)

The ISCR registers select the source that generates an interrupt request at pins $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$.

Bit	Bit Name	Initial Value	R/W	Description
15	IRQ7SCB	0	R/W	IRQ7 Sense Control B
14	IRQ7SCA	0	R/W	IRQ7 Sense Control A 00: Interrupt request generated at $\overline{\text{IRQ7}}$ input low level 01: Interrupt request generated at falling edge of $\overline{\text{IRQ7}}$ input 10: Interrupt request generated rising edge of $\overline{\text{IRQ7}}$ input 11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ7}}$ input
13	IRQ6SCB	0	R/W	IRQ6*[1] Sense Control B
12	IRQ6SCA	0	R/W	IRQ6*[1] Sense Control A 00: Setting prohibited when using on-chip USB suspend or resume interrupt 01: Interrupt request generated at falling edge of $\overline{\text{IRQ6}}$ input 1x: Setting prohibited
11	IRQ5SCB	0	R/W	IRQ5*[2] Sense Control B
10	IRQ5SCA	0	R/W	IRQ5*[2] Sense Control A 00: Setting prohibited when using RTC interrupt 01: Interrupt request generated at falling edge of $\overline{\text{IRQ5}}$ input 1x: Setting prohibited
9	IRQ4SCB	0	R/W	IRQ4 Sense Control B
8	IRQ4SCA	0	R/W	IRQ4 Sense Control A 00: Interrupt request generated at $\overline{\text{IRQ4}}$ input low level 01: Interrupt request generated at falling edge of $\overline{\text{IRQ4}}$ input 10: Interrupt request generated at rising edge of $\overline{\text{IRQ4}}$ input 11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ4}}$ input

6.3.6 Pin Function Control Register (PFCR)

PFCR performs address output control in external extended mode. When using the USB with the emulator (E6000), enable the A8 and A9 output by setting AE3 to AE0 to 0010.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	Undefined	R/W	Reserved The write value should always be 0.
3	AE3	1/0*	R/W	Address Output Enable 3 to 0 These bits select enabling or disabling of address outputs A8 to A23 in ROMless extended mode and modes with ROM. When a pin is enabled for address output, the address is output regardless of the corresponding DDR setting. When a pin is disabled for address output, it becomes an output port when the corresponding DDR bit is set to 1. 0000: A8 to A23 output disabled (initial value of mode 6 and 7) 0001: A8 output enabled; A9 to A23 output disabled 0010: A8, A9 output enabled; A10 to A23 output disabled 0011: A8 to A10 output enabled; A11 to A23 output disabled 0100: A8 to A11 output enabled; A12 to A23 output disabled 0101: A8 to A12 output enabled; A13 to A23 output disabled 0110: A8 to A13 output enabled; A14 to A23 output disabled 0111: A8 to A14 output enabled; A15 to A23 output disabled 1000: A8 to A15 output enabled; A16 to A23 output disabled 1001: A8 to A16 output enabled; A17 to A23 output disabled 1010: A8 to A17 output enabled; A18 to A23 output disabled 1011: A8 to A18 output enabled; A19 to A23 output disabled 1100: A8 to A19 output enabled; A20 to A23 output disabled 1101: A8 to A20 output enabled; A21 to A23 output disabled (initial value of modes 4 and 5) 1110: A8 to A21 output enabled; A22, A23 output disabled 1111: A8 to A23 output enabled
2	AE2	1/0*	R/W	
1	AE1	0	R/W	
0	AE0	1/0*	R/W	

Note: * In modes 4 and 5, initial value of each bit is 1. In modes 6 and 7, initial value of each bit is 0.

8-Bit 3-State Access Space (Except Area 6): Figure 6.11 shows the bus timing for an 8-bit 3-state access space in the H8S/2218 Group. When an 8-bit access space is accessed, the upper half (D15 to D8) of the data bus is used.

Wait states can be inserted.

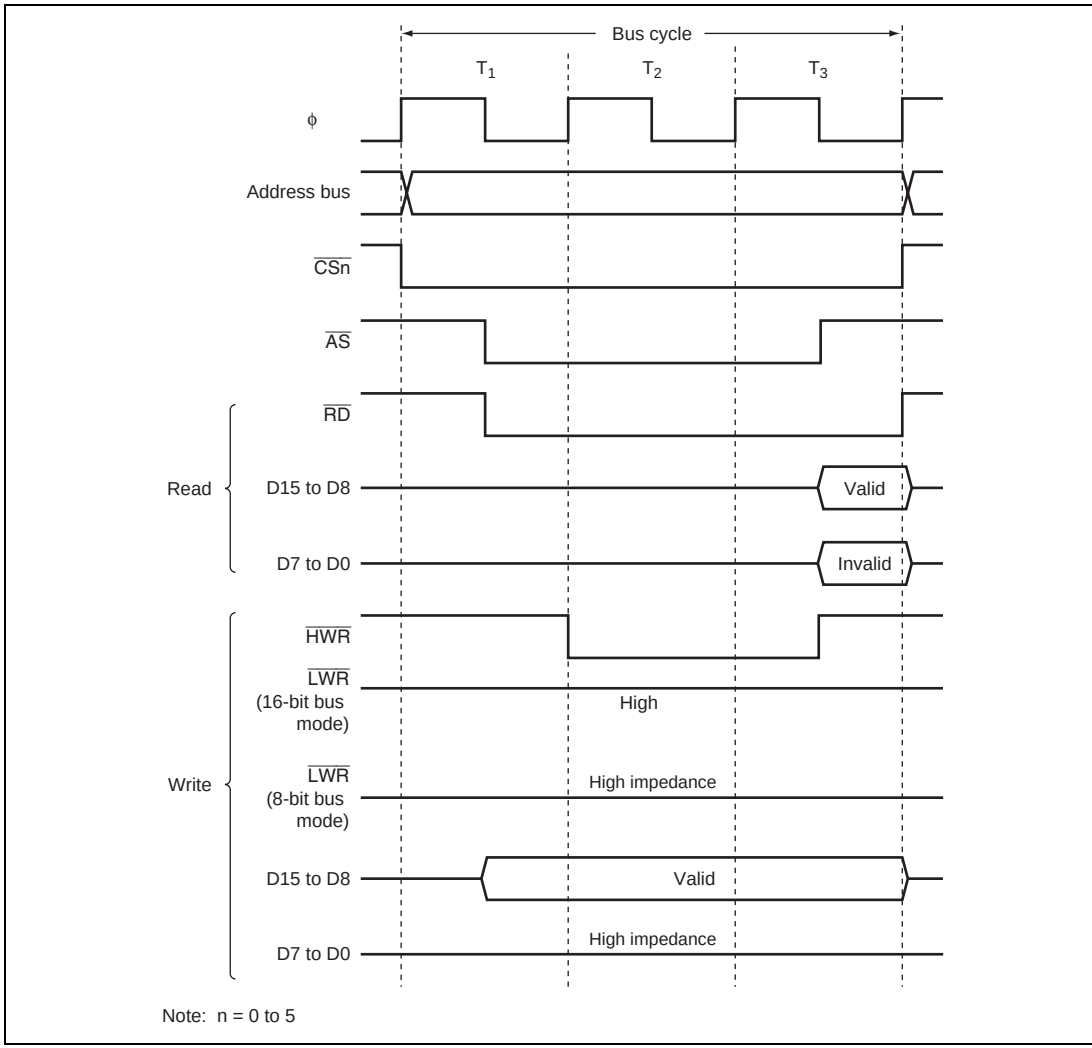


Figure 6.11 Bus Timing for 8-Bit 3-State Access Space (Except Area 6)

7.3 Register Descriptions

7.3.1 Memory Address Registers (MAR)

- Short Address Mode

  MAR is a 32-bit readable/writable register that specifies the transfer source address or destination address. The upper 8 bits of MAR are reserved: they are always read as 0, and cannot be modified. Whether MAR functions as the source address register or as the destination address register can be selected by means of the DTDIR bit in DMACR.

  MAR is incremented or decremented each time a byte or word transfer is executed, so that the address specified by MAR is constantly updated. For details, see section 7.3.4, DMA Control Register (DMACR). MAR is not initialized by a reset or in standby mode.

- Full Address Mode

  MAR is a 32-bit readable/writable register; MARA functions as the transfer source address register, and MARB as the destination address register.

  MAR is composed of two 16-bit registers, MARH and MARL. The upper 8 bits of MARH are reserved: they are always read as 0, and cannot be modified. MAR is incremented or decremented each time a byte or word transfer is executed, so that the source or destination memory address can be updated automatically. For details, see section 7.3.4, DMA Control Register (DMACR). MAR is not initialized by a reset or in standby mode.

7.3.2 I/O Address Register (IOAR)

- Short Address Mode

  IOAR is a 16-bit readable/writable register that specifies the lower 16 bits of the transfer source address or destination address. The upper 8 bits of the transfer address are automatically set to H'FF. Whether IOAR functions as the source address register or as the destination address register can be selected by means of the DTDIR bit in DMACR.

  IOAR is not incremented or decremented each time a transfer is executed, so that the address specified by IOAR is fixed. IOAR is not initialized by a reset or in standby mode.

- Full Address Mode:

  IOAR is not used in full address mode transfer.

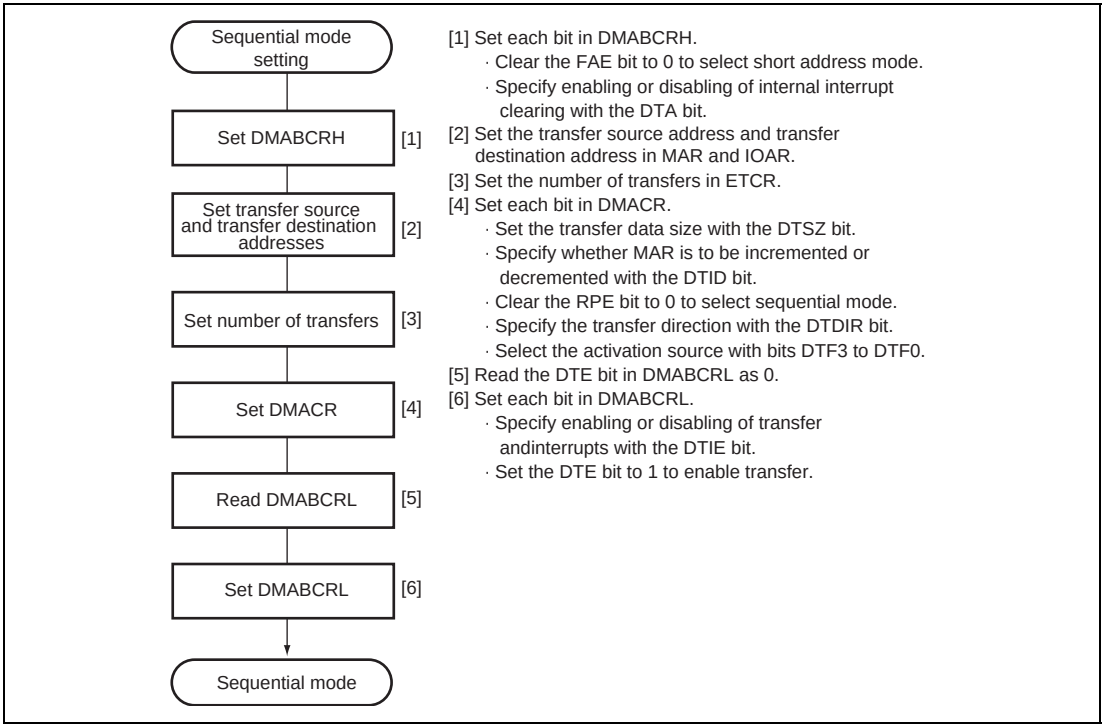


Figure 7.3 Example of Sequential Mode Setting Procedure

Full Address Mode (Cycle Steal Mode): Figure 7.16 shows a transfer example in which $\overline{\text{TEND}}$* output is enabled and word-size full address mode transfer (cycle steal mode) is performed from external 16-bit, 2-state access space to external 16-bit, 2-state access space.

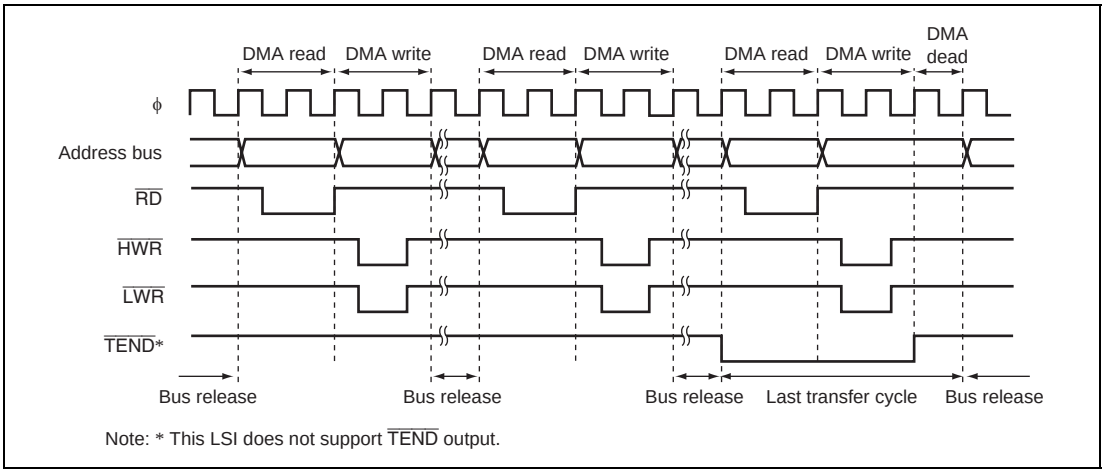


Figure 7.16 Example of Full Address Mode (Cycle Steal) Transfer

A one-byte or one-word transfer is performed, and after the transfer the bus is released. While the bus is released one bus cycle is inserted by the CPU.

In the transfer end cycle (the cycle in which the transfer counter reaches 0), a one-state DMA dead cycle is inserted after the DMA write cycle.

Note: * This LSI does not support $\overline{\text{TEND}}$ output.

8.1 Port 1

In the H8S/2218 Group, the port 1 is an 8-bit I/O port also functioning as address bus pins, TPU I/O pins, and external interrupt input pins. In the H8S/2212 Group, the port 1 is an 8-bit I/O port also functioning as TPU I/O pins and external interrupt input pins. The port 1 has the following registers.

- Port 1 data direction register (P1DDR)
- Port 1 data register (P1DR)
- Port 1 register (PORT1)

8.1.1 Port 1 Data Direction Register (P1DDR)

P1DDR specifies input or output for the pins of the port 1.

Since P1DDR is a write-only register, the bit manipulation instructions must not be used to write P1DDR. For details, see section 2.9.4, Accessing Registers Containing Write-Only Bits.

Bit	Bit Name	Initial Value	R/W	Description
7	P17DDR	0	W	(H8S/2218 Group)
6	P16DDR	0	W	Modes 4 to 6: If address output is enabled by the setting of bits AE3 to AE0 in PFCR, pins P13 to P10 are address outputs. Pins P17 to P14, and pins P13 to P10 when address output is disabled, are output ports when the corresponding P1DDR bits are set to 1, and input ports when the corresponding P1DDR bits are cleared to 0. Mode 7: Setting a P1DDR bit to 1 makes the corresponding port 1 pin an output port, while clearing the bit to 0 makes the pin an input port. (H8S/2212 Group) Setting a P1DDR bit to 1 makes the corresponding port 1 pin an output port, while clearing the bit to 0 makes the pin an input port.
5	P15DDR	0	W	
4	P14DDR	0	W	
3	P13DDR	0	W	
2	P12DDR	0	W	
1	P11DDR	0	W	
0	P10DDR	0	W	

Bit	Bit Name	Initial Value	R/W	Description
1	P71DDR	0	W	(H8S/2218 Group)
0	P70DDR	0	W	Setting a P7DDR bit to 1 makes the corresponding port 7 pin an output pin, while clearing the bit to 0 makes the pin an input pin. (H8S/2212 Group) Reserved These bits are undefined and cannot be modified.

8.4.2 Port 7 Data Register (P7DR)

P7DR stores output data for the port 7 pins.

Bit	Bit Name	Initial Value	R/W	Description
7	P77DR	0	R/W	(H8S/2218 Group)
6	P76DR	0	R/W	Reserved These bits are undefined and cannot be modified.
5	P75DR	0	R/W	(H8S/2212 Group) Store output data for the port 7 pins.
4	P74DR	0	R/W	(H8S/2218 Group) Stores output data for the port 7 pins. (H8S/2212 Group) Reserved This bit is undefined and cannot be modified.
3, 2	—	Undefined	—	Reserved These bits are undefined and cannot be modified.
1	P71DR	0	R/W	(H8S/2218 Group)
0	P70DR	0	R/W	Store output data for the port 7 pins. (H8S/2212 Group) Reserved These bits are undefined and cannot be modified.

8.7.5 Pin Functions

Port B pins also function as address bus (A15 to A9) output pins. The correspondence between the register specification and the pin functions is shown below.

Note: When using the USB with the emulator (E6000), set A9 and A8 as address bus output pins.

Table 8.37 PB7 Pin Function

Operating mode	Modes 4 to 6			Mode 7	
AE3 to AE0	B'1×××	Other than B'1×××		—	
PB7DDR	—	0	1	0	1
Pin Function	A15 output pin	PB7 input pin	PB7 output pin	PB7 input pin	PB7 output pin

Table 8.38 PB6 Pin Function

Operating mode	Modes 4 to 6			Mode 7	
AE3 to AE0	B'0111 or B'1×××	Other than B'0111 or B'1×××		—	
PB6DDR	—	0	1	0	1
Pin Function	A14 output pin	PB6 input pin	PB6 output pin	PB6 input pin	PB6 output pin

Table 8.39 PB5 Pin Function

Operating mode	Modes 4 to 6			Mode 7	
AE3 to AE0	B'011× or B'1×××	Other than B'011× or B'1×××		—	
PB5DDR	—	0	1	0	1
Pin Function	A13 output pin	PB5 input pin	PB5 output pin	PB5 input pin	PB5 output pin

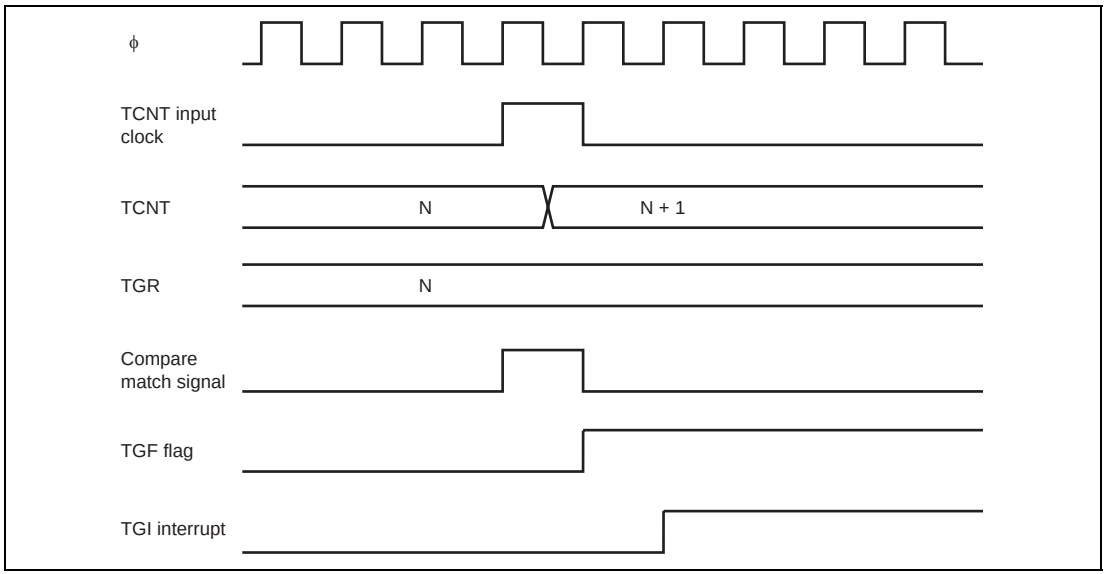


Figure 9.38 TGI Interrupt Timing (Compare Match)

TGF Flag Setting Timing in Case of Input Capture: Figure 9.39 shows the timing for setting of the TGF flag in TSR by input capture occurrence, and TGI interrupt request signal timing.

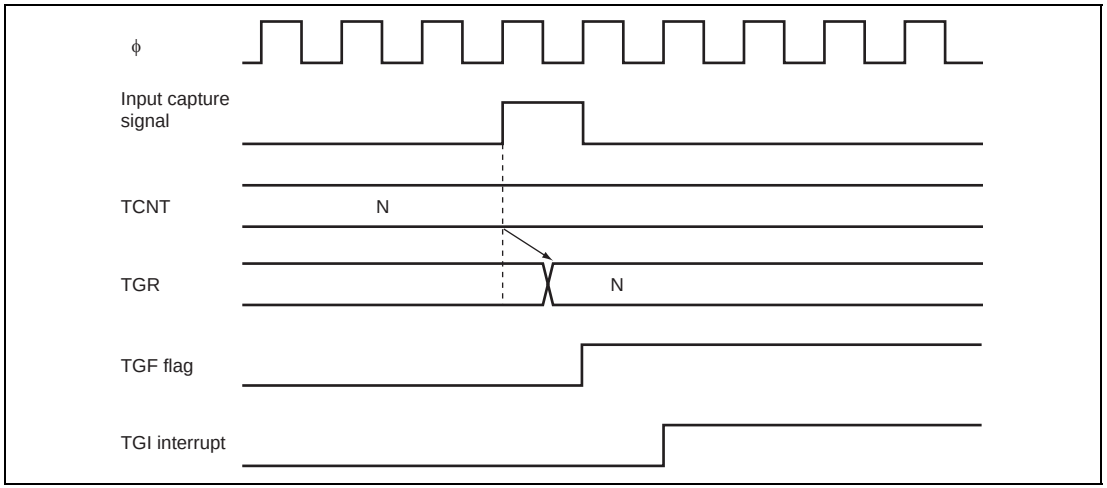


Figure 9.39 TGI Interrupt Timing (Input Capture)

11.3.8 Extended Module Stop Register (EXMDLSTP)

EXMDLSTP controls the clock supply of the RTC and USB.

Note: When reading pin states using the port D register (PORTD), after accessing EXMDLSTP (address range: H'FFFF40 to H'FFFF5F), you must perform a dummy read to the external address space (such as H'FFEF00 to H'FF7FF) outside the range H'FFFF40 to H'FFFF5F before reading PORTD.

Bit	Bit Name	Initial Value	R/W	Module
7 to 2	—	Undefined	—	Reserved These bits are always read as undefined values. These bits should not to be modified.
1	RTCSTOP	0	R/W	RTC Module Stop 0: RTC module stop cancelled 1: RTC module stop
0	USBSTOP1	0	R/W	USB Module Stop 0: USB module stop partly cancelled 1: USB module completely stop

12.10.7 Switching from SCK Pin Function to Port Pin Function:

When switching the SCK pin function to the output port function (high-level output) by making the following settings while DDR = 1, DR = 1, C/$\overline{A}$ = 1, CKE1 = 0, CKE0 = 0, and TE = 1 (synchronous mode), low-level output occurs for one half-cycle.

1. End of serial data transmission
2. TE bit = 0
3. C/$\overline{A}$ bit = 0 ... switchover to port output
4. Occurrence of low-level output (see figure 12.43)

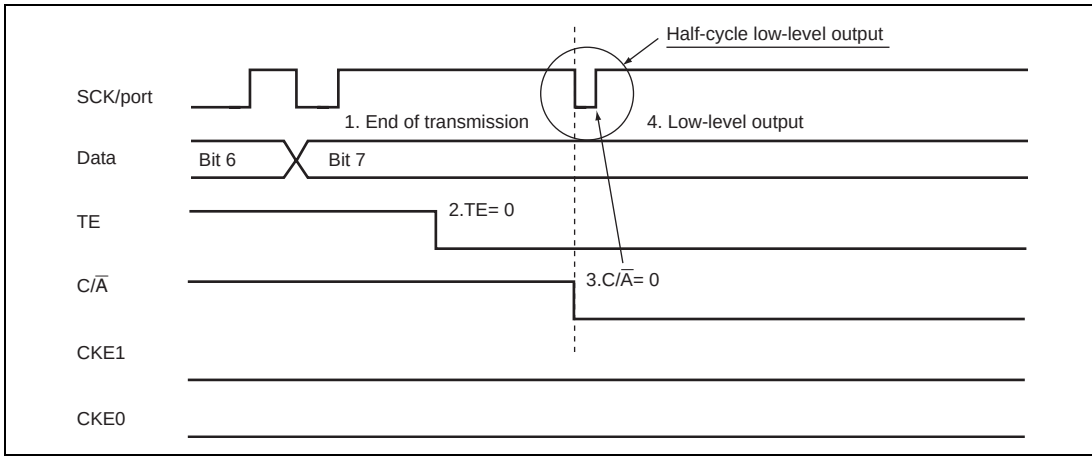


Figure 12.43 Operation when Switching from SCK Pin Function to Port Pin Function

- USB interrupt flag register 0 (UIFR0)
- USB interrupt flag register 1 (UIFR1)
- USB interrupt flag register 3 (UIFR3)
- USB interrupt enable register 0 (UIER0)
- USB interrupt enable register 1 (UIER1)
- USB interrupt enable register 3 (UIER3)
- USB interrupt select register 0 (UISR0)
- USB interrupt select register 1 (UISR1)
- USB interrupt select register 3 (UISR3)
- USB data status register (UDSR)
- USB Configuration value register (UCVR)
- USB test register 0 (UTSTR0)
- USB test register 1 (UTSTR1)
- USB test registers 2 and A to F (UTSTR2, UTSTRA to UTSTRF)
- Module stop control register B (MSTPCRB)
- Extended module stop register (EXMDLSTP)

14.3.1 USB Control Register (UCTLR)

UCTLR is used to select the USB operation clock and control the USB module internal reset. UCTLR can be read from or written to even when the USB module stop 2 bit (MSTPB0) in MSTPCRB is 1. For details on UCTLR setting procedure, refer to section 14.5, Communication Operation.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R/W	Reserved The write value should always be 0.
6	TMOWE	0	R/W	TMOW Pin Enable 0: The USPND/TMOW pin outputs USPND of USB. 1: The USPND/TMOW pin outputs TMOW of RTC.

17.4 Input/Output Pins

The flash memory is controlled by means of the pins shown in table 17.2.

Table 17.2 Pin Configuration

Pin Name	I/O	Function	
$\overline{\text{RES}}$	Input	Reset	All
FWE	Input	Flash program/erase protection by hardware	
MD2, MD1, MD0	Input	Sets this LSI's operating mode	
PF3, PF0, P16, P14	Input	Sets this LSI's operating mode in programmer mode	
EMLE	Input	Emulator enable	
TxD2	Output	Serial transmit data output	HD64F2218, HD64F2212, HD64F2211
RxD2	Input	Serial receive data input	
USD+, USD−	Input/output	USB data input/output	HD64F2218U, HD64F2218CU, HD64F2217CU, HD64F2212U, HD64F2212CU, HD64F2211U
VBUS	Input	USB cable connect/cut detect	
$\overline{\text{UBPM}}$	Input	USB bus power mode/self power mode select	
USPND	Output	USB suspend output	
P36 (PUPD+)	Output	D+ pull-up control	

17.5 Register Descriptions

The flash memory has the following registers. For details on register addresses and register states during each processing, refer to section 21, List of Registers.

- Flash memory control register 1 (FLMCR1)
- Flash memory control register 2 (FLMCR2)
- Erase block register 1 (EBR1)
- Erase block register 2 (EBR2)
- RAM emulation register (RAMER)
- Serial control register X (SCRX)

The masked ROM version is not equipped with the above registers. Attempting to read them with produce an undetermined value, and writing to them is invalid.

Table 20.2 Transition Conditions of Power-Down Modes

Pre-Transition State	Status of Control Bit at Transition				State after Transition Invoked by SLEEP Command	State after Transition Back from Power-Down Mode Invoked by Interrupt
	SSBY	PSS	LSON	DTON		
High-speed/ Medium-speed	0	×	0	×	Sleep	High-speed/Medium-speed
	0	×	1	×	—	—
	1	0	0	×	Software standby	High-speed/Medium-speed
	1	0	1	×	—	—
	1	1	0	0	Watch	High-speed
	1	1	1	0	Watch	Subactive
	1	1	0	1	—	—
	1	1	1	1	Subactive	—
Subactive	0	0	×	×	—	—
	0	1	0	×	—	—
	0	1	1	×	Sub sleep	Subactive
	1	0	×	×	—	—
	1	1	0	0	Watch	High-speed
	1	1	1	0	Watch	Subactive
	1	1	0	1	High-speed	—
	1	1	1	1	—	—

Legend:

×: Don’t care

—: Do not set

Item	Symbol	Condition A Min.	Condition A Max.	Condition B Min.	Condition B Max.	Condition C, D Min.	Condition C, D Max.	Unit	Test Conditions
Read data access time 3	t_{ACC3}	—	$2.0 \times t_{cyc} - 90$	—	$2.0 \times t_{cyc} - 65$	—	$2.0 \times t_{cyc} - 40$	ns	Figures 22.7, 22.10
Read data access time 4	t_{ACC4}	—	$2.5 \times t_{cyc} - 90$	—	$2.5 \times t_{cyc} - 65$	—	$2.5 \times t_{cyc} - 35$	ns	Figure 22.8
Read data access time 5	t_{ACC5}	—	$3.0 \times t_{cyc} - 90$	—	$3.0 \times t_{cyc} - 65$	—	$3.0 \times t_{cyc} - 40$	ns	
$\overline{WR}$ delay time 1	t_{WRD1}	—	90	—	50	—	20	ns	Figure 22.8
$\overline{WR}$ delay time 2	t_{WRD2}	—	90	—	50	—	25	ns	Figures 22.7, 22.8
$\overline{WR}$ pulse width 1	t_{WSW1}	$1.0 \times t_{cyc} - 60$	—	$1.0 \times t_{cyc} - 30$	—	$1.0 \times t_{cyc} - 20$	—	ns	Figure 22.7
$\overline{WR}$ pulse width 2	t_{WSW2}	$1.5 \times t_{cyc} - 60$	—	$1.5 \times t_{cyc} - 30$	—	$1.5 \times t_{cyc} - 20$	—	ns	Figure 22.8
Write data delay time	t_{WDD}	—	100	—	50	—	30	ns	Figures 22.7, 22.8
Write data setup time	t_{WDS}	$0.5 \times t_{cyc} - 80$	—	$0.5 \times t_{cyc} - 30$	—	$0.5 \times t_{cyc} - 20$	—	ns	Figure 22.8
Write data hold time	t_{WDH}	$0.5 \times t_{cyc} - 60$	—	$0.5 \times t_{cyc} - 15$	—	$0.5 \times t_{cyc} - 10$	—	ns	Figures 22.7, 22.8
$\overline{WAIT}$ setup time	t_{WTS}	90	—	50	—	25	—	ns	Figure 22.9
$\overline{WAIT}$ hold time	t_{WTH}	10	—	10	—	5	—	ns	
$\overline{BREQ}$ setup time	t_{BRQS}	90	—	50	—	25	—	ns	Figure 22.11
$\overline{BACK}$ delay time	t_{BACD}	—	90	—	50	—	35	ns	
Bus-floating time	t_{BZD}	—	160	—	80	—	50	ns	

B. Product Model Lineup

Product Class		Part No.	Model Name	Marking	Package (code)
H8S/2218 Group	Flash memory Version	HD64F2218	HD64F2218TF24	F2218TF24	100-pin TQFP (TFP-100G, TFP-100GV)
			HD64F2218BR24	64F2218BR24	112-pin P-LFBGA (BP-112, BP-112V)
		HD64F2218U	HD64F2218UTF24	F2218UTF24	100-pin TQFP (TFP-100G, TFP-100GV)
			HD64F2218UBR24	64F2218UBR24	112-pin P-LFBGA (BP-112, BP-112V)
		HD64F2218CU	HD64F2218CUTF24	F2218CUTF24	100-pin TQFP (TFP-100GV)
			HD64F2218CUBR24	64F2218CUBR24	112-pin P-LFBGA (BP-112V)
		HD64F2217CU	HD64F2217CUTF24	F2217CUTF24	100-pin TQFP (TFP-100GV)
			HD64F2217CUBR24	64F2217CUBR24	112-pin P-LFBGA (BP-112V)
	Masked ROM Version	HD6432217	HD6432217(***)TF	2217(***)TF	100-pin TQFP (TFP-100G, TFP-100GV)
			HD6432217(***)BR	2217(***)BR	112-pin P-LFBGA (BP-112, BP-112V)
H8S/2212 Group	Flash memory Version	HD64F2212	HD64F2212FP24	2212FP24	64-pin LQFP (FP-64E, FP-64EV)
			HD64F2212NP24	F2212NP24	64-pin VQFN (TNP-64B, TNP-64BV)
		HD64F2212U	HD64F2212UFP24	2212UFP24	64-pin LQFP (FP-64E, FP-64EV)
			HD64F2212UNP24	F2212UNP24	64-pin VQFN (TNP-64B, TNP-64BV)
		HD64F2212CU	HD64F2212CUFP24	2212CUFP24	64-pin LQFP (FP-64EV)
			HD64F2212CUNP24	F2212CUNP24	64-pin VQFN (TNP-64BV)
		HD64F2211	HD64F2211FP24	2211FP24	64-pin LQFP (FP-64E, FP-64EV)
			HD64F2211NP24	F2211NP24	64-pin VQFN (TNP-64B, TNP-64BV)

Index