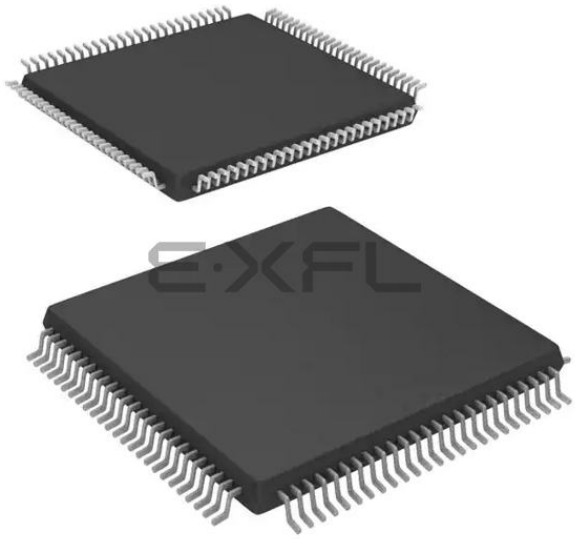
Renesas Electronics America Inc - DF2218UTF24V Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	24MHz
Connectivity	SCI, SmartCard, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	69
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2218utf24v

Item	Page	Revision (See Manual for Details)
Section 16 RAM	551	Table amended

Product Class		ROM Type	RAM Size	RAM Address
H8S/2218 Group	HD64F2218 HD64F2218U HD64F2218CU HD64F2217CU	Flash memory Version	12 kbytes	H'FFC000 to H'FFEFBF H'FFFFC0 to H'FFFFFF
	HD6432217	Masked ROM Version	8 kbytes	H'FFD000 to H'FFEFBF H'FFFFC0 to H'FFFFFF
H8S/2212 Group	HDF64F2212 HDF64F2212U HDF64F2212CU	Flash memory Version	12 kbytes	H'FFC000 to H'FFEFBF H'FFFFC0 to H'FFFFFF
	HD64F2211 HD64F2211U HD64F2211CU HD64F2210CU		8 kbytes	H'FFD000 to H'FFEFBF H'FFFFC0 to H'FFFFFF
	HD6432211	Masked ROM Version	8 kbytes	H'FFD000 to H'FFEFBF H'FFFFC0 to H'FFFFFF
	HD6432210 HD6432210S		4 kbytes	H'FFE000 to H'FFEFBF H'FFFFC0 to H'FFFFFF

17.1 Features	553	Table amended

- Size:

Product Class		ROM Size	ROM Address
H8S/2218 Group	HD64F2218, HD64F2218U HD64F2218CU	128 kbytes	H'000000 to H'01FFFF (Modes 6 and 7)
	HD64F2217CU	64 kbytes	H'000000 to H'00FFFF (Modes 6 and 7)
H8S/2212 Group	HD64F2212, HD64F2212U HD64F2212CU	128 kbytes	H'000000 to H'01FFFF (Mode 7)
	HD64F2211, HD64F2211U HD64F2211CU	64 kbytes	H'000000 to H'00FFFF (Mode 7)
	HD64F2210CU	32 kbytes	H'000000 to H'007FFF (Mode 7)

- Two flash memory operating modes

Description amended

— Boot mode

SCI boot mode: HD64F2218, HD64F2212, and HD64F2211
USB boot mode: HD64F2218U, HD64F2218CU, HD64F2217CU, HD64F2212U, HD64F2212CU, HD64F2211U, HD64F2211CU and HD64F2210CU

Section 2 CPU

The H8S/2000 CPU is a high-speed central processing unit with an internal 32-bit architecture that is upward compatible with the H8/300 and H8/300H CPUs. The H8S/2000 CPU has sixteen 16-bit general registers, can address a 16-Mbyte linear address space, and is ideal for realtime control.

This section describes the H8S/2000 CPU. The usable modes and address spaces differ depending on the product. For details on each product, refer to section 3, MCU Operating Modes.

2.1 Features

- Upward-compatible with H8/300 and H8/300H CPUs
  - Can execute H8/300 and H8/300H CPU object programs
- General-register architecture
  - Sixteen 16-bit general registers also usable as sixteen 8-bit registers or eight 32-bit registers
- Sixty-five basic instructions
  - 8/16/32-bit arithmetic and logic instructions
  - Multiply and divide instructions
  - Powerful bit-manipulation instructions
- Eight addressing modes
  - Register direct [Rn]
  - Register indirect [@ERn]
  - Register indirect with displacement [@(d:16,ERn) or @(d:32,ERn)]
  - Register indirect with post-increment or pre-decrement [@ERn+ or @–ERn]
  - Absolute address [@aa:8, @aa:16, @aa:24, or @aa:32]
  - Immediate [#xx:8, #xx:16, or #xx:32]
  - Program-counter relative [@(d:8,PC) or @(d:16,PC)]
  - Memory indirect [@@aa:8]
- 16-Mbyte address space
  - Program: 16 Mbytes
  - Data: 16 Mbytes
- High-speed operation
  - All frequently-used instructions execute in one or two states
  - 8/16/32-bit register-register add/subtract: 1 state
  - 8 × 8-bit register-register multiply: 12 states
  - 16 ÷ 8-bit register-register divide: 12 states

Section 3 MCU Operating Modes

3.1 Operating Mode Selection

This LSI supports four operating modes (modes 4 to 7). These modes enable selection of the CPU operating mode, enabling/disabling of on-chip ROM, and the initial bus width setting, by setting the mode pins (MD2 to MD0) as show in table 3.1. Modes 4 to 6 are external extended modes that allow access to the external memory and peripheral devices. In external extended mode, 8-bit or 16-bit address space can be set for each area depending on the bus controller setting after program execution starts. If 16-bit access is selected for any one area, 16-bit bus mode is set; if 8-bit access is selected for all areas, 8-bit bus mode is set. In mode 7, the external address space cannot be used. Do not change the mode pin settings during operation. Only mode 7 is available in the H8S/2212 Group.

Table 3.1 MCU Operating Mode Selection

MCU Operating Mode	MD2	MD1	MD0	CPU Operating Mode	Description	On-chip ROM	External Data Bus	
							Initial Value	Maximum Value
4	1	0	0	Advanced mode	On-chip ROM disabled, extended mode	Disabled	16 bits	16 bits
5	1	0	1	Advanced mode	On-chip ROM disabled, extended mode	Disabled	8 bits	16 bits
6	1	1	0	Advanced mode	On-chip ROM enabled, extended mode	Enabled	8 bits	16 bits
7	1	1	1	Advanced mode	Single-chip mode	Enabled	–	–

Note: When using the E6000 emulator:

- Mode 7 is not available in the H8S/2218 Group. (The E6000 emulator does not support mode 7.)
- Note following restrictions to use the RTC and USB in mode 6.
  Specify PFCR so that A9 and A8 are output on the PB1 and PB0 pins.
  Set H'FF in PCDDR so that A7 to A0 are output on the PC7 to PC0 pins.

4.8 Notes on Use of the Stack

When accessing word data or longword data, this LSI assumes that the lowest address bit is 0. The stack should always be accessed by word transfer instruction or longword transfer instruction, and the value of the stack pointer (SP: ER7) should always be kept even. Use the following instructions to save registers:

PUSH.W Rn (or MOV.W Rn, @-SP)
PUSH.L ERn (or MOV.L ERn, @-SP)

Use the following instructions to restore registers:

POP.W Rn (or MOV.W @SP+, Rn)
POP.L ERn (or MOV.L @SP+, ERn)

Setting SP to an odd value may lead to a malfunction. Figure 4.4 shows an example of what happens when the SP value is odd.

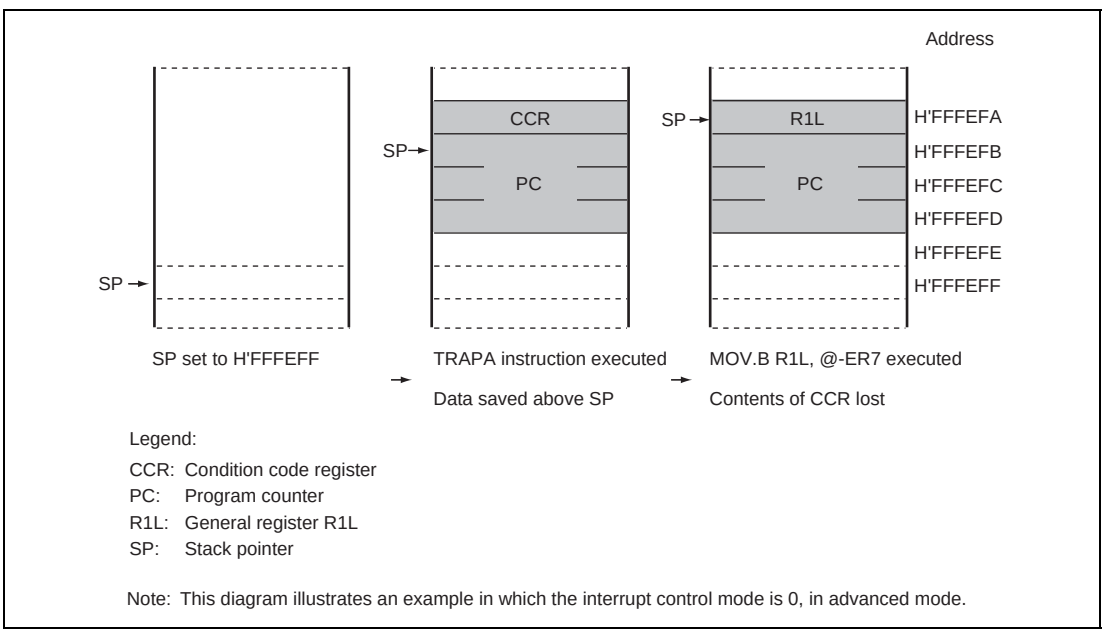


Figure 4.4 Operation when SP Value Is Odd

- WCRL

Bit	Bit Name	Initial Value	R/W	Description
7	W31	1	R/W	Area 3 Wait Control 1 and 0
6	W30	1	R/W	These bits select the number of program wait states when area 3 in external space is accessed while the AST3 bit in ASTCR is set to 1. 00: Program wait not inserted when external space area 3 is accessed 01: 1 program wait state inserted when external space area 3 is accessed 10: 2 program wait states inserted when external space area 3 is accessed 11: 3 program wait states inserted when external space area 3 is accessed
5	W21	1	R/W	Area 2 Wait Control 1 and 0
4	W20	1	R/W	These bits select the number of program wait states when area 2 in external space is accessed while the AST2 bit in ASTCR is set to 1. 00: Program wait not inserted when external space area 2 is accessed 01: 1 program wait state inserted when external space area 2 is accessed 10: 2 program wait states inserted when external space area 2 is accessed 11: 3 program wait states inserted when external space area 2 is accessed

6.6.4 Wait Control

When accessing external space, this LSI can extend the bus cycle by inserting one or more wait states (Tw). There are two ways of inserting wait states: program wait insertion and pin wait insertion using the $\overline{\text{WAIT}}$ pin.

Program Wait Insertion: From 0 to 3 wait states can be inserted automatically between the T_2 state and T_3 state on an individual area basis in 3-state access space, according to the settings of WCRH and WCRL.

Pin Wait Insertion: Setting the WAITE bit in BCRH to 1 enables wait insertion by means of the $\overline{\text{WAIT}}$ pin in the H8S/2218 Group. When external space is accessed in this state, program wait insertion is first carried out according to the settings in WCRH and WCRL. Then, if the $\overline{\text{WAIT}}$ pin is low at the falling edge of ϕ in the last T_2 or T_W state, a T_W state is inserted. If the $\overline{\text{WAIT}}$ pin is held low, T_W states are inserted until it goes high.

7.6.4 Activation Source Acceptance

At the start of activation source acceptance, a low level is detected in both $\overline{\text{DREQ}}$ signal falling edge sensing and low level sensing. Similarly, in the case of an internal interrupt, the interrupt request is detected. Therefore, a request is accepted from an internal interrupt or $\overline{\text{DREQ}}$ pin low level that occurs before execution of the DMABCRL write to enable transfer.

When the DMAC is activated, take any necessary steps to prevent an internal interrupt or $\overline{\text{DREQ}}$ signal low level remaining from the end of the previous transfer, etc.

7.6.5 Internal Interrupt after End of Transfer

When the DTE bit is cleared to 0 by the end of transfer or an abort, the selected internal interrupt request will be sent to the CPU even if DTA is set to 1.

Also, if internal DMAC activation has already been initiated when operation is aborted, the transfer is executed but flag clearing is not performed for the selected internal interrupt even if DTA is set to 1.

An internal interrupt request following the end of transfer or an abort should be handled by the CPU as necessary.

7.6.6 Channel Re-Setting

To reactivate a number of channels when multiple channels are enabled, use exclusive handling of transfer end interrupts, and perform DMABCR control bit operations exclusively. Note, in particular, that in cases where multiple interrupts are generated between reading and writing of DMABCR, and a DMABCR operation is performed during new interrupt handling, the DMABCR write data in the original interrupt handling routine will be incorrect, and the write may invalidate the results of the operations by the multiple interrupts. Ensure that overlapping DMABCR operations are not performed by multiple interrupts, and that there is no separation between read and write operations by the use of a bit-manipulation instruction. Also, when the DTE and DTME bits are cleared by the DMAC or are written with 0, they must first be read while cleared to 0 before the CPU can write a 1 to them.

8.1.4 Pin Functions

Pin Functions of H8S/2218 Group

Port 1 pins also function as address bus (A23 to A20) output pins, TPU I/O pins, and external interrupt input ($\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$) pins. The correspondence between the register specification and the pin functions is shown below.

Table 8.3 P17 Pin Function

TPU Channel 2 Setting*	Output Setting	Input Setting or Initial Value	
P17DDR	—	0	1
Pin Function	TIOCB2 output pin	P17 input pin	P17 output pin
		TIOCB2 input pin	
	TCLKD input pin		

Note: * For details on the TPU channel setting, refer to section 9, 16-Bit Timer Pulse Unit (TPU).

Table 8.4 P16 Pin Function

TPU Channel 2 Setting*[1]	Output Setting	Input Setting or Initial Value	
P16DDR	—	0	1
Pin Function	TIOCA2 output pin	P16 input pin	P16 output pin
		TIOCA2 input pin	
	$\overline{\text{IRQ1}}$ input pin*[2]		

Notes: 1. For details on the TPU channel setting, refer to section 9, 16-Bit Timer Pulse Unit (TPU).
2. When this pin is used as an external interrupt pin, this pin must not be used for another function.

Table 8.5 P15 Pin Function

TPU Channel 1 Setting*	Output Setting	Input Setting or Initial Value	
P15DDR	—	0	1
Pin Function	TIOCB1 output pin	P15 input pin	P15 output pin
		TIOCB1 input pin	
	TCLKC input pin		

Note: * For details on the TPU channel setting, refer to section 9, 16-Bit Timer Pulse Unit (TPU).

Table 8.27 P76 Pin Function

EMLE	0		1
P76DDR	0	1	—
Pin Function	P76 input pin	P76 output pin	TCK input pin

Table 8.28 P75 Pin Function

EMLE	0		1
P75DDR	0	1	—
Pin Function	P75 input pin	P75 output pin	TMS input pin

8.5 Port 9

The port 9 is a 2-bit input port also functioning as A/D converter analog input pins. The port 9 of the H8S/2218 Group has the same function as that of the H8S/2212 Group.

- Port 9 register (PORT9)

8.5.1 Port 9 Register (PORT9)

PORT9 indicates the pin states of the port 9.

Bit	Bit Name	Initial Value	R/W	Description
7	P97	—*	R	The pin states are always read when these bits are read.
6	P96	—*	R	
5 to 0	—	Undefined	—	Reserved These bits are undefined.

Note: * Determined by the states of pins P97 and P96.

8.5.2 Pin Function

The port 9 also functions as A/D converter analog input (AN15 and AN14) pins.

Bit	Bit Name	Initial value	R/W	Description
4	BFA	0	R/W	Buffer Operation A Specifies whether TGRA is to operate in the normal way, or TGRA and TGRC are to be used together for buffer operation. When TGRC is used as a buffer register, TGRC input capture/output compare is not generated. In channels 1 and 2, which have no TGRC, bit 4 is reserved. It is always read as 0 and cannot be modified. 0: TGRA operates normally 1: TGRA and TGRC used together for buffer operation
3	MD3	0	R/W	Modes 3 to 0 These bits are used to set the timer operating mode. MD3 is a reserved bit. In a write, the write value should always be 0. See table 9.8, for details.
2	MD2	0	R/W	
1	MD1	0	R/W	
0	MD0	0	R/W	

Table 9.8 MD3 to MD0

Bit 3	Bit2	Bit 1	Bit 0	
MD3*[1]	**MD2*[2]**	**MD1**	**MD0**	**Description**
0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	×	×	×	—

Legend:

×: Don't care

Notes: 1. MD3 is reserved bit. In a write, it should be written with 0.

2. Phase counting mode cannot be set for channels 0 and 3. In this case, 0 should always be written to MD2.

9.3.9 Timer Synchro Register (TSYR)

TSYR selects independent operation or synchronous operation for the channel 0 to 2 TCNT counters. A channel performs synchronous operation when the corresponding bit in TSYR is set to 1.

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	–	All 0	–	Reserved The write value should always be 0.
2	SYNC2	0	R/W	Timer Synchro 2 to 0
1	SYNC1	0	R/W	These bits select whether operation is independent of or synchronized with other channels. When synchronous operation is selected, synchronous presetting of multiple channels, and synchronous clearing through counter clearing on another channel are possible. To set synchronous operation, the SYNC bits for at least two channels must be set to 1. To set synchronous clearing, in addition to the SYNC bit, the TCNT clearing source must also be set by means of bits CCLR2 to CCLR0 in TCR. 0: TCNT_2 to TCNT_0 operates independently (TCNT presetting /clearing is unrelated to other channels) 1: TCNT_2 to TCNT_0 performs synchronous operation TCNT synchronous presetting/synchronous clearing is possible
0	SYNC0	0	R/W	

Example of Synchronous Operation: Figure 9.15 shows an example of synchronous operation. In this example, synchronous operation and PWM mode 1 have been designated for channels 0 to 2, TGRB_0 compare match has been set as the channel 0 counter clearing source, and synchronous clearing has been set for the channel 1 and 2 counter clearing source. Three-phase PWM waveforms are output from pins TIOC0A, TIOC1A, and TIOC2A. At this time, synchronous presetting, and synchronous clearing by TGRB_0 compare match, is performed for channel 0 to 2 TCNT counters, and the data set in TGRB_0 is used as the PWM cycle. For details of PWM modes, see section 9.5.4, PWM Modes.

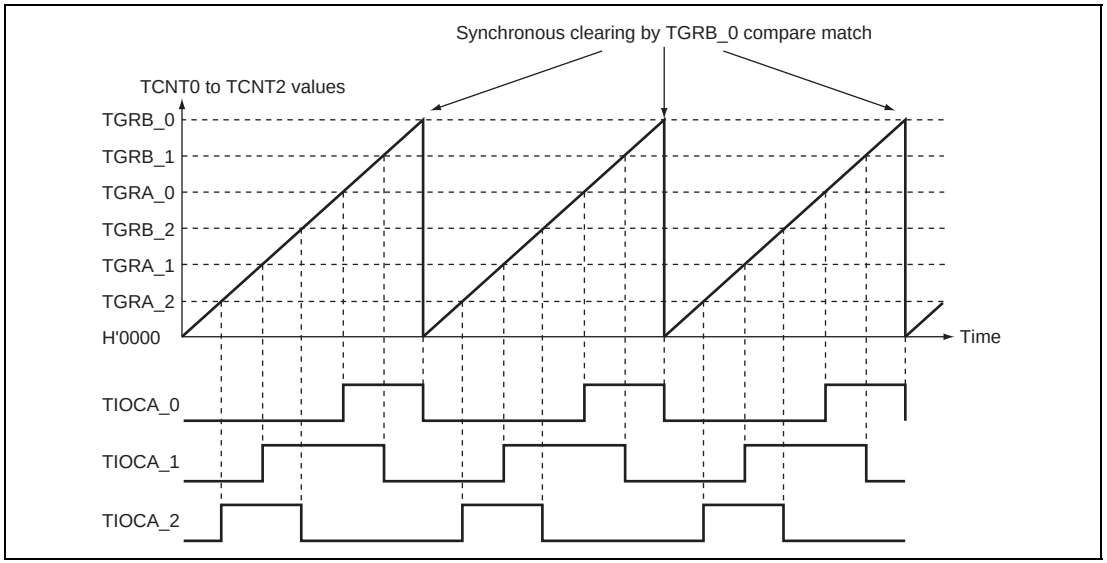


Figure 9.15 Example of Synchronous Operation

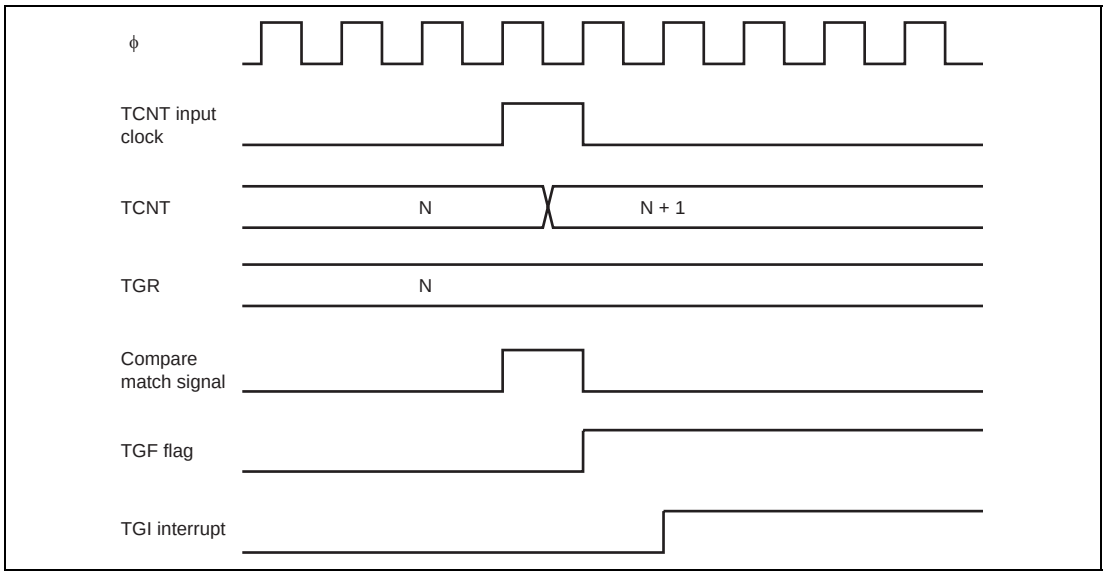


Figure 9.38 TGI Interrupt Timing (Compare Match)

TGF Flag Setting Timing in Case of Input Capture: Figure 9.39 shows the timing for setting of the TGF flag in TSR by input capture occurrence, and TGI interrupt request signal timing.

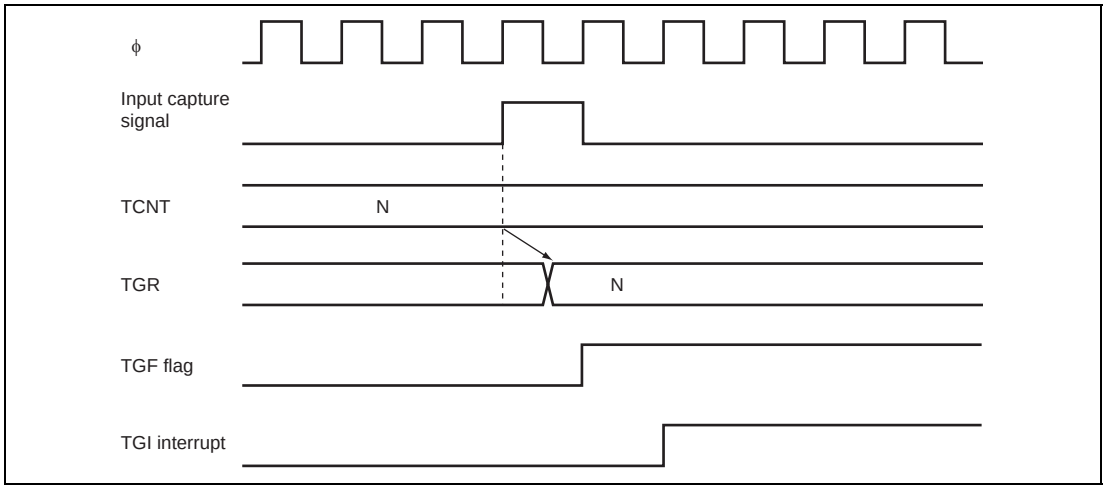
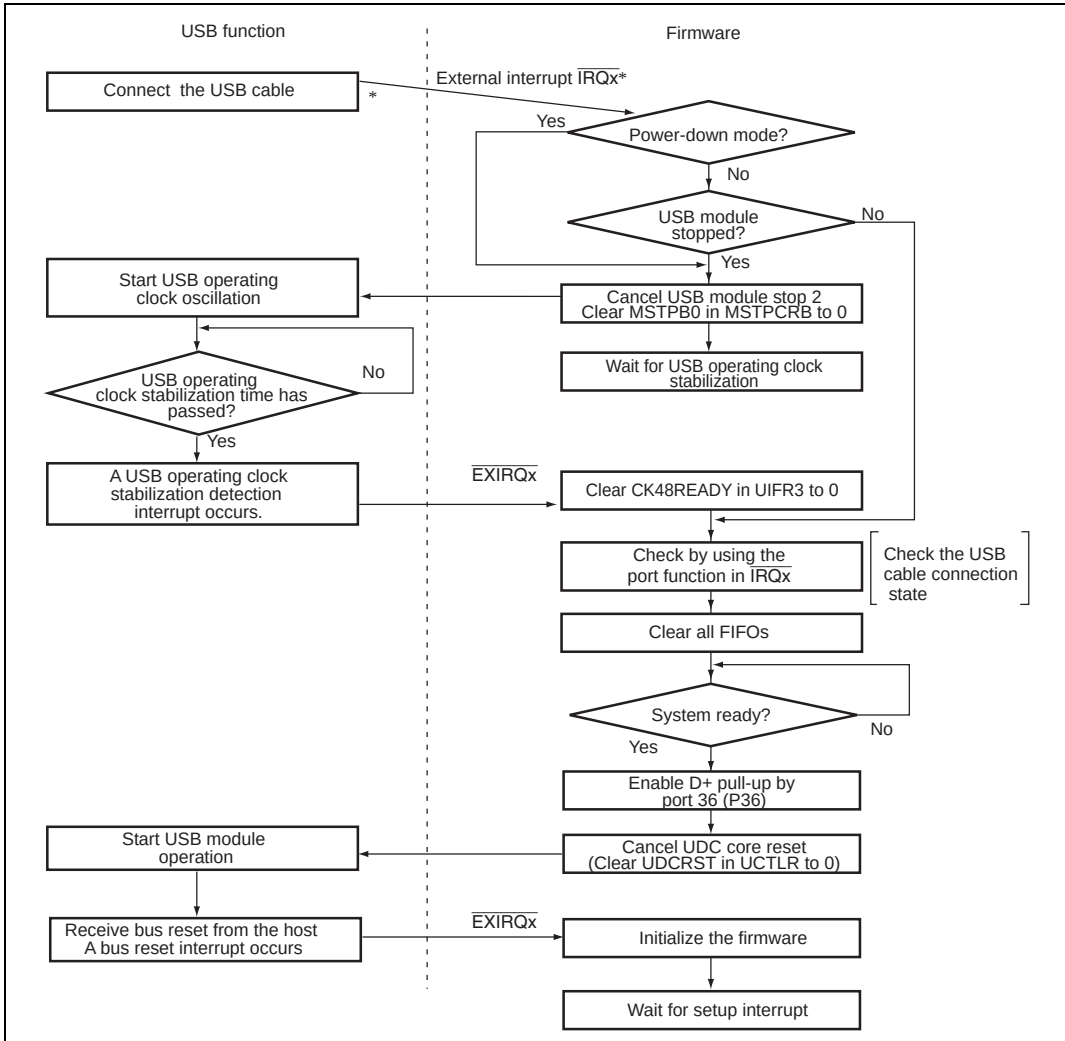


Figure 9.39 TGI Interrupt Timing (Input Capture)

Bit	Bit Name	Initial Value	R/W	Description
1	UIFRST	1	R/W	USB Interface Software Reset Controls USB module internal reset. When the UIFRST bit is set to 1, the USB internal modules other than UCTLR, UIER3, and the CK48READY bit in UIFR3 are all reset. At initialization, the UIFRST bit must be cleared to 0 after the USB operating clock (48 MHz) stabilization time has passed following the clearing of the USB module stop 2 bit. 0: Sets the USB internal modules to the operating state. (At initialization, this bit must be cleared after the USB operating clock stabilization time has passed.) 1: Sets the USB internal modules other than UCTLR, UIER3, and the CK48READY bit in UIFR3 to the reset state. If the UIFRST bit is set to 1 after it is cleared to 0, the UDCRST bit should also be set to 1 simultaneously.
0	UDCRST	1	R/W	UDC Core Software Reset Controls reset of the UDC core in the USB module. When the UDCRST bit is set to 1, the UDC core is reset and the USB bus synchronization operation stops. At initialization, UDCRST must be cleared to 0 after D+ pull-up by the port (P36) control following the clearing of the UIFRST bit. In the suspend state, to maintain the internal state of the UDC core, enter power-down mode after setting the USB module stop 2 bit with the UDCRST bit to be maintained to 0. After VBUS disconnection detection, UDCRST must be set to 1. 0: Sets the UDC core in the USB module to operating state. (At initialization, UDCRST must be cleared to 0 after D+ pull-up by the port control following the clearing of the UIFRST bit.) 1: Sets the UDC core in the USB module to reset state. (In the suspend state, UDCRST must not be set to 1; after VBUS disconnection detection, UDCRST must be set to 1.)

(2) USB Cable Connection (When USB module stop or power-down mode is used)

If the USB cable enters the connection state from the disconnection state in an application (self powered) where USB module stop or power-down mode is used, perform the operation as shown in figure 14.4.



Note: * A VBUS interrupts in the USB module cannot be detected in power-down mode or in the USB module stop state. Accordingly, in an application (self powered) where power-down mode or USB module stop is used,VBUS interrupts of the USB must be detected via the external interrupt pin IRQx.
In this case, the IRQx pin must be specified as both-edge sensitive. When IRQx is used, VBUS interrupts in the USB module need not to be used.

Figure 14.4 USB Cable Connection (When USB Module Stop or Power-Down Mode Is Used)

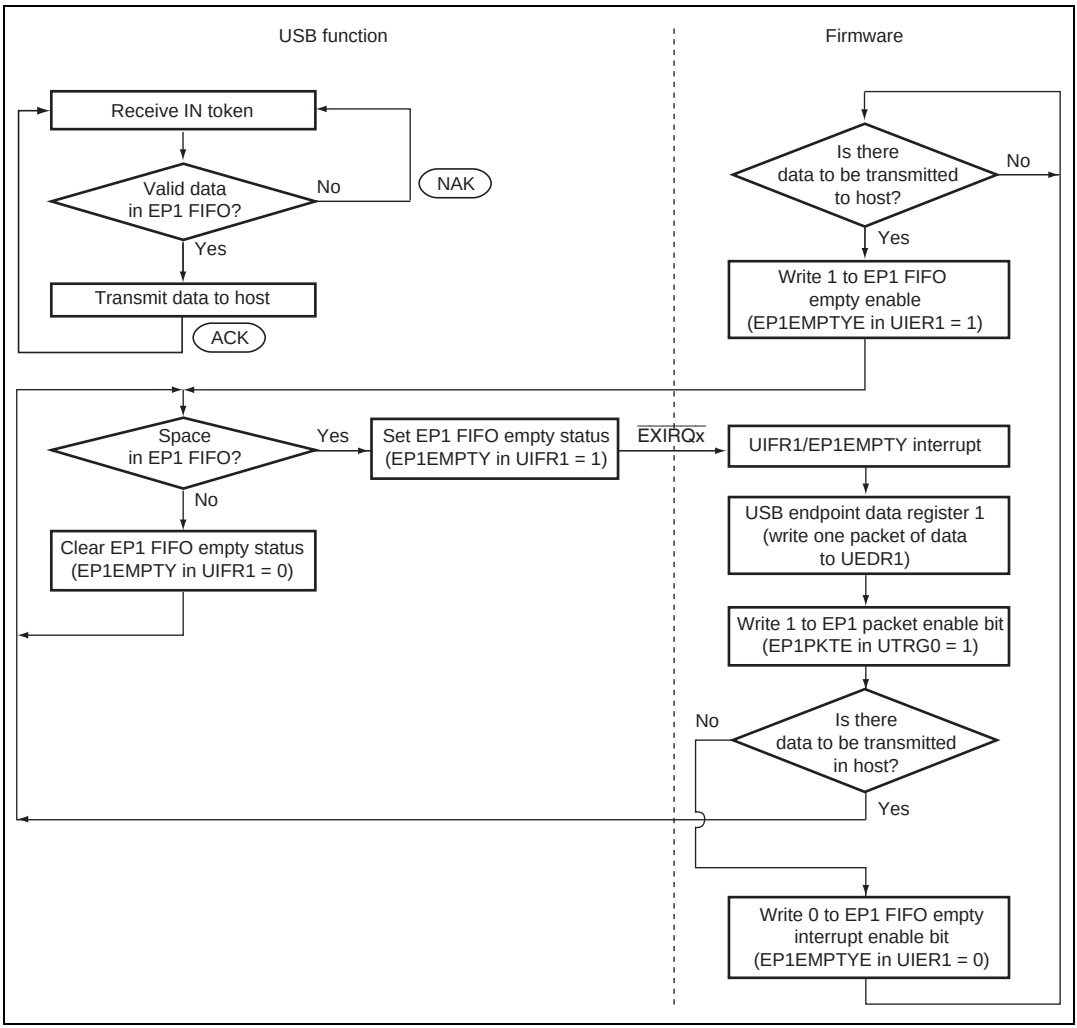


Figure 14.18 EP1 Bulk-In Transfer Operation

Figure 17.6 shows the block configuration of 64-kbyte flash memory in the HD64F2217CU, HD64F2211, HD64F2211U and HD64F2211CU. The thick lines indicate erasing units, the narrow lines indicate programming units, and the values are addresses. The flash memory is divided into one kbyte (four blocks), 28 kbytes (one block), and 16 kbytes (one block), eight kbytes (two blocks). Erasing is performed in these divided units. Programming is performed in 128-byte units starting from an address whose lower eight bits are H'00 or H'80.

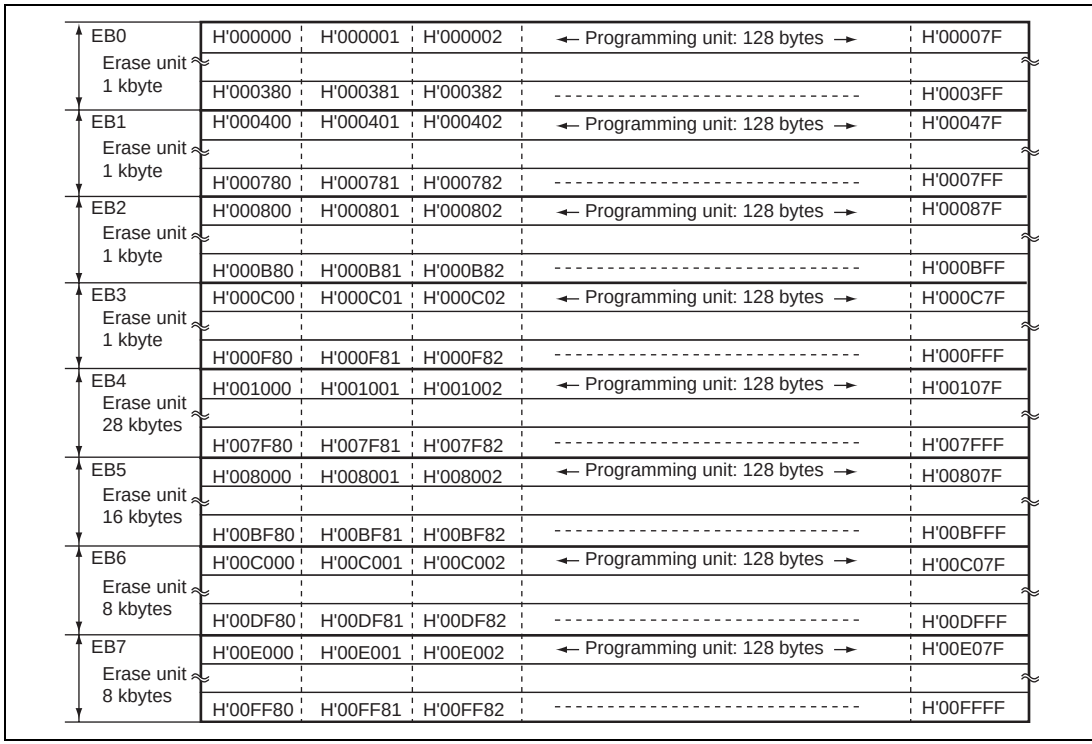


Figure 17.6 Flash Memory Block Configuration (HD64F2217CU, HD64F2211, HD64F2211U, HD64F2211CU)

Table 20.2 Transition Conditions of Power-Down Modes

Pre-Transition State	Status of Control Bit at Transition				State after Transition Invoked by SLEEP Command	State after Transition Back from Power-Down Mode Invoked by Interrupt
	SSBY	PSS	LSON	DTON		
High-speed/ Medium-speed	0	×	0	×	Sleep	High-speed/Medium-speed
	0	×	1	×	—	—
	1	0	0	×	Software standby	High-speed/Medium-speed
	1	0	1	×	—	—
	1	1	0	0	Watch	High-speed
	1	1	1	0	Watch	Subactive
	1	1	0	1	—	—
	1	1	1	1	Subactive	—
Subactive	0	0	×	×	—	—
	0	1	0	×	—	—
	0	1	1	×	Sub sleep	Subactive
	1	0	×	×	—	—
	1	1	0	0	Watch	High-speed
	1	1	1	0	Watch	Subactive
	1	1	0	1	High-speed	—
	1	1	1	1	—	—

Legend:

×: Don’t care

—: Do not set

Appendix

A. I/O Port States in Each Processing State

Port Name / Pin Name	MCU Operating Mode	Power-on Reset	Manual Reset	Hardware Standby Mode	Software Standby Mode or Watch Mode	Bus Right Release State	Program Execution State or Sleep Mode
P17 to P14	4 to 7	T	keep	T	keep	keep	I/O port
P13/A23 P12/A22 P11/A21	7	T	keep	T	keep	keep	I/O port
Address output selected by AEn bit	4 to 6	T	keep	T	[OPE=0] T [OPE=1] keep	T	Address output
Port selection	4 to 6	T	keep	T	keep	keep	I/O port
P10/A20	7	T	keep	T	keep	keep	I/O port
Address output selected by AEn bit	4 and 5	L	keep	T	[OPE=0] T [OPE=1] keep	T	Address output
	6	T					
Port selection	4 to 6	T*1	keep	T	keep	keep	I/O port
Port 3	4 to 7	T	keep	T	keep	keep	I/O port
Port 4	4 to 7	T	T	T	T	T	Input port
P77 to P75*3	7	T	keep	T	keep	keep	I/O port
P74*2	4 to 7	T	keep	T	keep	keep	I/O port
P71/$\overline{CS5}$*2	7	T	keep	T	keep	keep	I/O port
P70/$\overline{CS4}$*2	4 to 6	T	keep	T	[DDR•OPE=0] T [DDR•OPE=1] H	T	[DDR=0] Input port [DDR=1] $\overline{CS5}$, $\overline{CS4}$
Port 9	4 to 7	T	T	T	[DAOEn=1] keep [DAOEn=0] T	keep	Input port

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