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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	8
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	10-VFDFN Exposed Pad
Supplier Device Package	11-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f302r

1. System Overview

C8051F300/1/2/3/4/5 devices are fully integrated mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 1.1 on page 14 for specific product feature selection.

- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 8-bit 500 ksps 11-channel ADC with programmable gain pre-amplifier and analog multiplexer (C8051F300/2 only)
- Precision programmable 25 MHz internal oscillator
- Up to 8 kB of on-chip Flash memory
- 256 bytes of on-chip RAM
- SMBus/I^2C and Enhanced UART serial interfaces implemented in hardware
- Three general-purpose 16-bit timers
- Programmable counter/timer array (PCA) with three capture/compare modules and watchdog timer function
- On-chip power-on reset, V_{DD} monitor, and temperature sensor
- On-chip voltage comparator
- Byte-wide I/O port (5 V tolerant)

With on-chip Power-On Reset, V_{DD} monitor, Watchdog Timer, and clock oscillator, the C8051F300/1/2/3/4/5 devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Laboratories 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 2.7 to 3.6 V operation over the industrial temperature range (–45 to +85 °C). The Port I/O and $\overline{RST}$ pins are tolerant of input signals up to 5 V. The C8051F300/1/2/3/4/5 are available in 3 x 3 mm 11-pin QFN or 14-pin SOIC packaging.

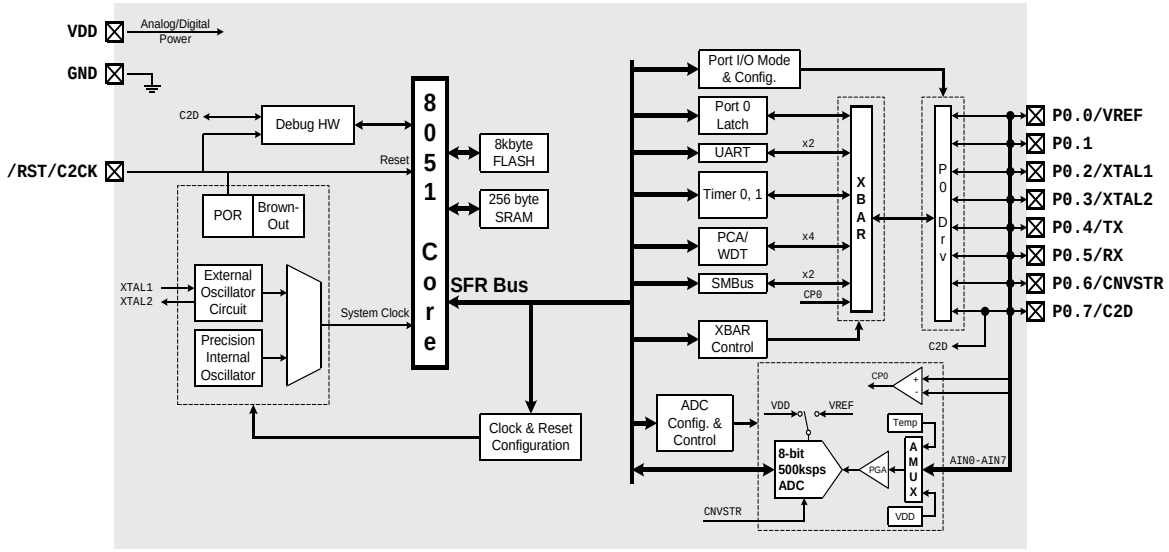

Figure 1.1. C8051F300/2 Block Diagram

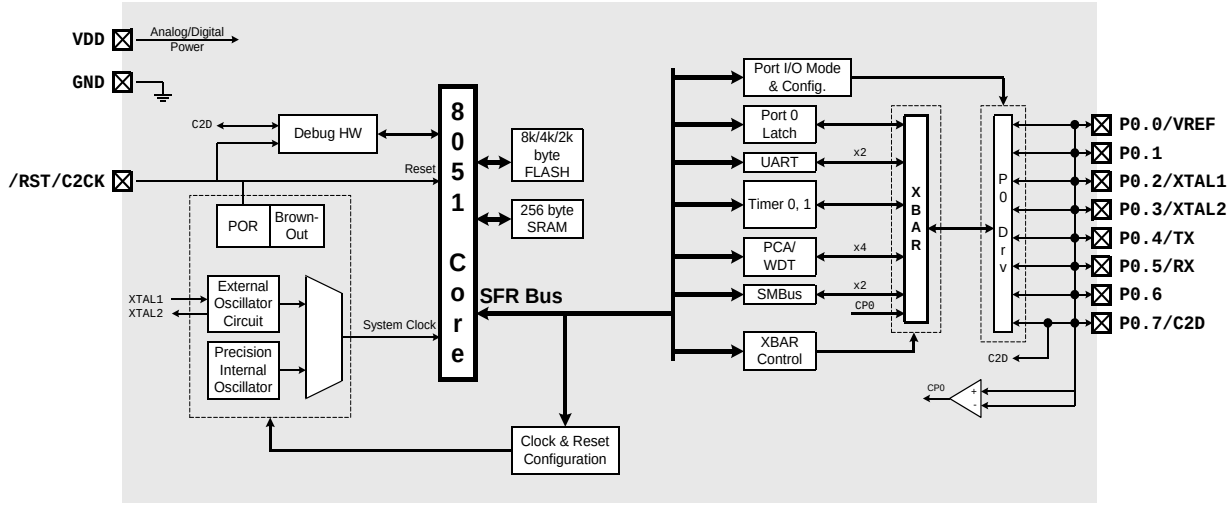

Figure 1.2. C8051F301/3/4/5 Block Diagram

Perhaps the most unique Port I/O enhancement is the Digital Crossbar. This is essentially a digital switching network that allows mapping of internal digital system resources to Port I/O pins (See Figure 1.7). On-chip counter/timers, serial buses, HW interrupts, comparator output, and other digital signals in the controller can be configured to appear on the Port I/O pins specified in the Crossbar Control registers. This allows the user to select the exact mix of general purpose Port I/O and digital resources needed for the particular application.

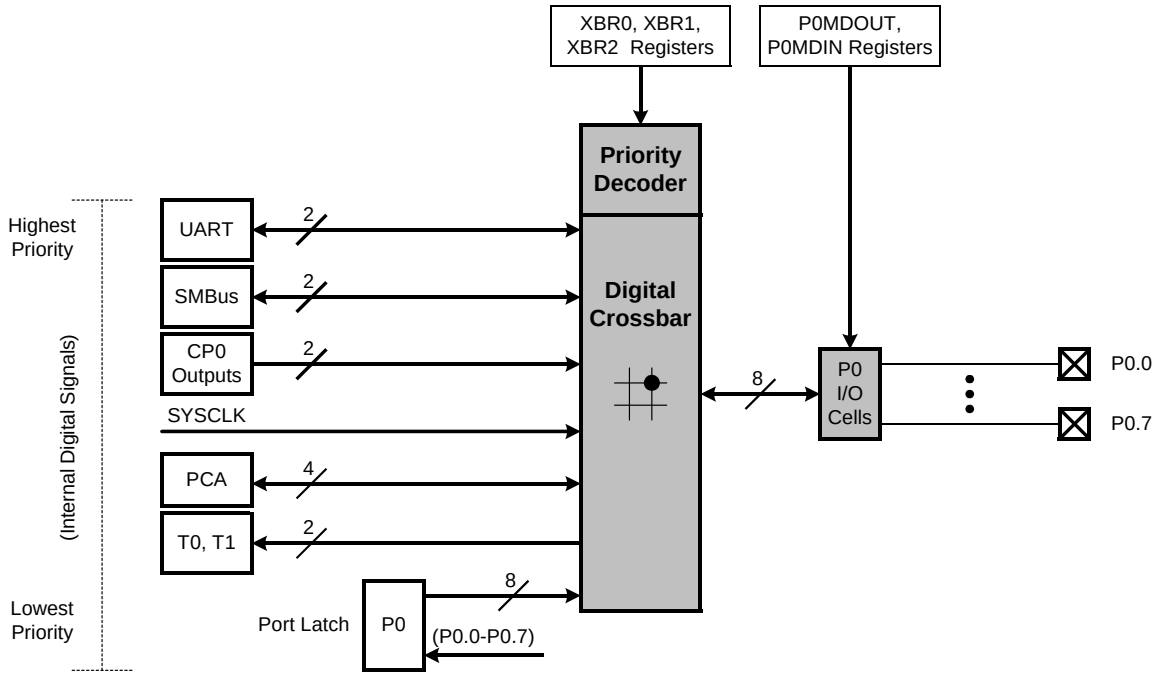

Figure 1.7. Digital Crossbar Diagram

1.5. Serial Ports

The C8051F300/1/2/3/4/5 Family includes an SMBus/I^2C interface and a full-duplex UART with enhanced baud rate configuration. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little CPU intervention.

1.8. Comparator

C8051F300/1/2/3/4/5 devices include an on-chip voltage comparator that is enabled/disabled and configured via user software. All Port I/O pins may be configurated as comparator inputs. Two comparator outputs may be routed to a Port pin if desired: a latched output and/or an unlatched (asynchronous) output. Comparator response time is programmable, allowing the user to select between high-speed and low-power modes. Positive and negative hysteresis is also configurable.

Comparator interrupts may be generated on rising, falling, or both edges. When in IDLE mode, these interrupts may be used as a “wake-up” source. The comparator may also be configured as a reset source.

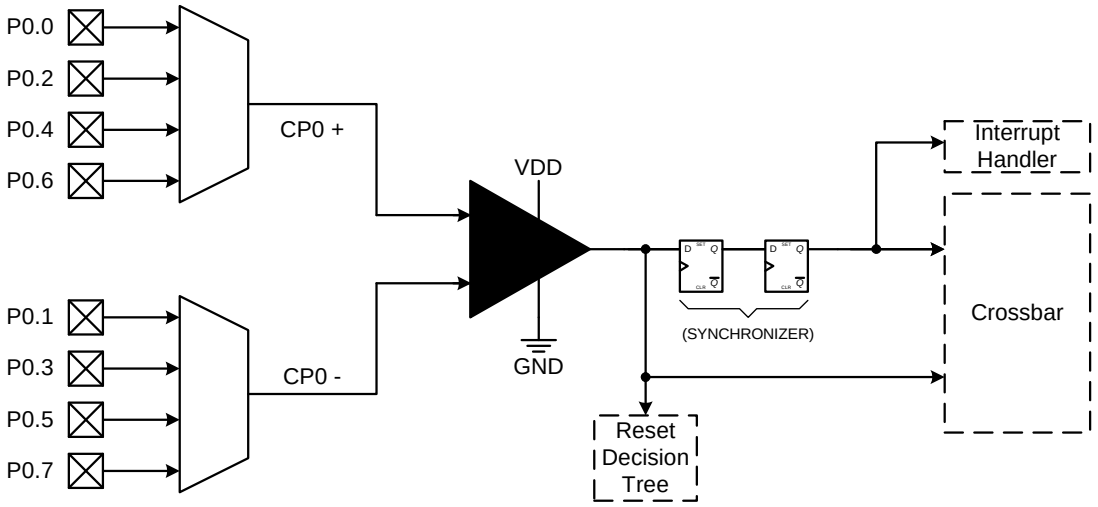

Figure 1.11. Comparator Block Diagram

3. Global Electrical Characteristics

Table 3.1. Global Electrical Characteristics

–40 to +85 °C, 25 MHz system clock unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Digital Supply Voltage		V_{RST}[1]	3.0	3.6	V
Digital Supply RAM Data Retention Voltage		—	1.5	—	V
SYSCLK (System Clock) (Note 2)		0	—	25	MHz
T_{SYSH} (SYSCLK High Time)		18	—	—	ns
T_{SYSL} (SYSCLK Low Time)		18	—	—	ns
Specified Operating Temperature Range		–40	—	+85	°C
Digital Supply Current—CPU Active (Normal Mode, fetching instructions from Flash)					
I_{DD} (Note 3)	V_{DD} = 3.6 V, F = 25 MHz	—	9.4	10.2	mA
	V_{DD} = 3.0 V, F = 25 MHz	—	6.6	7.2	mA
	V_{DD} = 3.0 V, F = 1 MHz	—	0.45	—	mA
	V_{DD} = 3.0 V, F = 80 kHz	—	36	—	µA
I_{DD} Supply Sensitivity (Note 3)	F = 25 MHz	—	69	—	%/V
	F = 1 MHz	—	51	—	%/V
I_{DD} Frequency Sensitivity (Note 3, Note 4)	V_{DD} = 3.0 V, F <= 15 MHz, T = 25 °C	—	0.45	—	mA/MHz
	V_{DD} = 3.0 V, F > 15 MHz, T = 25 °C	—	0.16	—	mA/MHz
	V_{DD} = 3.6 V, F <= 15 MHz, T = 25 °C	—	0.69	—	mA/MHz
	V_{DD} = 3.6 V, F > 15 MHz, T = 25 °C	—	0.20	—	mA/MHz
Digital Supply Current—CPU Inactive (Idle Mode, not fetching instructions from Flash)					
I_{DD} (Note 3)	V_{DD} = 3.6 V, F = 25 MHz	—	3.3	4.0	mA
	V_{DD} = 3.0 V, F = 25 MHz	—	2.5	3.2	mA
	V_{DD} = 3.0 V, F = 1 MHz	—	0.10	—	mA
	V_{DD} = 3.0 V, F = 80 kHz	—	8	—	µA

5.1. Analog Multiplexer and PGA

The analog multiplexers (AMUX0) select the positive and negative inputs to the PGA, allowing any Port pin to be measured relative to any other Port pin or GND. Additionally, the on-chip temperature sensor or the positive power supply (V_{DD}) may be selected as the positive PGA input. **When GND is selected as the negative input, ADC0 operates in Single-ended Mode; all other times, ADC0 operates in Differential Mode.** The ADC0 input channels are selected in the AMX0SL register as described in SFR Definition 5.1.

The conversion code format differs in Single-ended versus Differential modes, as shown below. When in Single-ended Mode (negative input is selected GND), conversion codes are represented as 8-bit unsigned integers. Inputs are measured from ‘0’ to VREF x 255/256. Example codes are shown below.

Input Voltage	ADC0 Output (Conversion Code)
VREF x 255/256	0xFF
VREF x 128/256	0x80
VREF x 64/256	0x40
0	0x00

When in Differential Mode (negative input is not selected as GND), conversion codes are represented as 8-bit signed 2s complement numbers. Inputs are measured from –VREF to VREF x 127/128. Example codes are shown below.

Input Voltage	ADC0 Output (Conversion Code)
VREF x 127/128	0x7F
VREF x 64/128	0x40
0	0x00
–VREF x 64/128	0xC0
–VREF	0x80

Important Note About ADC0 Input Configuration: Port pins selected as ADC0 inputs should be configured as analog inputs and should be skipped by the Digital Crossbar. To configure a Port pin for analog input, set to ‘0’ the corresponding bit in register P0MDIN. To force the Crossbar to skip a Port pin, set to ‘1’ the corresponding bit in register XBR0. See **Section “12. Port Input/Output” on page 103** for more Port I/O configuration details.

The PGA amplifies the AMUX0 output signal as defined by the AMP0GN1-0 bits in the ADC0 Configuration register (SFR Definition 5.2). The PGA is software-programmable for gains of 0.5, 1, 2, or 4. The gain defaults to 0.5 on reset.

5.2. Temperature Sensor

The typical temperature sensor transfer function is shown in Figure 5.2. The output voltage (V_{TEMP}) is the positive PGA input when the temperature sensor is selected by bits AMX0P2-0 in register AMX0SL; this voltage will be amplified by the PGA according to the user-programmed PGA settings.

8. CIP-51 Microcontroller

The MCU system controller core is the CIP-51 microcontroller. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The MCU family has a superset of all the peripherals included with a standard 8051. Included are three 16-bit counter/timers (see description in **Section 15**), an enhanced full-duplex UART (see description in **Section 14**), 256 bytes of internal RAM, 128 byte Special Function Register (SFR) address space (**Section 8.2.6**), and one byte-wide I/O Port (see description in **Section 12**). The CIP-51 also includes on-chip debug hardware (see description in **Section 17**), and interfaces directly with the analog and digital subsystems providing a complete data acquisition or control-system solution in a single integrated circuit.

The CIP-51 Microcontroller core implements the standard 8051 organization and peripherals as well as additional custom peripherals and functions to extend its capability (see Figure 8.1 for a block diagram). The CIP-51 includes the following features:

- Fully Compatible with MCS-51 Instruction Set
- 25 MIPS Peak Throughput with 25 MHz Clock
- 0 to 25 MHz Clock Frequency
- 256 Bytes of Internal RAM
- Byte-Wide I/O Port
- Extended Interrupt Handler
- Reset Input
- Power Management Modes
- On-chip Debug Logic
- Program and Data Memory Security

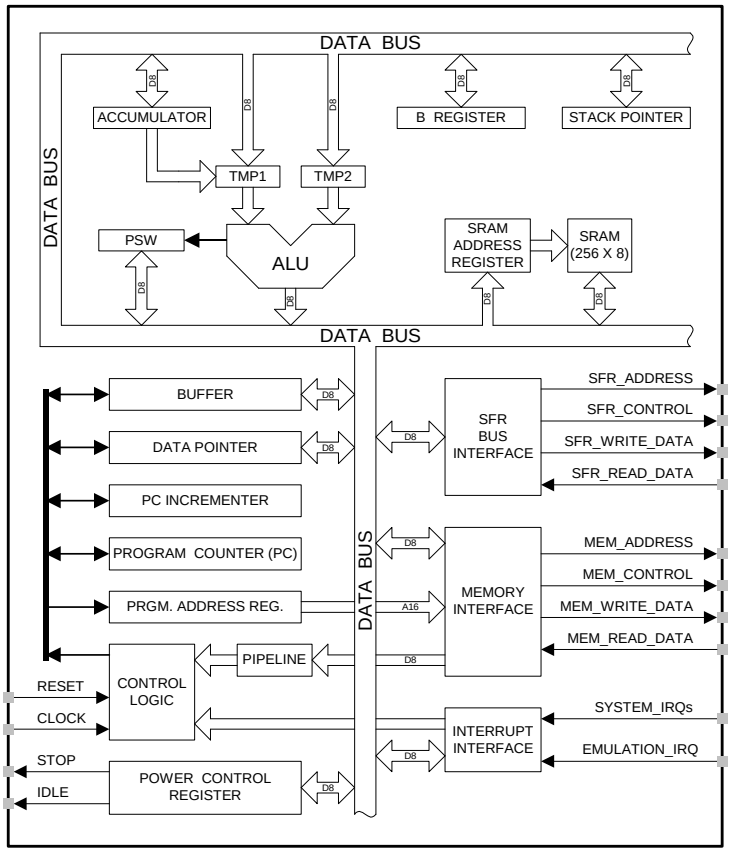

Figure 8.1. CIP-51 Block Diagram

Table 8.3. Special Function Registers* (Continued)

Register	Address	Description	Page No.
FLSCL	0xB6	Flash Scale	93
IE	0xA8	Interrupt Enable	75
IP	0xB8	Interrupt Priority	76
IT01CF	0xE4	INT0/INT1 Configuration Register	79
OSCICL	0xB3	Internal Oscillator Calibration	98
OSCICN	0xB2	Internal Oscillator Control	98
OSCXCN	0xB1	External Oscillator Control	100
P0	0x80	Port 0 Latch	109
P0MDIN	0xF1	Port 0 Input Mode Configuration	109
P0MDOUT	0xA4	Port 0 Output Mode Configuration	110
PCA0CN	0xD8	PCA Control	167
PCA0MD	0xD9	PCA Mode	168
PCA0CPH0	0xFC	PCA Capture 0 High	171
PCA0CPH1	0xEA	PCA Capture 1 High	171
PCA0CPH2	0xEC	PCA Capture 2 High	171
PCA0CPL0	0xFB	PCA Capture 0 Low	171
PCA0CPL1	0xE9	PCA Capture 1 Low	171
PCA0CPL2	0xEB	PCA Capture 2 Low	171
PCA0CPM0	0xDA	PCA Module 0 Mode Register	169
PCA0CPM1	0xDB	PCA Module 1 Mode Register	169
PCA0CPM2	0xDC	PCA Module 2 Mode Register	169
PCA0H	0xFA	PCA Counter High	170
PCA0L	0xF9	PCA Counter Low	170
PCON	0x87	Power Control	81
PSCTL	0x8F	Program Store R/W Control	92
PSW	0xD0	Program Status Word	70
REF0CN	0xD1	Voltage Reference Control	49
RSTSRC	0xEF	Reset Source Configuration/Status	87
SBUF0	0x99	UART 0 Data Buffer	137
SCON0	0x98	UART 0 Control	136
SMB0CF	0xC1	SMBus Configuration	118
SMB0CN	0xC0	SMBus Control	120
SMB0DAT	0xC2	SMBus Data	122
SP	0x81	Stack Pointer	69
TMR2CN	0xC8	Timer/Counter 2 Control	154
TCON	0x88	Timer/Counter Control	147
TH0	0x8C	Timer/Counter 0 High	150

***Note:** SFRs are listed in alphabetical order. All undefined SFR locations are reserved

SFR Definition 8.10. EIP1: Extended Interrupt Priority 1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
—	—	PCP0R	PCP0F	PPCA0	PADC0C	PWADC0	PSMB0	11000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xF6

Bits7–6: UNUSED. Read = 11b. Write = don't care.

Bit5: PCP0R: Comparator0 (CP0) Rising Interrupt Priority Control.
This bit sets the priority of the CP0 rising-edge interrupt.
0: CP0 rising interrupt set to low priority level.
1: CP0 rising interrupt set to high priority level.

Bit4: PCP0F: Comparator0 (CP0) Falling Interrupt Priority Control.
This bit sets the priority of the CP0 falling-edge interrupt.
0: CP0 falling interrupt set to low priority level.
1: CP0 falling interrupt set to high priority level.

Bit3: PPCA0: Programmable Counter Array (PCA0) Interrupt Priority Control.
This bit sets the priority of the PCA0 interrupt.
0: PCA0 interrupt set to low priority level.
1: PCA0 interrupt set to high priority level.

Bit2: PADC0C ADC0 Conversion Complete Interrupt Priority Control
This bit sets the priority of the ADC0 Conversion Complete interrupt.
0: ADC0 Conversion Complete interrupt set to low priority level.
1: ADC0 Conversion Complete interrupt set to high priority level.

Bit1: PWADC0: ADC0 Window Comparator Interrupt Priority Control.
This bit sets the priority of the ADC0 Window interrupt.
0: ADC0 Window interrupt set to low priority level.
1: ADC0 Window interrupt set to high priority level.

Bit0: PSMB0: SMBus Interrupt Priority Control.
This bit sets the priority of the SMBus interrupt.
0: SMBus interrupt set to low priority level.
1: SMBus interrupt set to high priority level.

8.4.2. Stop Mode

Setting the Stop Mode Select bit (PCON.1) causes the CIP-51 to enter Stop mode as soon as the instruction that sets the bit completes execution. In Stop mode the internal oscillator, CPU, and all digital peripherals are stopped; the state of the external oscillator circuit is not affected. Each analog peripheral (including the external oscillator circuit) may be shut down individually prior to entering Stop Mode. Stop mode can only be terminated by an internal or external reset. On reset, the CIP-51 performs the normal reset sequence and begins program execution at address 0x0000.

If enabled, the Missing Clock Detector will cause an internal reset and thereby terminate the Stop mode. The Missing Clock Detector should be disabled if the CPU is to be put to in STOP mode for longer than the MCD timeout of 100 µsec.

SFR Definition 8.12. PCON: Power Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
GF5	GF4	GF3	GF2	GF1	GF0	STOP	IDLE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x87

Bits7–2: GF5–GF0: General Purpose Flags 5-0.
These are general purpose flags for use under software control.

Bit1: STOP: Stop Mode Select.
Setting this bit will place the CIP-51 in Stop mode. This bit will always be read as 0.
1: CPU goes into Stop mode (turns off internal oscillator).

Bit0: IDLE: Idle Mode Select.
Setting this bit will place the CIP-51 in Idle mode. This bit will always be read as 0.
1: CPU goes into Idle mode (shuts off clock to CPU, but clock to Timers, Interrupts, Serial Ports, and Analog Peripherals are still active).

viced in priority order after the Flash operation has been completed and interrupts have been re-enabled by software.

10. Make certain that the Flash write and erase pointer variables are not located in XRAM. See your compiler documentation for instructions regarding how to explicitly locate variables in different memory areas.
11. Add address bounds checking to the routines that write or erase Flash memory to ensure that a routine called with an illegal address does not result in modification of the Flash.

10.4.3. System Clock

12. If operating from an external crystal, be advised that crystal performance is susceptible to electrical interference and is sensitive to layout and to changes in temperature. If the system is operating in an electrically noisy environment, use the internal oscillator or use an external CMOS clock.
13. If operating from the external oscillator, switch to the internal oscillator during Flash write or erase operations. The external oscillator can continue to run, and the CPU can switch back to the external oscillator after the Flash operation has completed.

Additional Flash recommendations and example code can be found in *AN201, "Writing to Flash from Firmware"*, available from the Silicon Laboratories web site.

NOTES:

SFR Definition 11.1. OSCICL: Internal Oscillator Calibration

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
—								Variable
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xB3

Bit7: UNUSED. Read = 0. Write = don't care.
Bits 6–0: OSCICL: Internal Oscillator Calibration Register.
This register calibrates the internal oscillator period. The reset value for OSCICL defines the internal oscillator base frequency. On C8051F300/1 devices, the reset value is factory calibrated to generate an internal oscillator frequency of 24.5 MHz.

SFR Definition 11.2. OSCICN: Internal Oscillator Control

R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	Reset Value
—	—	—	IFRDY	CLKSL	IOSCEN	IFCN1	IFCN0	00010100
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xB2

Bits7–5: UNUSED. Read = 000b, Write = don't care.
Bit4: IFRDY: Internal Oscillator Frequency Ready Flag.
0: Internal Oscillator is not running at programmed frequency.
1: Internal Oscillator is running at programmed frequency.
Bit3: CLKSL: System Clock Source Select Bit.
0: SYSCLK derived from the Internal Oscillator, and scaled as per the IFCN bits.
1: SYSCLK derived from the External Oscillator circuit.
Bit2: IOSCEN: Internal Oscillator Enable Bit.
0: Internal Oscillator Disabled.
1: Internal Oscillator Enabled.
Bits1–0: IFCN1-0: Internal Oscillator Frequency Control Bits.
00: SYSCLK derived from Internal Oscillator divided by 8.
01: SYSCLK derived from Internal Oscillator divided by 4.
10: SYSCLK derived from Internal Oscillator divided by 2.
11: SYSCLK derived from Internal Oscillator divided by 1.

SFR Definition 12.6. P0MDOUT: Port0 Output Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xA4

Bits7–0: Output Configuration Bits for P0.7–P0.0 (respectively): ignored if corresponding bit in register P0MDIN is logic 0.
0: Corresponding P0.n Output is open-drain.
1: Corresponding P0.n Output is push-pull.

(Note: When SDA and SCL appear on any of the Port I/O, each are open-drain regardless of the value of P0MDOUT).

Table 12.1. Port I/O DC Electrical Characteristics

V_{DD} = 2.7 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameters	Conditions	Min	Typ	Max	Units
Output High Voltage	I_{OH} = –3 mA, Port I/O push-pull I_{OH} = –10 µA, Port I/O push-pull I_{OH} = –10 mA, Port I/O push-pull	V_{DD} – 0.7 V_{DD} – 0.1	 V_{DD}-0.8	—	V
Output Low Voltage	I_{OL} = 8.5 mA I_{OL} = 10 µA I_{OL} = 25 mA	— — —	— — 1.0	0.6 0.1 —	V
Input High Voltage		2.0	—	—	V
Input Low Voltage		—	—	0.8	V
Input Leakage Current	Weak Pull-up Off Weak Pull-up On, V_{IN} = 0 V	—	 25	±1 40	µA

13.4.3. Data Register

The SMBus Data register SMB0DAT holds a byte of serial data to be transmitted or one that has just been received. Software may safely read or write to the data register when the SI flag is set. Software should not attempt to access the SMB0DAT register when the SMBus is enabled and the SI flag is cleared to logic 0, as the interface may be in the process of shifting a byte of data into or out of the register.

Data in SMB0DAT is always shifted out MSB first. After a byte has been received, the first bit of received data is located at the MSB of SMB0DAT. While data is being shifted out, data on the bus is simultaneously being shifted in. SMB0DAT always contains the last data byte present on the bus. In the event of lost arbitration, the transition from master transmitter to slave receiver is made with the correct data or address in SMB0DAT.

SFR Definition 13.3. SMB0DAT: SMBus Data

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xC2

Bits7–0: SMB0DAT: SMBus Data.
The SMB0DAT register contains a byte of data to be transmitted on the SMBus serial interface or a byte that has just been received on the SMBus serial interface. The CPU can read from or write to this register whenever the SI serial interrupt flag (SMB0CN.0) is set to logic one. The serial data in the register remains stable as long as the SI flag is set. When the SI flag is not set, the system may be in the process of shifting data in/out and the CPU should not attempt to access this register.

13.5. SMBus Transfer Modes

The SMBus interface may be configured to operate as master and/or slave. At any particular time, it will be operating in one of the following four modes: Master Transmitter, Master Receiver, Slave Transmitter, or Slave Receiver. The SMBus interface enters Master Mode any time a START is generated, and remains in Master Mode until it loses arbitration or generates a STOP. An SMBus interrupt is generated at the end of all SMBus byte frames; however, note that the interrupt is generated before the ACK cycle when operating as a receiver, and after the ACK cycle when operating as a transmitter.

13.5.1. Master Transmitter Mode

Serial data is transmitted on SDA while the serial clock is output on SCL. The SMBus interface generates the START condition and transmits the first byte containing the address of the target slave and the data direction bit. In this case the data direction bit (R/W) will be logic 0 (WRITE). The master then transmits one or more bytes of serial data. After each byte is transmitted, an acknowledge bit is generated by the slave. The transfer is ended when the STO bit is set and a STOP is generated. Note that the interface will switch to Master Receiver Mode if SMB0DAT is not written following a Master Transmitter interrupt. Figure 13.5 shows a typical Master Transmitter sequence. Two transmit data bytes are shown, though any number of bytes may be transmitted. Notice that the 'data byte transferred' interrupts occur **after** the ACK cycle in this mode.

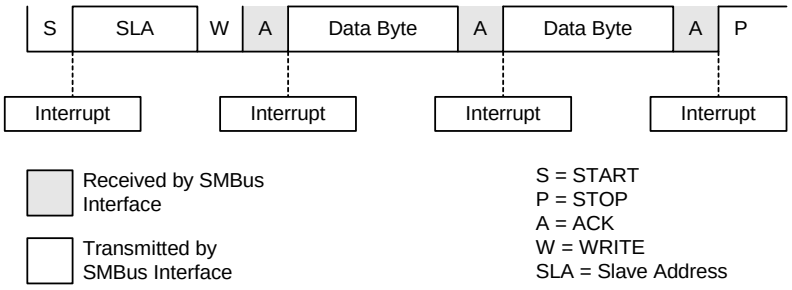

Figure 13.5. Typical Master Transmitter Sequence

SFR Definition 15.9. TMR2RLL: Timer 2 Reload Register Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xCA

Bits 7–0: TMR2RLL: Timer 2 Reload Register Low Byte.
TMR2RLL holds the low byte of the reload value for Timer 2.

SFR Definition 15.10. TMR2RLH: Timer 2 Reload Register High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xCB

Bits 7–0: TMR2RLH: Timer 2 Reload Register High Byte.
The TMR2RLH holds the high byte of the reload value for Timer 2.

SFR Definition 15.11. TMR2L: Timer 2 Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xCC

Bits 7–0: TMR2L: Timer 2 Low Byte.
In 16-bit mode, the TMR2L register contains the low byte of the 16-bit Timer 2. In 8-bit mode, TMR2L contains the 8-bit low byte timer value.

SFR Definition 15.12. TMR2H Timer 2 High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xCD

Bits 7–0: TMR2H: Timer 2 High Byte.
In 16-bit mode, the TMR2H register contains the high byte of the 16-bit Timer 2. In 8-bit mode, TMR2H contains the 8-bit high byte timer value.

16.2.6. 16-Bit Pulse Width Modulator Mode

A PCA module may also be operated in 16-bit PWM mode. In this mode, the 16-bit capture/compare module defines the number of PCA clocks for the low time of the PWM signal. When the PCA counter matches the module contents, the output on CEXn is set to ‘1’; when the counter overflows, CEXn is set to ‘0’. To output a varying duty cycle, new value writes should be synchronized with PCA CCFn match interrupts. 16-bit PWM Mode is enabled by setting the ECOMn, PWMn, and PWM16n bits in the PCA0CPMn register. For a varying duty cycle, match interrupts should be enabled (ECCFn = 1 AND MATn = 1) to help synchronize the capture/compare register writes. The duty cycle for 16-bit PWM Mode is given by Equation 16.3.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to ‘0’; writing to PCA0CPHn sets ECOMn to ‘1’.

$$DutyCycle = \frac{(65536 - PCA0CPn)}{65536}$$

Equation 16.3. 16-Bit PWM Duty Cycle

Using Equation 16.3, the largest duty cycle is 100% (PCA0CPn = 0), and the smallest duty cycle is 0.0015% (PCA0CPn = 0xFFFF). A 0% duty cycle may be generated by clearing the ECOMn bit to ‘0’.

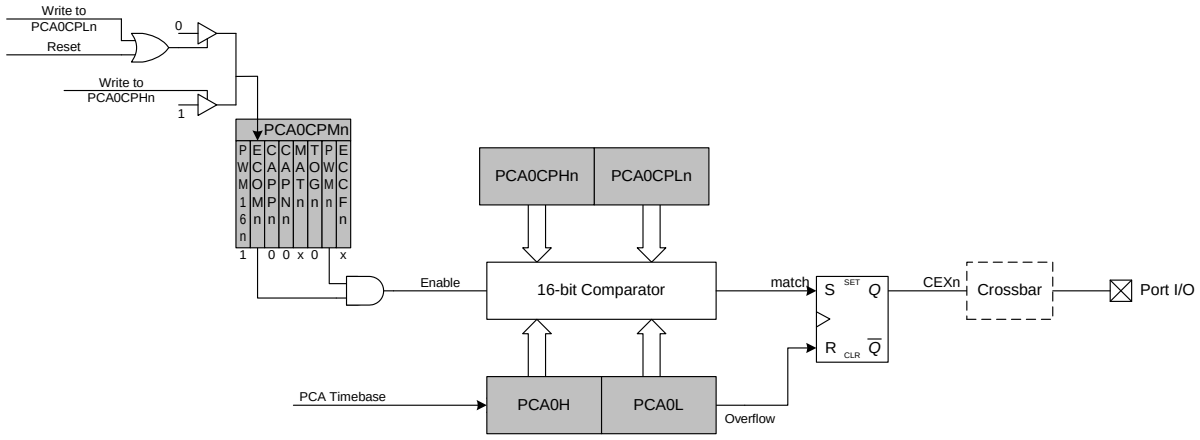

Figure 16.9. PCA 16-Bit PWM Mode

SFR Definition 16.2. PCA0MD: PCA Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CIDL	WDTE	WDLCK	—	CPS2	CPS1	CPS0	ECF	01000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xD9

Bit7: CIDL: PCA Counter/Timer Idle Control.
Specifies PCA behavior when CPU is in Idle Mode.
0: PCA continues to function normally while the system controller is in Idle Mode.
1: PCA operation is suspended while the system controller is in Idle Mode.

Bit6: WDTE: Watchdog Timer Enable
If this bit is set, PCA Module 2 is used as the Watchdog Timer.
0: Watchdog Timer disabled.
1: PCA Module 2 enabled as Watchdog Timer.

Bit5: WDLCK: Watchdog Timer Lock
This bit locks/unlocks the Watchdog Timer Enable. When WDLCK is set, the Watchdog Timer may not be disabled until the next system reset.
0: Watchdog Timer Enable unlocked.
1: Watchdog Timer Enable locked.

Bit4: UNUSED. Read = 0b, Write = don't care.

Bits3–1: CPS2–CPS0: PCA Counter/Timer Pulse Select.
These bits select the clock source for the PCA counter

CPS2	CPS1	CPS0	Timebase
0	0	0	System clock divided by 12
0	0	1	System clock divided by 4
0	1	0	Timer 0 overflow
0	1	1	High-to-low transitions on ECI (max rate = system clock divided by 4)
1	0	0	System clock
1	0	1	External clock divided by 8*
1	1	0	Reserved
1	1	1	Reserved

***Note:** External oscillator source divided by 8 is synchronized with the system clock.

Bit0: ECF: PCA Counter/Timer Overflow Interrupt Enable.
This bit sets the masking of the PCA Counter/Timer Overflow (CF) interrupt.
0: Disable the CF interrupt.
1: Enable a PCA Counter/Timer Overflow interrupt when CF (PCA0CN.7) is set.

Note: When the WDTE bit is set to '1', the PCA0MD register cannot be modified. To change the contents of the PCA0MD register, the Watchdog Timer must first be disabled.

Document Change List

Revision 2.3 to Revision 2.4

- Removed preliminary tag.
- Changed all references of MLP package to QFN package.
- Pinout chapter: Figure 4.3: Changed title to “Typical QFN-11 Solder Paste Mask.”
- ADC chapter: Added reference to minimum tracking time in the Tracking Modes section.
- Comparators chapter: SFR Definition 7.3, CPT0MD: Updated the register reset value and the CP0 response time table.
- CIP51 chapter: Updated IDLE mode and recommendations.
- CIP51 chapter: Updated Interrupt behavior and EA recommendations.
- CIP51 chapter: SFR Definition 8.4, PSW: Clarified OV flag description.
- CIP51 chapter: SFR Definition 8.8, IP register: Changed “default priority order” to “low priority” for low priority descriptions.
- Reset Sources chapter: Clarified description of VDD Ramp Time.
- Reset Sources chapter: Table 9.2, “Reset Electrical Characteristics”: Added VDD Ramp Time and changed “VDD POR Threshold” to “VDD Monitor Threshold.”
- FLASH Memory chapter: Clarified descriptions of FLASH security features.
- Oscillators chapter: Table 11.1 “Internal Oscillator Electrical Characteristics”: Added Calibrated Internal Oscillator specification over a smaller temperature range.
- Oscillators chapter: Clarified external crystal initialization steps and added a specific 32.768 kHz crystal example.
- Oscillators chapter: Clarified external capacitor example.
- SMBus chapter: Figure 14.5, SMB0CF register: Added a description of the behavior of Timer 3 in split mode if SMBTOE is set.
- Timers chapter: Changed references to “TL2” and “TH2” to “TMR2L” and “TMR2H,” respectively.

Revision 2.4 to Revision 2.5

- Fixed variables and applied formatting changes.

Revision 2.5 to Revision 2.6

- Updated Table 1.1 Product Selection Guide to include Lead-free information.

Revision 2.6 to Revision 2.7

- Removed non-RoHS compliant devices from Table 1.1, “Product Selection Guide,” on page 14.
- Added MIN and MAX specifications for ADC Offset Error and ADC Full Scale Error to Table 5.1, “ADC0 Electrical Characteristics,” on page 47.
- Improved power supply specifications in Table 3.1, “Global Electrical Characteristics,” on page 25.
- Added **Section “10.4. Flash Write and Erase Guidelines” on page 94**.
- Fixed minor typographical errors throughout.

Revision 2.7 to Revision 2.8

- Updated block diagram on page 1.

Revision 2.8 to Revision 2.9

- Updated QFN package drawings and notes.
- Added SOIC-14 package information.
- Added text to CPT0CN's SFR definition to indicate that the SFR is bit addressable.
- Changed SMBus maximum transfer speed from 1/10th system clock to 1/20th system clock in SMBus section.
- Added information pertaining to Slave Receiver and Slave Transmitter states in Table 13.4.
- Changed Table 5.1 and Figure 5.4 to indicate that 11 SAR clocks are needed for a SAR conversion to complete.
- Changed SCON0s SFR definition to show that SCON0 bit 6 always resets to a value of 1.