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Details

Product Status	Last Time Buy
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I ² C), UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	8
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f303-gs

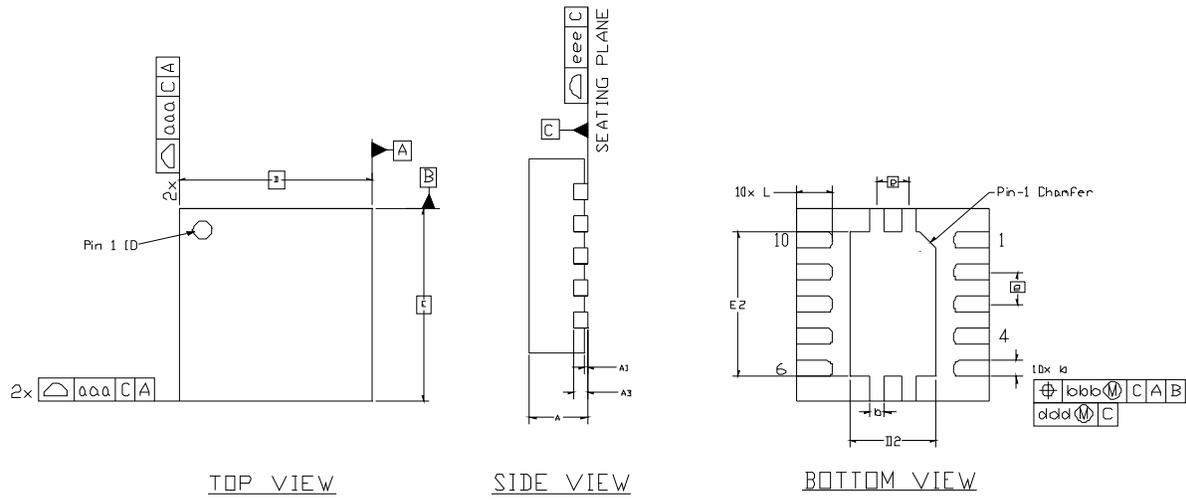


Figure 4.2. QFN-11 Package Drawing

Table 4.2. QFN-11 Package Dimensions

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	0.80	0.90	1.00	E	3.00 BSC.		
A1	0.03	0.07	0.11	E2	2.20	2.25	2.30
A3	0.25 REF			L	.45	.55	.65
b	0.18	0.25	0.30	aaa	--	--	0.15
D	3.00 BSC.			bbb	--	--	0.15
D2	1.30	1.35	1.40	ddd	--	--	0.05
e	0.50 BSC.			eee	--	--	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-243, variation VEED except for custom features D2, E2, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

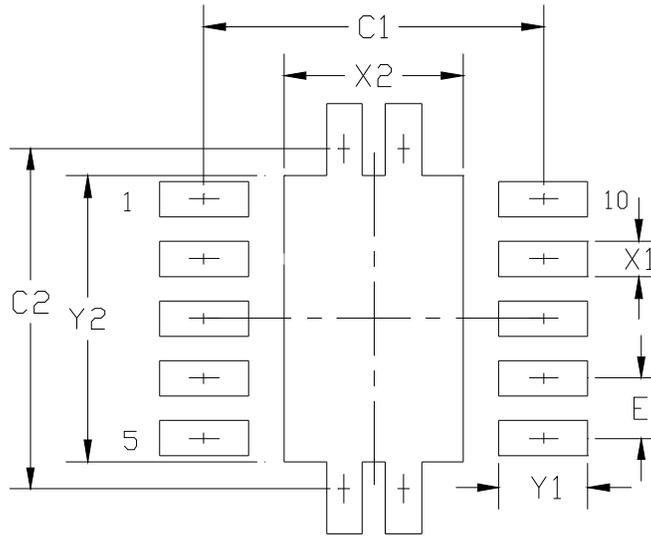


Figure 4.4. Typical QFN-11 Landing Diagram

Table 4.3. QFN-11 Landing Diagram Dimensions

Dimension	MIN	MAX
C1	2.75	2.85
C2	2.75	2.85
E	0.50 BSC	
X1	0.20	0.30
X2	1.40	1.50
Y1	0.65	0.75
Y2	2.30	2.40

Notes: General

- All dimensions shown are in millimeters (mm) unless otherwise noted.
- This land pattern design is based on the IPC-7351 guidelines.

Notes: Solder Mask Design

- All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Notes: Stencil Design

- A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- The stencil thickness should be 0.125 mm (5 mils).
- The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
- A 3 x 1 array of 1.30 x 0.60 mm openings on 0.80 mm pitch should be used for the center ground pad.

Notes: Card Assembly

- A No-Clean, Type-3 solder paste is recommended.
- The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

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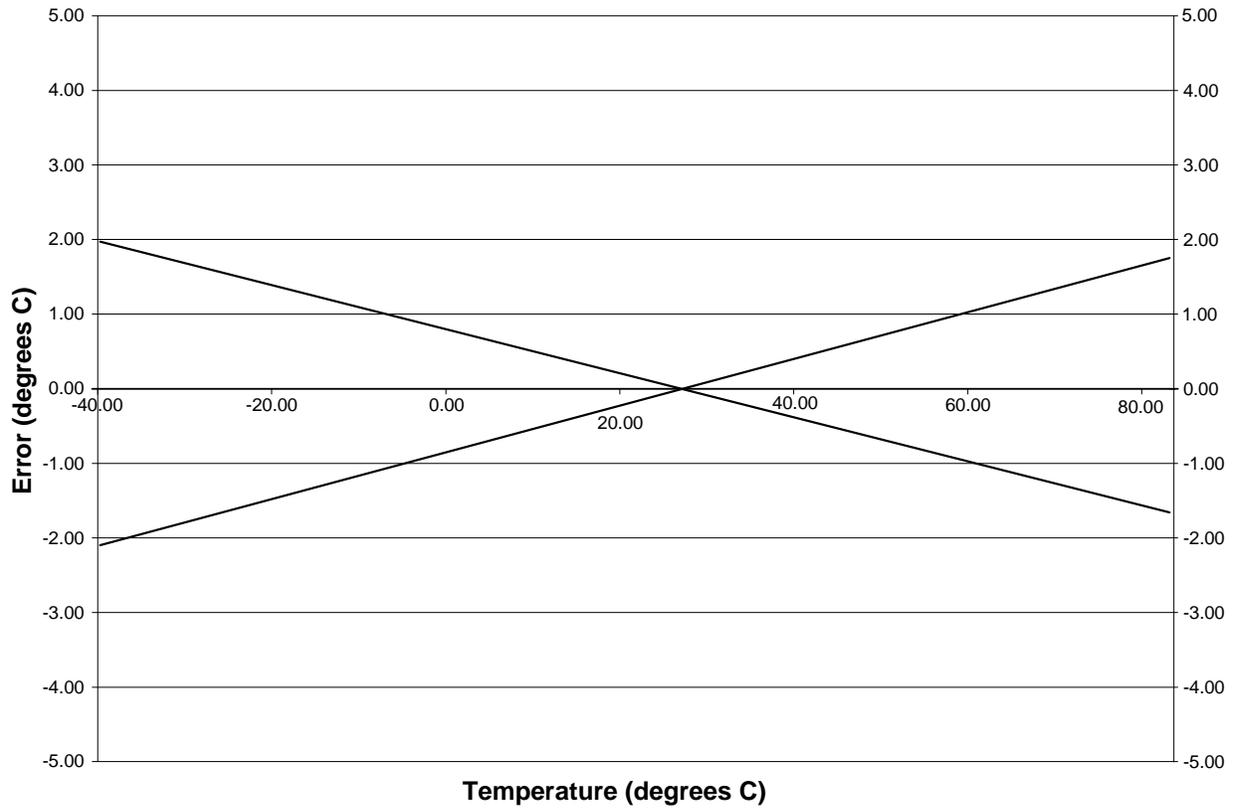


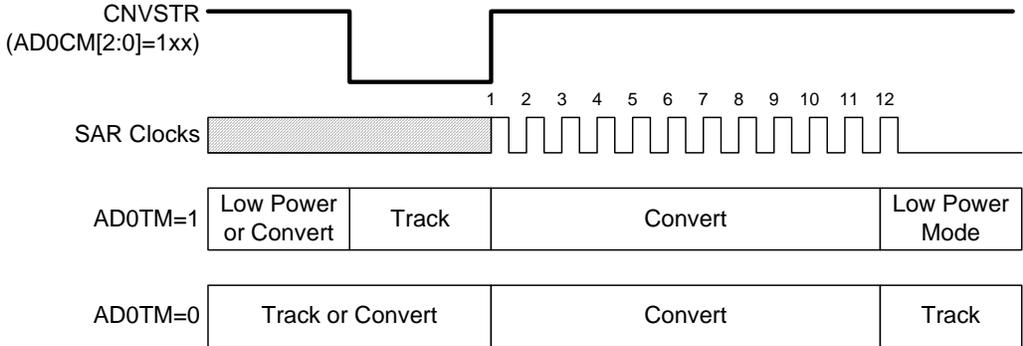
Figure 5.3. Temperature Sensor Error with 1-Point Calibration (VREF = 2.40 V)

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5.3.2. Tracking Modes

According to Table 5.1 on page 47, each ADC0 conversion must be preceded by a minimum tracking time for the converted result to be accurate. The AD0TM bit in register ADC0CN controls the ADC0 track-and-hold mode. In its default state, the ADC0 input is continuously tracked except when a conversion is in progress. When the AD0TM bit is logic 1, ADC0 operates in low-power track-and-hold mode. In this mode, each conversion is preceded by a tracking period of 3 SAR clocks (after the start-of-conversion signal). When the CNVSTR signal is used to initiate conversions in low-power tracking mode, ADC0 tracks only when CNVSTR is low; conversion begins on the rising edge of CNVSTR (see Figure 5.4). Tracking can also be disabled (shutdown) when the device is in low power standby or sleep modes. Low-power track-and-hold mode is also useful when AMUX or PGA settings are frequently changed, due to the settling time requirements described in **Section “5.3.3. Settling Time Requirements” on page 41.**

A. ADC Timing for External Trigger Source



B. ADC Timing for Internal Trigger Source

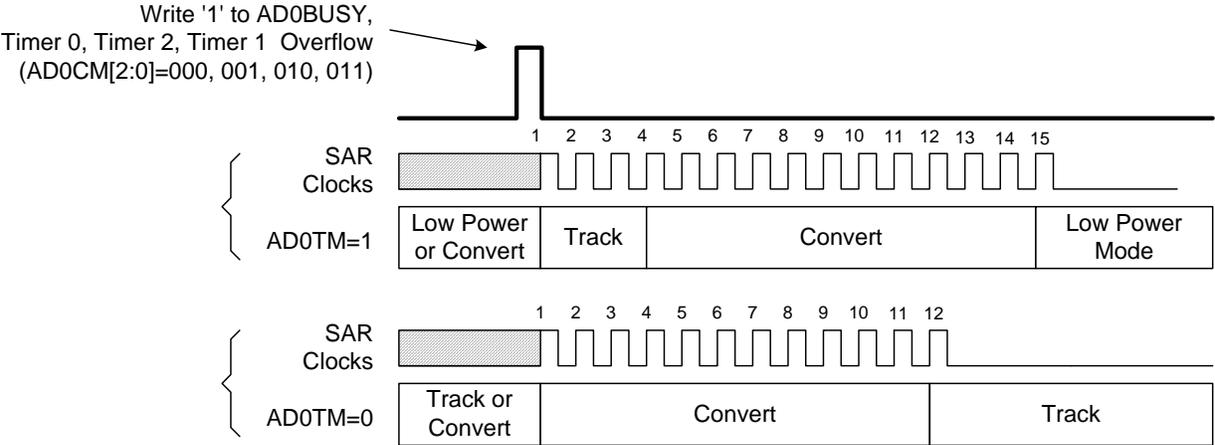


Figure 5.4. 8-Bit ADC Track and Conversion Example Timing

7. Comparator0

C8051F300/1/2/3/4/5 devices include an on-chip programmable voltage comparator, which is shown in Figure 7.1. Comparator0 offers programmable response time and hysteresis, an analog input multiplexer, and two outputs that are optionally available at the Port pins: a synchronous “latched” output (CP0), or an asynchronous “raw” output (CP0A). The asynchronous CP0A signal is available even when the system clock is not active. This allows Comparator0 to operate and generate an output with the device in STOP mode. When assigned to a Port pin, the Comparator0 output may be configured as open drain or push-pull (see Section “12.2. Port I/O Initialization” on page 106). Comparator0 may also be used as a reset source (see Section “9.5. Comparator0 Reset” on page 85).

The inputs for Comparator0 are selected in the CPT0MX register (SFR Definition 7.2). The CMX0P1-CMX0P0 bits select the Comparator0 positive input; the CMX0N1-CMX0N0 bits select the Comparator0 negative input.

Important Note About Comparator Inputs: The Port pins selected as comparator inputs should be configured as analog inputs in their associated Port configuration register, and configured to be skipped by the Crossbar (for details on Port configuration, see Section “12.3. General Purpose Port I/O” on page 108).

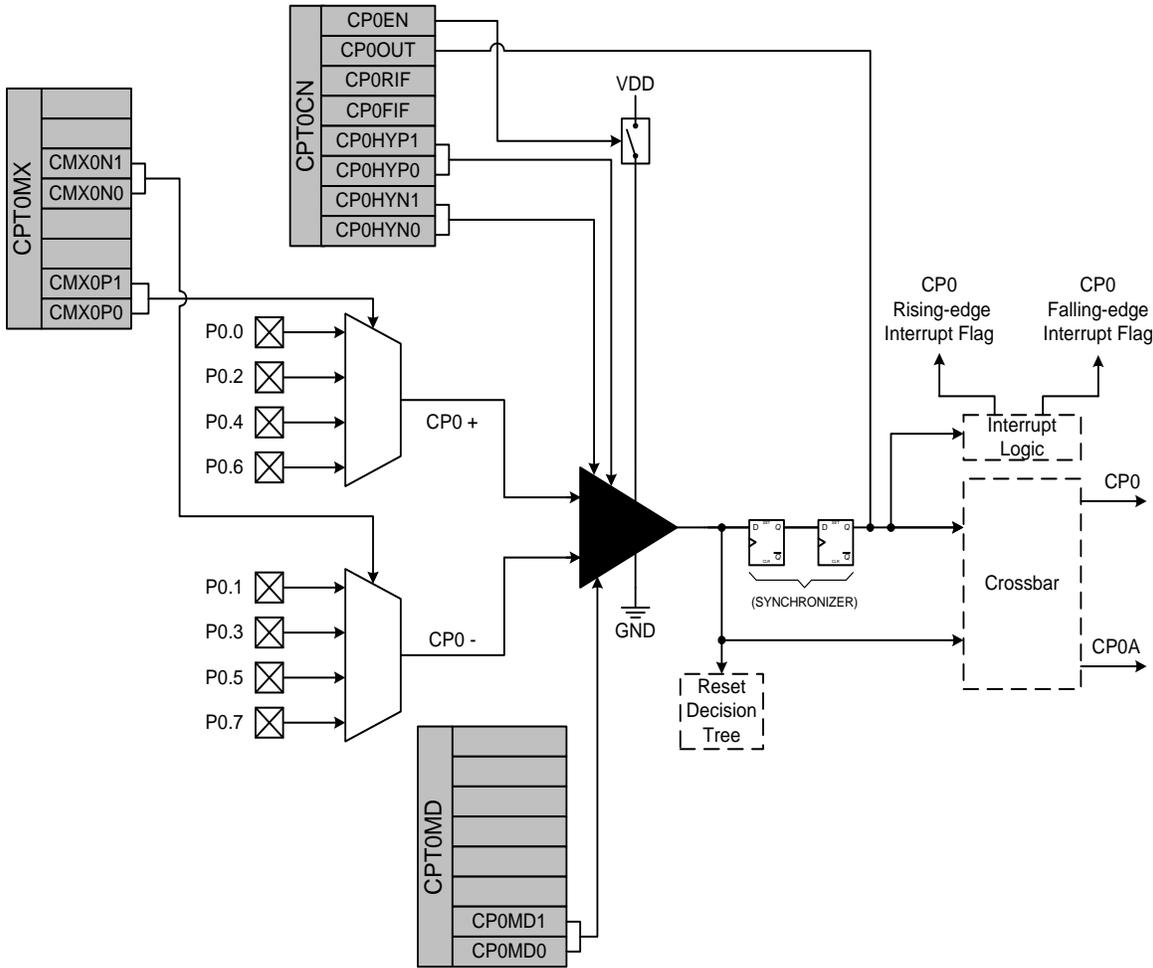


Figure 7.1. Comparator0 Functional Block Diagram

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Performance

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute, and usually have a maximum system clock of 12 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with no instructions taking more than eight system clock cycles.

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS. The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

Programming and Debugging Support

In-system programming of the Flash program memory and communication with on-chip debug support logic is accomplished via the Silicon Labs 2-Wire Development Interface (C2). Note that the re-programmable Flash can also be read and changed a single byte at a time by the application software using the MOVC and MOVX instructions. This feature allows program memory to be used for non-volatile data storage as well as updating program code under software control.

The on-chip debug support logic facilitates full speed in-circuit debugging, allowing the setting of hardware breakpoints, starting, stopping and single stepping through program execution (including interrupt service routines), examination of the program's call stack, and reading/writing the contents of registers and memory. This method of on-chip debugging is completely non-intrusive, requiring no RAM, Stack, timers, or other on-chip resources. C2 details can be found in **Section "17. C2 Interface" on page 173**.

The CIP-51 is supported by development tools from Silicon Labs and third party vendors. Silicon Labs provides an integrated development environment (IDE) including editor, macro assembler, debugger and programmer. The IDE's debugger and programmer interface to the CIP-51 via the C2 interface to provide fast and efficient in-system device programming and debugging. Third party macro assemblers and C compilers are also available.

8.1. Instruction Set

The instruction set of the CIP-51 System Controller is fully compatible with the standard MCS-51™ instruction set. Standard 8051 development tools can be used to develop software for the CIP-51. All CIP-51 instructions are the binary and functional equivalent of their MCS-51™ counterparts, including opcodes, addressing modes and effect on PSW flags. However, instruction timing is different than that of the standard 8051.

8.1.1. Instruction and CPU Timing

In many 8051 implementations, a distinction is made between machine cycles and clock cycles, with machine cycles varying from 2 to 12 clock cycles in length. However, the CIP-51 implementation is based solely on clock cycle timing. All instruction timings are specified in terms of clock cycles.

Due to the pipelined architecture of the CIP-51, most instructions execute in the same number of clock cycles as there are program bytes in the instruction. Conditional branch instructions take one less clock cycle to complete when the branch is not taken as opposed to when the branch is taken. Table 8.1 is the

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Table 8.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
JNZ rel	Jump if A does not equal zero	2	2/3
CJNE A, direct, rel	Compare direct byte to A and jump if not equal	3	3/4
CJNE A, #data, rel	Compare immediate to A and jump if not equal	3	3/4
CJNE Rn, #data, rel	Compare immediate to Register and jump if not equal	3	3/4
CJNE @Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	4/5
DJNZ Rn, rel	Decrement Register and jump if not zero	2	2/3
DJNZ direct, rel	Decrement direct byte and jump if not zero	3	3/4
NOP	No operation	1	1

Notes on Registers, Operands and Addressing Modes:

Rn - Register R0-R7 of the currently selected register bank.

@Ri - Data RAM location addressed indirectly through R0 or R1.

rel - 8-bit, signed (two's complement) offset relative to the first byte of the following instruction. Used by SJMP and all conditional jumps.

direct - 8-bit internal data location's address. This could be a direct-access Data RAM location (0x00-0x7F) or an SFR (0x80-0xFF).

#data - 8-bit constant

#data16 - 16-bit constant

bit - Direct-accessed bit in Data RAM or SFR

addr11 - 11-bit destination address used by ACALL and AJMP. The destination must be within the same 2K-byte page of program memory as the first byte of the following instruction.

addr16 - 16-bit destination address used by LCALL and LJMP. The destination may be anywhere within the 8K-byte program memory space.

There is one unused opcode (0xA5) that performs the same function as NOP.

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Table 8.3. Special Function Registers* (Continued)

Register	Address	Description	Page No.
TH1	0x8D	Timer/Counter 1 High	150
TL0	0x8A	Timer/Counter 0 Low	150
TL1	0x8B	Timer/Counter 1 Low	150
TMOD	0x89	Timer/Counter Mode	148
TMR2RLH	0xCB	Timer/Counter 2 Reload High	154
TMR2RLL	0xCA	Timer/Counter 2 Reload Low	154
TMR2H	0xCD	Timer/Counter 2 High	154
TMR2L	0xCC	Timer/Counter 2 Low	154
XBR0	0xE1	Port I/O Crossbar Control 0	107
XBR1	0xE2	Port I/O Crossbar Control 1	107
XBR2	0xE3	Port I/O Crossbar Control 2	108
0x97, 0xAE, 0xAF, 0xB4, 0xB6, 0xBF, 0xCE, 0xD2, 0xD3, 0xD4, 0xD5, 0xD6, 0xD7, 0xDD, 0xDE, 0xDF, 0xF5		Reserved	
*Note: SFRs are listed in alphabetical order. All undefined SFR locations are reserved			

8.2.7. Register Descriptions

Following are descriptions of SFRs related to the operation of the CIP-51 System Controller. Reserved bits should not be set to logic 1. Future product versions may use these bits to implement new features in which case the reset value of the bit will be logic 0, selecting the feature's default state. Detailed descriptions of the remaining SFRs are included in the sections of the datasheet associated with their corresponding system function.

SFR Definition 8.1. DPL: Data Pointer Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x82
<p>Bits7–0: DPL: Data Pointer Low. The DPL register is the low byte of the 16-bit DPTR. DPTR is used to access indirectly addressed Flash memory.</p>								

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10.1.3. Flash Write Procedure

Flash bytes are programmed by software with the following sequence:

- Step 1. Disable interrupts (recommended).
- Step 2. Erase the 512-byte Flash page containing the target location, as described in **Section 10.1.2**.
- Step 3. Set the PSWE bit in PSCTL.
- Step 4. Clear the PSEE bit in PSCTL.
- Step 5. Write the first key code to FLKEY: 0xA5.
- Step 6. Write the second key code to FLKEY: 0xF1.
- Step 7. Using the MOVX instruction, write a single data byte to the desired location within the 512-byte sector.

Steps 5–7 must be repeated for each byte to be written. After Flash writes are complete, PSWE should be cleared so that MOVX instructions do not target program memory. Writing to and erasing the Reserved area of Flash should be avoided.

Table 10.1. Flash Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Flash Size	C8051F300/1/2/3	8192*			bytes
	C8051F304	4096			bytes
	C8051F305	2048			bytes
Endurance		20k	100k		Erase/Write
Erase Cycle Time	25 MHz System Clock	10	15	20	ms
Write Cycle Time	25 MHz System Clock	40	55	70	µs
SYSCLK Frequency (Flash writes from application code)		100			kHz

***Note:** 512 bytes at location 0x1E00 to 0x1FFF are reserved.

10.2. Non-Volatile Data Storage

The Flash memory can be used for non-volatile data storage as well as program code. This allows data such as calibration coefficients to be calculated and stored at run time. Data is written using the MOVX instruction and read using the MOVC instruction.

10.3. Security Options

The CIP-51 provides security options to protect the Flash memory from inadvertent modification by software as well as to prevent the viewing of proprietary program code and constants. The Program Store Write Enable (bit PSWE in register PSCTL) and the Program Store Erase Enable (bit PSEE in register PSCTL) bits protect the Flash memory from accidental modification by software. PSWE must be explicitly set to '1' before software can modify the Flash memory; both PSWE and PSEE must be set to '1' before software can erase Flash memory. Additional security features prevent proprietary program code and data constants from being read or altered across the C2 interface.

A security lock byte stored at the last byte of Flash user space protects the Flash program memory from being read or altered across the C2 interface. See Table 10.2 for the security byte description; see Figure 10.1 for a program memory map and the security byte locations for each device.

11.4. External Crystal Example

If a crystal or ceramic resonator is used as an external oscillator source for the MCU, the circuit should be configured as shown in Figure 11.1, Option 1. The External Oscillator Frequency Control value (XFCN) should be chosen from the Crystal column of the table in SFR Definition 11.3 (OSCXCN register). For example, an 11.0592 MHz crystal requires an XFCN setting of 111b.

When the crystal oscillator is first enabled, the oscillator amplitude detection circuit requires a settling time to achieve proper bias. Introducing a delay of 1 ms between enabling the oscillator and checking the XTLVLD bit will prevent a premature switch to the external oscillator as the system clock. Switching to the external oscillator before the crystal oscillator has stabilized can result in unpredictable behavior. The recommended procedure is:

- Step 1. Force the XTAL1 and XTAL2 pins low by writing 0's to the port latch.
- Step 2. Configure XTAL1 and XTAL2 as analog inputs.
- Step 3. Enable the external oscillator.
- Step 4. Wait at least 1 ms.
- Step 5. Poll for XTLVLD => '1'.
- Step 6. Switch the system clock to the external oscillator.

Note: Tuning-fork crystals may require additional settling time before XTLVLD returns a valid result.

The capacitors shown in the external crystal configuration provide the load capacitance required by the crystal for correct oscillation. These capacitors are “in series” as seen by the crystal and “in parallel” with the stray capacitance of the XTAL1 and XTAL2 pins.

Note: The load capacitance depends upon the crystal and the manufacturer. Please refer to the crystal data sheet when completing these calculations.

For example, a tuning-fork crystal of 32.768 kHz with a recommended load capacitance of 12.5 pF should use the configuration shown in Figure 12.1, Option 1. The total value of the capacitors and the stray capacitance of the XTAL pins should equal 25 pF. With a stray capacitance of 3 pF per pin, the 22 pF capacitors yield an equivalent capacitance of 12.5 pF across the crystal, as shown in Figure 11.2.

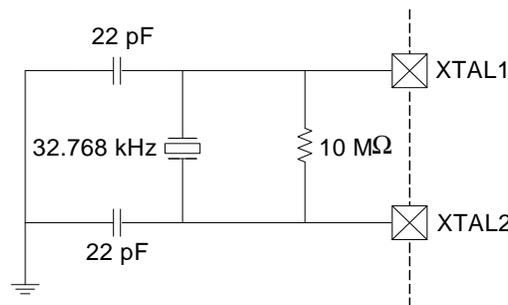


Figure 11.2. 32.768 kHz External Crystal Example

12. Port Input/Output

Digital and analog resources are available through a byte-wide digital I/O Port, Port0. Each of the Port pins can be defined as general-purpose I/O (GPIO), analog input, or assigned to one of the internal digital resources as shown in Figure 12.3. The designer has complete control over which functions are assigned, limited only by the number of physical I/O pins. This resource assignment flexibility is achieved through the use of a Priority Crossbar Decoder. Note that the state of a Port I/O pin can always be read in the corresponding Port latch, regardless of the Crossbar settings.

The Crossbar assigns the selected internal digital resources to the I/O pins based on the Priority Decoder (Figure 12.3 and Figure 12.4). The registers XBR0, XBR1, and XBR2, defined in SFR Definition 12.1, SFR Definition 12.2, and SFR Definition 12.3 are used to select internal digital functions.

All Port I/Os are 5 V tolerant (refer to Figure 12.2 for the Port cell circuit). The Port I/O cells are configured as either push-pull or open-drain in the Port0 Output Mode register (P0MDOUT). Complete Electrical Specifications for Port I/O are given in Table 12.1 on page 110.

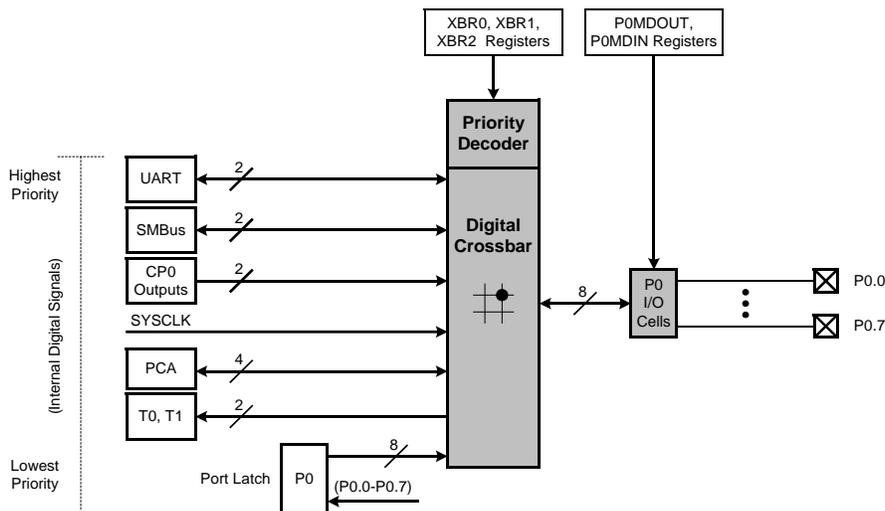


Figure 12.1. Port I/O Functional Block Diagram

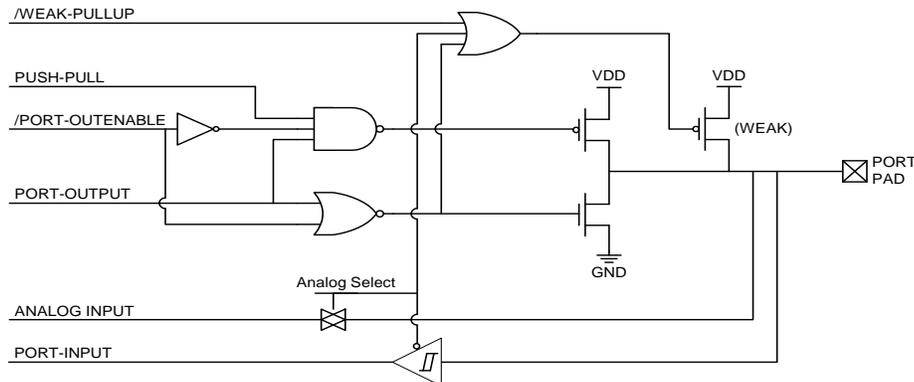
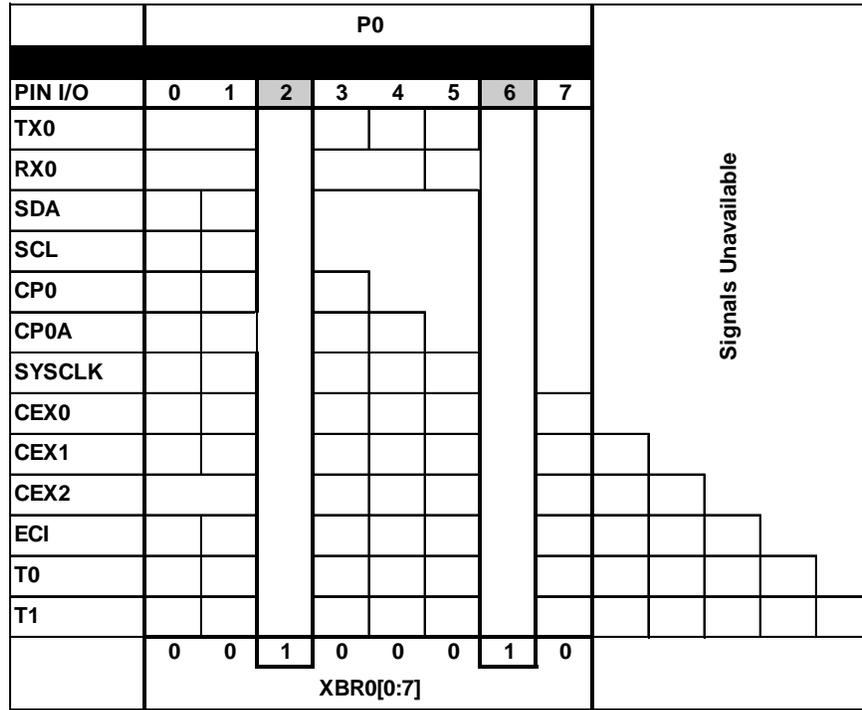


Figure 12.2. Port I/O Cell Block Diagram



Port pin potentially available to peripheral
 Port pin skipped by CrossBar
SF Signals Special Function Signals are not assigned by the crossbar. When these signals are enabled, the CrossBar must be manually configured to skip their corresponding port pins. Note: x1 refers to the XTAL1 signal; x2 refers to the XTAL2 signal.

Figure 12.4. Crossbar Priority Decoder with XBR0 = 0x44

Registers XBR1 and XBR2 are used to assign the digital I/O resources to the physical I/O Port pins. Note that when the SMBus is selected, the Crossbar assigns both pins associated with the SMBus (SDA and SCL). Either or both of the UART signals may be selected by the Crossbar. UART0 pin assignments are fixed for bootloading purposes: when UART TX0 is selected, it is always assigned to P0.4; when UART RX0 is selected, it is always assigned to P0.5. Standard Port I/Os appear contiguously after the prioritized functions have been assigned. For example, if assigned functions that take the first 3 Port I/O (P0.[2:0]), 5 Port I/O are left for analog or GPIO use.

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13.1. Supporting Documents

It is assumed the reader is familiar with or has access to the following supporting documents:

1. The I²C-Bus and How to Use It (including specifications), Philips Semiconductor.
2. The I²C-Bus Specification – Version 2.0, Philips Semiconductor.
3. System Management Bus Specification – Version 1.1, SBS Implementers Forum.

13.2. SMBus Configuration

Figure 13.2 shows a typical SMBus configuration. The SMBus specification allows any recessive voltage between 3.0 and 5.0 V; different devices on the bus may operate at different voltage levels. The bidirectional SCL (serial clock) and SDA (serial data) lines must be connected to a positive power supply voltage through a pull-up resistor or similar circuit. Every device connected to the bus must have an open-drain or open-collector output for both the SCL and SDA lines, so that both are pulled high (recessive state) when the bus is free. The maximum number of devices on the bus is limited only by the requirement that the rise and fall times on the bus not exceed 300 ns and 1000 ns, respectively.

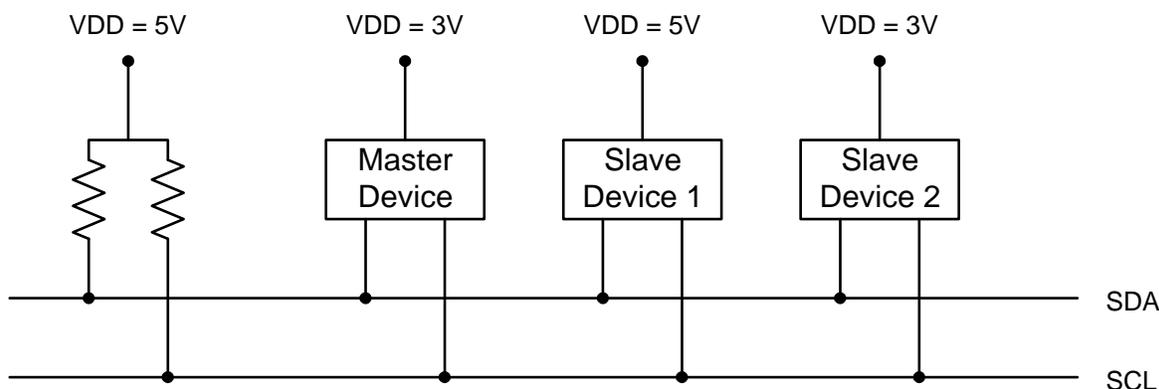


Figure 13.2. Typical SMBus Configuration

13.3. SMBus Operation

Two types of data transfers are possible: data transfers from a master transmitter to an addressed slave receiver (WRITE), and data transfers from an addressed slave transmitter to a master receiver (READ). The master device initiates both types of data transfers and provides the serial clock pulses on SCL. The SMBus interface may operate as a master or a slave, and multiple master devices on the same bus are supported. If two or more masters attempt to initiate a data transfer simultaneously, an arbitration scheme is employed with a single master always winning the arbitration. Note that it is not necessary to specify one device as the Master in a system; any device that transmits a START and a slave address becomes the master for the duration of that transfer.

A typical SMBus transaction consists of a START condition followed by an address byte (Bits7–1: 7-bit slave address; Bit0: R/W direction bit), one or more bytes of data, and a STOP condition. Each byte that is received (by a master or slave) must be acknowledged (ACK) with a low SDA during a high SCL (see Figure 13.3). If the receiving device does not ACK, the transmitting device will read a NACK (not acknowledge), which is a high SDA during a high SCL.

13.4.1. SMBus Configuration Register

The SMBus Configuration register (SMB0CF) is used to enable the SMBus Master and/or Slave modes, select the SMBus clock source, and select the SMBus timing and timeout options. When the ENSMB bit is set, the SMBus is enabled for all master and slave events. Slave events may be disabled by setting the INH bit. With slave events inhibited, the SMBus interface will still monitor the SCL and SDA pins; however, the interface will NACK all received addresses and will not generate any slave interrupts. When the INH bit is set, all slave events will be inhibited following the next START (interrupts will continue for the duration of the current transfer).

Table 13.1. SMBus Clock Source Selection

SMBCS1	SMBCS0	SMBus Clock Source
0	0	Timer 0 Overflow
0	1	Timer 1 Overflow
1	0	Timer 2 High Byte Overflow
1	1	Timer 2 Low Byte Overflow

The SMBCS1-0 bits select the SMBus clock source, which is used only when operating as a master or when the Free Timeout detection is enabled. When operating as a master, overflows from the selected source determine the absolute minimum SCL low and high times as defined in Equation 13.1. Note that the selected clock source may be shared by other peripherals so long as the timer is left running at all times. For example, Timer 1 overflows may generate the SMBus and UART baud rates simultaneously. Timer configuration is covered in **Section “15. Timers” on page 143**.

$$T_{HighMin} = T_{LowMin} = \frac{1}{f_{ClockSourceOverflow}}$$

Equation 13.1. Minimum SCL High and Low Times

The selected clock source should be configured to establish the minimum SCL High and Low times as per Equation 13.1. When the interface is operating as a master (and SCL is not driven or extended by any other devices on the bus), the typical SMBus bit rate is approximated by Equation 13.2.

$$BitRate = \frac{f_{ClockSourceOverflow}}{3}$$

Equation 13.2. Typical SMBus Bit Rate

Figure 13.4 shows the typical SCL generation described by Equation 13.2. Notice that T_{HIGH} is typically twice as large as T_{LOW} . The actual SCL output may vary due to other devices on the bus (SCL may be extended low by slower slave devices, or driven low by contending master devices). The bit rate when operating as a master will never exceed the limits defined by equation Equation 13.1.

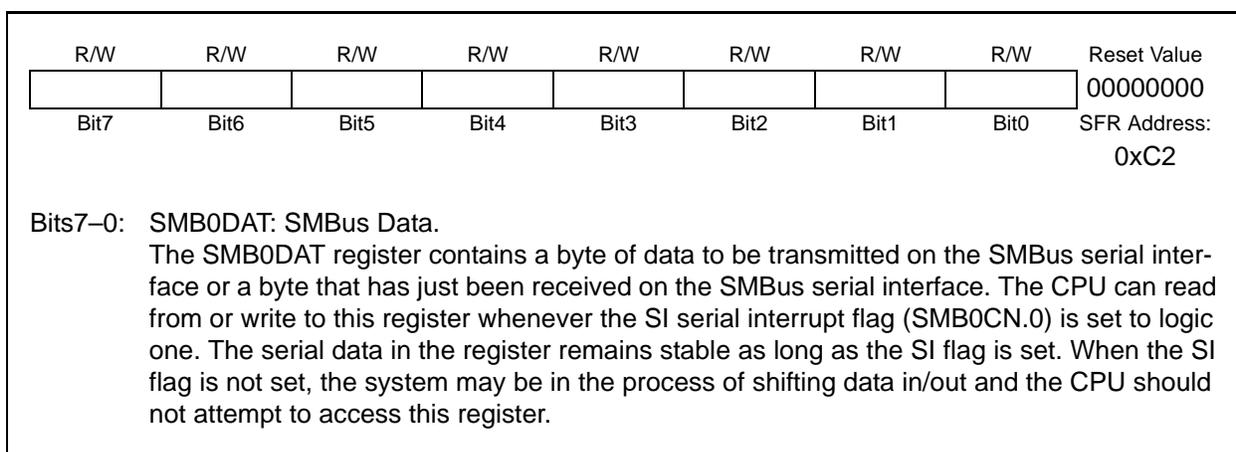
C8051F300/1/2/3/4/5

13.4.3. Data Register

The SMBus Data register SMB0DAT holds a byte of serial data to be transmitted or one that has just been received. Software may safely read or write to the data register when the SI flag is set. Software should not attempt to access the SMB0DAT register when the SMBus is enabled and the SI flag is cleared to logic 0, as the interface may be in the process of shifting a byte of data into or out of the register.

Data in SMB0DAT is always shifted out MSB first. After a byte has been received, the first bit of received data is located at the MSB of SMB0DAT. While data is being shifted out, data on the bus is simultaneously being shifted in. SMB0DAT always contains the last data byte present on the bus. In the event of lost arbitration, the transition from master transmitter to slave receiver is made with the correct data or address in SMB0DAT.

SFR Definition 13.3. SMB0DAT: SMBus Data



SFR Definition 15.3. CKCON: Clock Control

R/W	Reset Value							
—	T2MH	T2ML	T1M	T0M	—	SCA1	SCA0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x8E

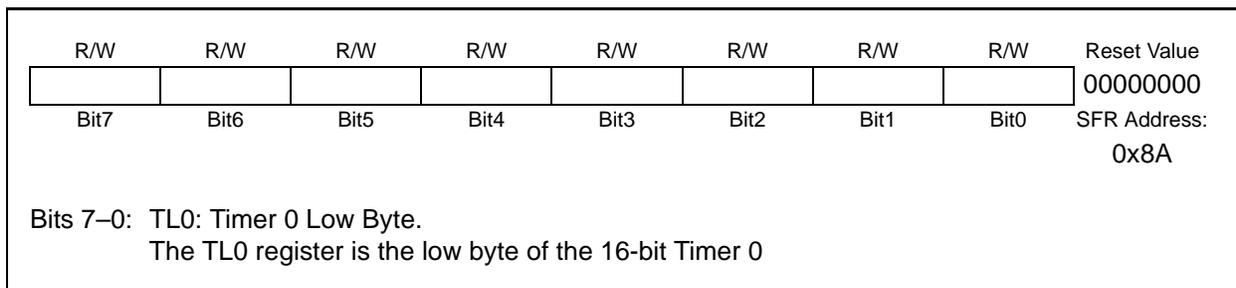
- Bit7: UNUSED. Read = 0b, Write = don't care.
- Bit6: T2MH: Timer 2 High Byte Clock Select
This bit selects the clock supplied to the Timer 2 high byte if Timer 2 is configured in split 8-bit timer mode. T2MH is ignored if Timer 2 is in any other mode.
0: Timer 2 high byte uses the clock defined by the T2XCLK bit in TMR2CN.
1: Timer 2 high byte uses the system clock.
- Bit5: T2ML: Timer 2 Low Byte Clock Select
This bit selects the clock supplied to Timer 2. If Timer 2 is configured in split 8-bit timer mode, this bit selects the clock supplied to the lower 8-bit timer.
0: Timer 2 low byte uses the clock defined by the T2XCLK bit in TMR2CN.
1: Timer 2 low byte uses the system clock.
- Bit4: T1M: Timer 1 Clock Select.
This select the clock source supplied to Timer 1. T1M is ignored when C/T1 is set to logic 1.
0: Timer 1 uses the clock defined by the prescale bits, SCA1–SCA0.
1: Timer 1 uses the system clock.
- Bit3: T0M: Timer 0 Clock Select.
This bit selects the clock source supplied to Timer 0. T0M is ignored when C/T0 is set to logic 1.
0: Counter/Timer 0 uses the clock defined by the prescale bits, SCA1–SCA0.
1: Counter/Timer 0 uses the system clock.
- Bit2: UNUSED. Read = 0b, Write = don't care.
- Bits1–0: SCA1–SCA0: Timer 0/1 Prescale Bits
These bits control the division of the clock supplied to Timer 0 and/or Timer 1 if configured to use prescaled clock inputs.

SCA1	SCA0	Prescaled Clock
0	0	System clock divided by 12
0	1	System clock divided by 4
1	0	System clock divided by 48
1	1	External clock divided by 8

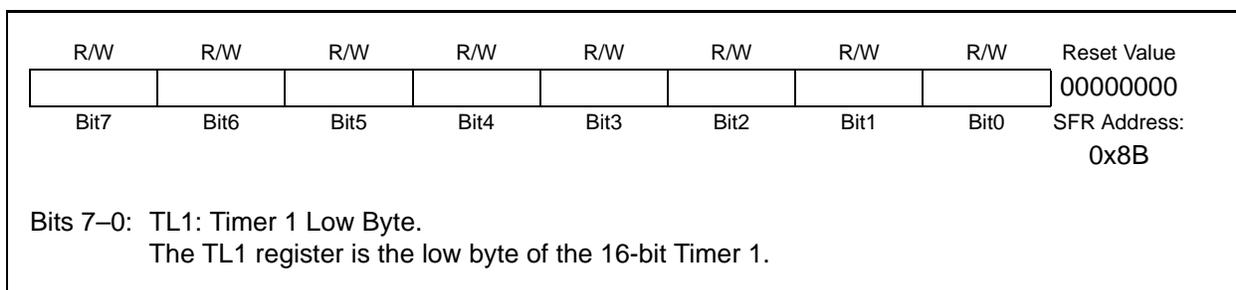
Note: External clock divided by 8 is synchronized with the system clock, and the external clock must be less than or equal to the system clock to operate in this mode.

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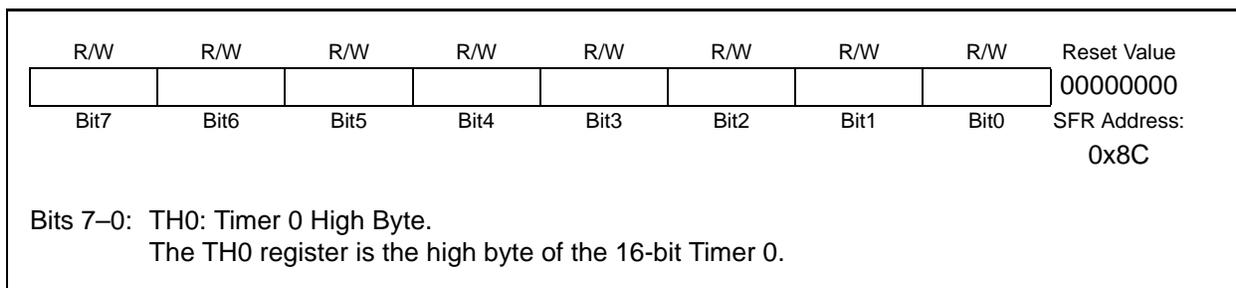
SFR Definition 15.4. TL0: Timer 0 Low Byte



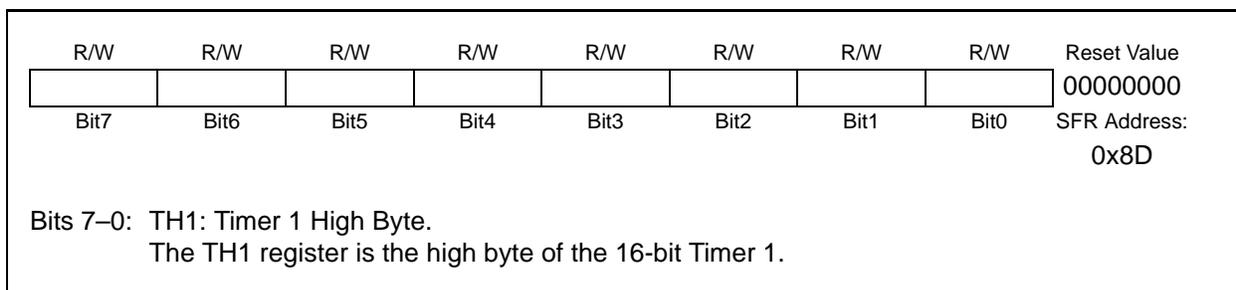
SFR Definition 15.5. TL1: Timer 1 Low Byte



SFR Definition 15.6. TH0: Timer 0 High Byte



SFR Definition 15.7. TH1: Timer 1 High Byte



16.2.6. 16-Bit Pulse Width Modulator Mode

A PCA module may also be operated in 16-bit PWM mode. In this mode, the 16-bit capture/compare module defines the number of PCA clocks for the low time of the PWM signal. When the PCA counter matches the module contents, the output on CEXn is set to '1'; when the counter overflows, CEXn is set to '0'. To output a varying duty cycle, new value writes should be synchronized with PCA CCFn match interrupts. 16-bit PWM Mode is enabled by setting the ECOMn, PWMn, and PWM16n bits in the PCA0CPMn register. For a varying duty cycle, match interrupts should be enabled (ECCFn = 1 AND MATn = 1) to help synchronize the capture/compare register writes. The duty cycle for 16-bit PWM Mode is given by Equation 16.3.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to '0'; writing to PCA0CPHn sets ECOMn to '1'.

$$DutyCycle = \frac{(65536 - PCA0CPn)}{65536}$$

Equation 16.3. 16-Bit PWM Duty Cycle

Using Equation 16.3, the largest duty cycle is 100% (PCA0CPn = 0), and the smallest duty cycle is 0.0015% (PCA0CPn = 0xFFFF). A 0% duty cycle may be generated by clearing the ECOMn bit to '0'.

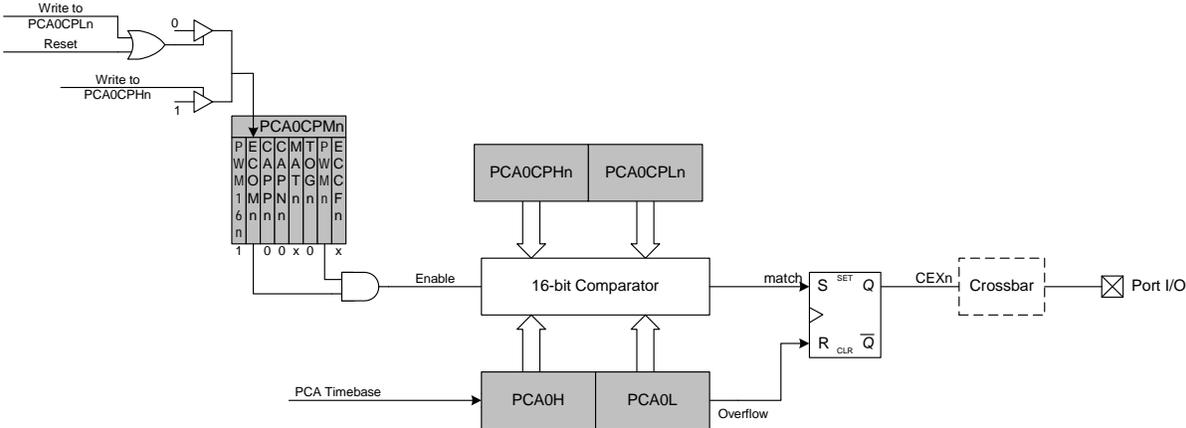


Figure 16.9. PCA 16-Bit PWM Mode

Note that the 8-bit offset held in PCA0CPH2 is compared to the upper byte of the 16-bit PCA counter. This offset value is the number of PCA0L overflows before a reset. Up to 256 PCA clocks may pass before the first PCA0L overflow occurs, depending on the value of the PCA0L when the update is performed. The total offset is then given (in PCA clocks) by Equation 16.4, where PCA0L is the value of the PCA0L register at the time of the update.

$$\text{Offset} = (256 \times \text{PCA0CPL2}) + (256 - \text{PCA0L})$$

Equation 16.4. Watchdog Timer Offset in PCA Clocks

The WDT reset is generated when PCA0L overflows while there is a match between PCA0CPH2 and PCA0H. Software may force a WDT reset by writing a '1' to the CCF2 flag (PCA0CN.2) while the WDT is enabled.

16.3.2. Watchdog Timer Usage

To configure the WDT, perform the following tasks:

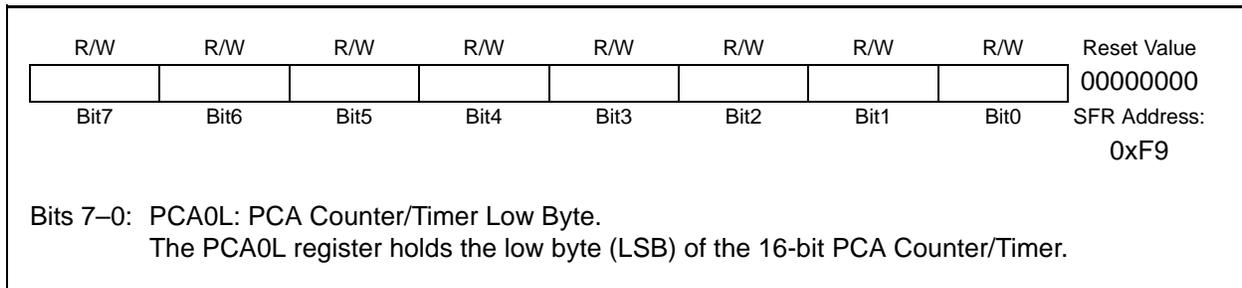
- Disable the WDT by writing a '0' to the WDTE bit.
- Select the desired PCA clock source (with the CPS2–CPS0 bits).
- Load PCA0CPL2 with the desired WDT update offset value.
- Configure the PCA Idle mode (set CIDL if the WDT should be suspended while the CPU is in Idle mode).
- Enable the WDT by setting the WDTE bit to '1'.
- Reload the WDT by writing any value to PCA0CPH2.

The PCA clock source and Idle mode select cannot be changed while the WDT is enabled. The Watchdog Timer is enabled by setting the WDTE or WDLCK bits in the PCA0MD register. When WDLCK is set, the WDT cannot be disabled until the next system reset. If WDLCK is not set, the WDT is disabled by clearing the WDTE bit.

The WDT is enabled following any reset. The PCA0 counter clock defaults to the system clock divided by 12, PCA0L defaults to 0x00, and PCA0CPL2 defaults to 0x00. Using Equation 16.4, this results in a WDT timeout interval of 3072 system clock cycles. Table 16.3 lists some example timeout intervals for typical system clocks, assuming SYSCLK / 12 as the PCA clock source.

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SFR Definition 16.4. PCA0L: PCA Counter/Timer Low Byte



SFR Definition 16.5. PCA0H: PCA Counter/Timer High Byte

