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## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

| Details | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | Dual ARM® Cortex®-A9 MPCore™ with CoreSight™ |
| Flash Size | - |
| RAM Size | 256KB |
| Peripherals | DMA |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG |
| Speed | 800MHz |
| Primary Attributes | Kintex™-7 FPGA, 444K Logic Cells |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 900-BBGA, FCBGA |
| Supplier Device Package | 900-FCBGA (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc7z100-2ffg900i |

*Table 3:* **DC Characteristics Over Recommended Operating Conditions**

| Symbol | Description | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|
| $V_{DRINT}$ | Data retention $V_{CCINT}$ voltage (below which configuration data might be lost) | 0.75 | – | – | V |
| $V_{DRI}$ | Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost) | 1.5 | – | – | V |
| $I_{REF}$ | $V_{REF}$ leakage current per pin | – | – | 15 | µA |
| $I_L$ | Input or output leakage current per pin (sample-tested) | – | – | 15 | µA |
| $C_{IN}$[2] | PL die input capacitance at the pad | – | – | 8 | pF |
| $C_{PIN}$[2] | PS die input capacitance at the pad | – | – | 8 | pF |
| $I_{RPU}$ | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 3.3V | 90 | – | 330 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 2.5V | 68 | – | 250 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.8V | 34 | – | 220 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.5V | 23 | – | 150 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.2V | 12 | – | 120 | µA |
| $I_{RPD}$ | Pad pull-down (when selected) @ $V_{IN}$ = 3.3V | 68 | – | 330 | µA |
| | Pad pull-down (when selected) @ $V_{IN}$ = 1.8V | 45 | – | 180 | µA |
| $I_{CCADC}$ | Analog supply current, analog circuits in powered up state | – | – | 25 | mA |
| $I_{BATT}$[3] | Battery supply current | – | – | 150 | nA |
| $R_{IN\_TERM}$[4] | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_40) for commercial (C), industrial (I), and extended (E) temperature devices | 28 | 40 | 55 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_50) for commercial (C), industrial (I), and extended (E) temperature devices | 35 | 50 | 65 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_60) for commercial (C), industrial (I), and extended (E) temperature devices | 44 | 60 | 83 | Ω |
| n | Temperature diode ideality factor | – | 1.010 | – | – |
| r | Temperature diode series resistance | – | 2 | – | Ω |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}$/2 level.

# DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $I_{OL}$ and $I_{OH}$ are guaranteed over the recommended operating conditions at the $V_{OL}$ and $V_{OH}$ test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum $V_{CCO}$ with the respective $V_{OL}$ and $V_{OH}$ voltage levels shown. Other standards are sample tested.

## PS I/O Levels

*Table 9:* **PS DC Input and Output Levels**(1)

| Bank | I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|---|
| | | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| MIO | LVCMOS18 | –0.300 | 35% $V_{CCO\_MIO}$ | 65% $V_{CCO\_MIO}$ | $V_{CCO\_MIO}$ + 0.300 | 0.450 | $V_{CCO\_MIO}$ – 0.450 | 8 | –8 |
| MIO | LVCMOS25 | –0.300 | 0.700 | 1.700 | $V_{CCO\_MIO}$ + 0.300 | 0.400 | $V_{CCO\_MIO}$ – 0.400 | 8 | –8 |
| MIO | LVCMOS33 | –0.300 | 0.800 | 2.000 | 3.450 | 0.400 | $V_{CCO\_MIO}$ – 0.400 | 8 | –8 |
| MIO | HSTL_I_18 | –0.300 | $V_{PREF}$ – 0.100 | $V_{PREF}$ + 0.100 | $V_{CCO\_MIO}$ + 0.300 | 0.400 | $V_{CCO\_MIO}$ – 0.400 | 8 | –8 |
| DDR | SSTL18_I | –0.300 | $V_{PREF}$ – 0.125 | $V_{PREF}$ + 0.125 | $V_{CCO\_DDR}$ + 0.300 | $V_{CCO\_DDR}$/2 – 0.470 | $V_{CCO\_DDR}$/2 + 0.470 | 8 | –8 |
| DDR | SSTL15 | –0.300 | $V_{PREF}$ – 0.100 | $V_{PREF}$ + 0.100 | $V_{CCO\_DDR}$ + 0.300 | $V_{CCO\_DDR}$/2 – 0.175 | $V_{CCO\_DDR}$/2 + 0.175 | 13.0 | –13.0 |
| DDR | SSTL135 | –0.300 | $V_{PREF}$ – 0.090 | $V_{PREF}$ + 0.090 | $V_{CCO\_DDR}$ + 0.300 | $V_{CCO\_DDR}$/2 – 0.150 | $V_{CCO\_DDR}$/2 + 0.150 | 13.0 | –13.0 |
| DDR | HSUL_12 | –0.300 | $V_{PREF}$ – 0.130 | $V_{PREF}$ + 0.130 | $V_{CCO\_DDR}$ + 0.300 | 20% $V_{CCO\_DDR}$ | 80% $V_{CCO\_DDR}$ | 0.1 | –0.1 |

**Notes:**

1. Tested according to relevant specifications.

*Table 10:* **PS Complementary Differential DC Input and Output Levels**

| Bank | I/O Standard | $V_{ICM}$(1) | | | $V_{ID}$(2) | | $V_{OL}$(3) | $V_{OH}$(4) | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| | | V, Min | V,Typ | V, Max | V,Min | V, Max | V, Max | V, Min | mA, Max | mA, Min |
| DDR | DIFF_HSUL_12 | 0.300 | 0.600 | 0.850 | 0.100 | – | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.100 | –0.100 |
| DDR | DIFF_SSTL135 | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO\_DDR}$/2) – 0.150 | ($V_{CCO\_DDR}$/2) + 0.150 | 13.0 | –13.0 |
| DDR | DIFF_SSTL15 | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO\_DDR}$/2) – 0.175 | ($V_{CCO\_DDR}$/2) + 0.175 | 13.0 | –13.0 |
| DDR | DIFF_SSTL18_I | 0.300 | 0.900 | 1.425 | 0.100 | – | ($V_{CCO\_DDR}$/2) – 0.470 | ($V_{CCO\_DDR}$/2) + 0.470 | 8.00 | –8.00 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage (Q–$\overline{Q}$).
3. $V_{OL}$ is the single-ended low-output voltage.
4. $V_{OH}$ is the single-ended high-output voltage.

*Table 26:* **DDR3L Interface Switching Characteristics (800 Mb/s)(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{DQVALID}$ | Input data valid window | 500 | – | ps |
| $T_{DQDS}$(2) | Output DQ to DQS skew | 321 | – | ps |
| $T_{DQDH}$(3) | Output DQS to DQ skew | 380 | – | ps |
| $T_{DQSS}$ | Output clock to DQS skew | –0.12 | 0.04 | $T_{CK}$ |
| $T_{CACK}$(4) | Command/address output setup time with respect to CLK | 636 | – | ps |
| $T_{CKCA}$(5) | Command/address output hold time with respect to CLK | 853 | – | ps |

**Notes:**

1. Recommended $V_{CCO\_DDR}$ = 1.35V ±5%.
2. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}$(AC) or the falling edge of DQ that crosses $V_{IL}$(AC) to $V_{REF}$ of DQS.
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}$(DC) or the falling edge of DQ that crosses $V_{IH}$(DC) to $V_{REF}$ of DQS.
4. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}$(AC) or the falling edge of CMD/ADDR that crosses $V_{IL}$(AC) to $V_{REF}$ of CLK.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}$(DC) or the falling edge of CMD/ADDR that crosses $V_{IH}$(DC) to $V_{REF}$ of CLK.

*Table 27:* **LPDDR2 Interface Switching Characteristics (800 Mb/s)(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{DQVALID}$ | Input data valid window | 500 | – | ps |
| $T_{DQDS}$(2) | Output DQ to DQS skew | 111 | – | ps |
| $T_{DQDH}$(3) | Output DQS to DQ skew | 318 | – | ps |
| $T_{DQSS}$ | Output clock to DQS skew | 0.91 | 1.10 | $T_{CK}$ |
| $T_{CACK}$(4) | Command/address output setup time with respect to CLK | 132 | – | ps |
| $T_{CKCA}$(5) | Command/address output hold time with respect to CLK | 363 | – | ps |

**Notes:**

1. Recommended $V_{CCO\_DDR}$ = 1.2V ±5%.
2. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}$(AC) or the falling edge of DQ that crosses $V_{IL}$(AC) to $V_{REF}$ of DQS.
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}$(DC) or the falling edge of DQ that crosses $V_{IH}$(DC) to $V_{REF}$ of DQS.
4. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}$(AC) or the falling edge of CMD/ADDR that crosses $V_{IL}$(AC) to $V_{REF}$ of CLK.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}$(DC) or the falling edge of CMD/ADDR that crosses $V_{IH}$(DC) to $V_{REF}$ of CLK.

## Static Memory Controller

*Table 31:* **SMC Interface Delay Characteristics(1)(2)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{NANDDOUT}$ | NAND_IO output delay from last register to pad | 4.12 | 6.45 | ns |
| $T_{NANDALE}$ | NAND_ALE output delay from last register to pad | 5.08 | 6.33 | ns |
| $T_{NANDCLE}$ | NAND_CLE output delay from last register to pad | 4.87 | 6.40 | ns |
| $T_{NANDWE}$ | NAND_WE_B output delay from last register to pad | 4.69 | 5.89 | ns |
| $T_{NANDRE}$ | NAND_RE_B output delay from last register to pad | 5.12 | 6.44 | ns |
| $T_{NANDCE}$ | NAND_CE_B output delay from last register to pad | 4.68 | 5.89 | ns |
| $T_{NANDDIN}$ | NAND_IO setup time and input delay from pad to first register | 1.48 | 3.09 | ns |
| $T_{NANDBUSY}$ | NAND_BUSY setup time and input delay from pad to first register | 2.48 | 3.33 | ns |
| $T_{SRAMA}$ | SRAM_A output delay from last register to pad | 3.94 | 5.73 | ns |
| $T_{SRAMDOUT}$ | SRAM_DQ output delay from last register to pad | 4.66 | 6.45 | ns |
| $T_{SRAMCE}$ | SRAM_CE output delay from last register to pad | 4.57 | 5.95 | ns |
| $T_{SRAMOE}$ | SRAM_OE_B output delay from last register to pad | 4.79 | 6.13 | ns |
| $T_{SRAMBLS}$ | SRAM_BLS_B output delay from last register to pad | 5.25 | 6.74 | ns |
| $T_{SRAMWE}$ | SRAM_WE_B output delay from last register to pad | 5.12 | 6.48 | ns |
| $T_{SRAMDIN}$ | SRAM_DQ setup time and input delay from pad to first register | 1.93 | 3.05 | ns |
| $T_{SRAMWAIT}$ | SRAM_WAIT setup time and input delay from pad to first register | 2.26 | 3.15 | ns |

**Notes:**

1. All parameters do not include the package flight time and register controlled delays.
2. Refer to the ARM® PrimeCell® Static Memory Controller (PL350 series) Technical Reference Manual for more SMC timing details.

## Quad-SPI Interfaces

*Table 32:* **Quad-SPI Interface Switching Characteristics**[1][2]

| Symbol | Description | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| **Feedback Clock Enabled** | | | | | |
| $T_{DCQSPICLK1}$ | Quad-SPI clock duty cycle | 44 | – | 56 | % |
| $T_{QSPICKO1}$ | Data and slave select output delay | –0.10 | – | 3.40 | ns |
| $T_{QSPIDCK1}$ | Input data setup time | 2.00 | – | – | ns |
| $T_{QSPICKD1}$ | Input data hold time | 1.30 | – | – | ns |
| $T_{QSPISSCLK1}$ | Slave select asserted to next clock edge | 1 | – | – | $F_{QSPI\_REF\_CLK}$ cycle |
| $T_{QSPICLKSS1}$ | Clock edge to slave select deasserted | 1 | – | – | $F_{QSPI\_REF\_CLK}$ cycle |
| $F_{QSPICLK1}$ | Quad-SPI device clock frequency | – | – | 100[3] | MHz |
| **Feedback Clock Disabled** | | | | | |
| $T_{DCQSPICLK2}$ | Quad-SPI clock duty cycle | 44 | – | 56 | % |
| $T_{QSPICKO2}$ | Data and slave select output delay | –0.10 | – | 3.80 | ns |
| $T_{QSPIDCK2}$ | Input data setup time[4] | $11 - \frac{1}{F_{QSPI\_REF\_CLK}}$ | – | – | ns |
| $T_{QSPICKD2}$ | Input data hold time | $\frac{1}{2 \times F_{QSPICLK2}}$ | – | – | ns |
| $T_{QSPISSCLK2}$ | Slave select asserted to next clock edge | 1 | – | – | $F_{QSPI\_REF\_CLK}$ cycle |
| $T_{QSPICLKSS2}$ | Clock edge to slave select deasserted | 1 | – | – | $F_{QSPI\_REF\_CLK}$ cycle |
| $F_{QSPICLK2}$ | Quad-SPI device clock frequency | – | – | 40 | MHz |
| **Feedback Clock Enabled or Disabled** | | | | | |
| $F_{QSPI\_REF\_CLK}$ | Quad-SPI reference clock frequency | – | – | 200 | MHz |

**Notes:**

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
2. Dual slave select 4-bit stacked I/O configuration is not covered.
3. Requires appropriate component selection/board design.
4. Use 0 ns as the input data setup time when the calculated $T_{QSPIDCK2}$ value is negative.

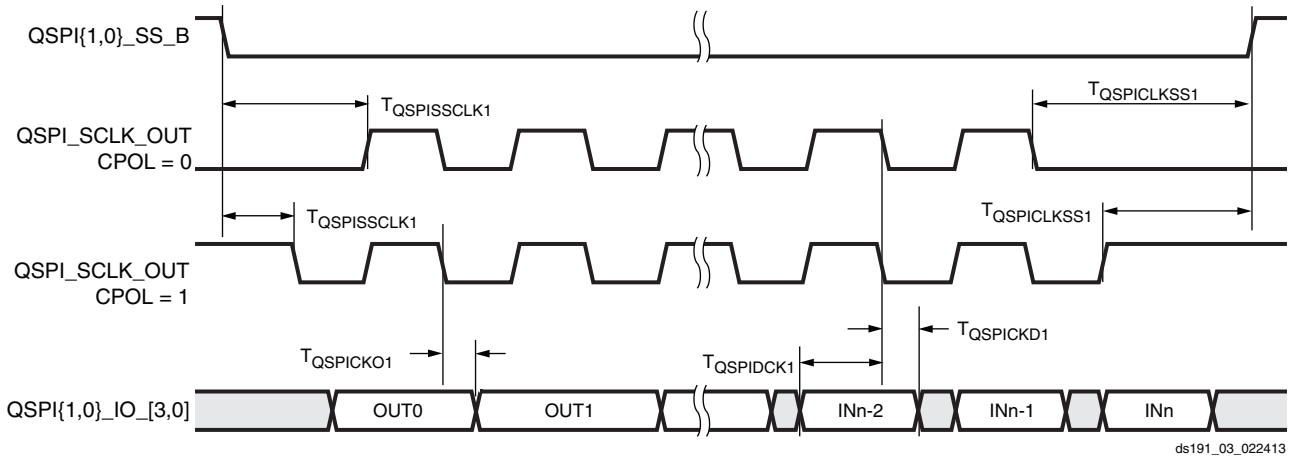


*Figure 3:* **Quad-SPI Interface (Feedback Clock Enabled) Timing Diagram**

## RGMII and MDIO Interfaces

*Table 34:* **RGMII and MDIO Interface Switching Characteristics(1)(2)(3)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_{DCGETXCLK}$ | Transmit clock duty cycle | 45 | – | 55 | % |
| $T_{GEMTXCKO}$ | RGMII_TX_D[3:0], RGMII_TX_CTL output clock to out time | –0.50 | – | 0.50 | ns |
| $T_{GEMRXDCK}$ | RGMII_RX_D[3:0], RGMII_RX_CTL input setup time | 0.80 | – | – | ns |
| $T_{GEMRXCKD}$ | RGMII_RX_D[3:0], RGMII_RX_CTL input hold time | 0.80 | – | – | ns |
| $T_{MDIOCLK}$ | MDC output clock period | 400 | – | – | ns |
| $T_{MDIOCKH}$ | MDC clock High time | 160 | – | – | ns |
| $T_{MDIOCKL}$ | MDC clock Low time | 160 | – | – | ns |
| $T_{MDIODCK}$ | MDIO input data setup time | 80 | – | – | ns |
| $T_{MDIOCKD}$ | MDIO input data hold time | 0 | – | – | ns |
| $T_{MDIOCKO}$ | MDIO data output delay | –20 | – | 170 | ns |
| $F_{GETXCLK}$ | RGMII_TX_CLK transmit clock frequency | – | 125 | – | MHz |
| $F_{GERXCLK}$ | RGMII_RX_CLK receive clock frequency | – | 125 | – | MHz |
| $F_{ENET\_REF\_CLK}$ | Ethernet reference clock frequency | – | 125 | – | MHz |

**Notes:**

1. Test conditions: LVCMOS25, fast slew rate, 8 mA drive strength, 15 pF loads. Values in this table are specified during 1000 Mb/s operation.
2. LVCMOS25 slow slew rate and LVCMOS33 are not supported.
3. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

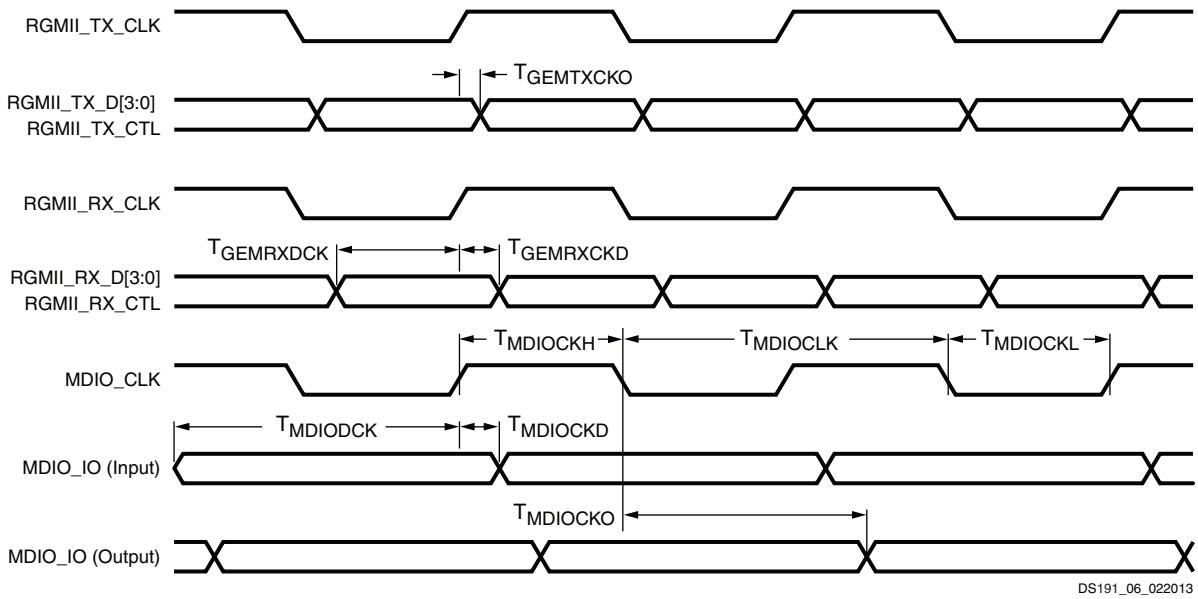


*Figure 6:* **RGMII Interface Timing Diagram**

## SPI Interfaces

*Table 39:* **SPI Master Mode Interface Switching Characteristics(1)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_{DCMSPICLK}$ | SPI master mode clock duty cycle | – | 50 | – | % |
| $T_{MSPIDCK}$ | Input setup time for SPI{0,1}_MISO | 2.00 | – | – | ns |
| $T_{MSPICKD}$ | Input hold time for SPI{0,1}_MISO | 8.20 | – | – | ns |
| $T_{MSPICKO}$ | Output delay for SPI{0,1}_MOSI and SPI{0,1}_SS | –3.10 | – | 3.90 | ns |
| $T_{MSPISSCLK}$ | Slave select asserted to first active clock edge | 1 | – | – | $F_{SPI\_REF\_CLK}$ cycles |
| $T_{MSPICLKSS}$ | Last active clock edge to slave select deasserted | 0.5 | – | – | $F_{SPI\_REF\_CLK}$ cycles |
| $F_{MSPICLK}$ | SPI master mode device clock frequency | – | – | 50.00 | MHz |
| $F_{SPI\_REF\_CLK}$ | SPI reference clock frequency | – | – | 200.00 | MHz |

**Notes:**

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

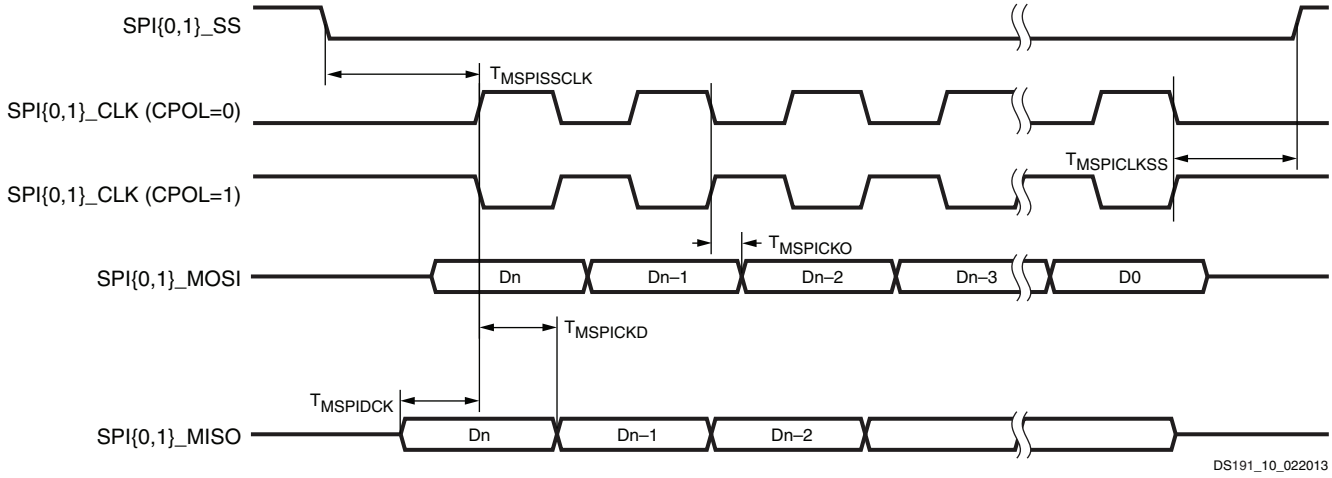


*Figure 11:* **SPI Master (CPHA = 0) Interface Timing Diagram**

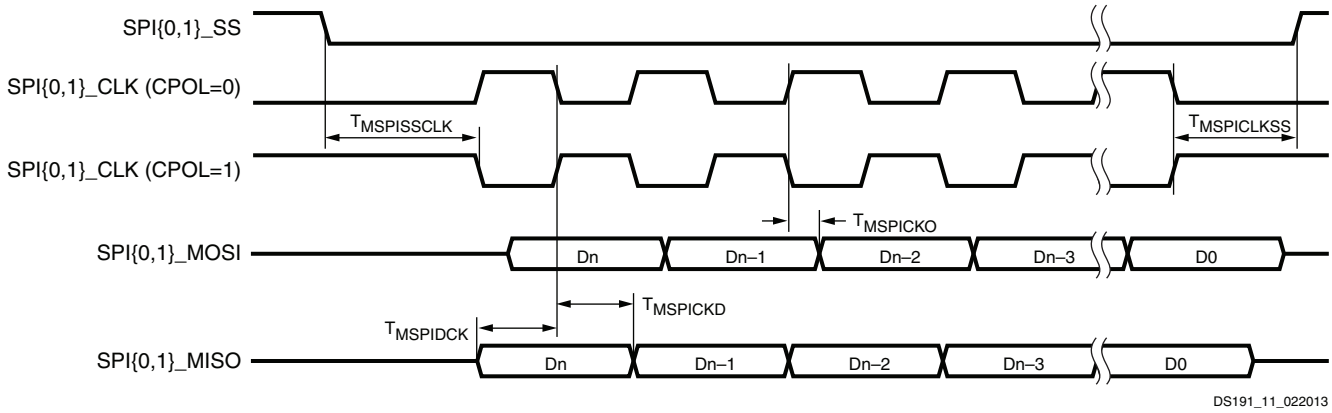


*Figure 12:* **SPI Master (CPHA = 1) Interface Timing Diagram**

*Table 50:* **Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator (FFG Packages)(1)(2)**

| Memory Standard | I/O Bank Type | $V_{CCAUX\_IO}$ | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | |
| **4:1 Memory Controllers** | | | | | | |
| DDR3 | HP | 2.0V | 1866 | 1866 | 1600 | Mb/s |
| | HP | 1.8V | 1600 | 1333 | 1066 | Mb/s |
| | HR | N/A | 1066 | 1066 | 800 | Mb/s |
| DDR3L | HP | 2.0V | 1600 | 1600 | 1333 | Mb/s |
| | HP | 1.8V | 1333 | 1066 | 800 | Mb/s |
| | HR | N/A | 800 | 800 | 667 | Mb/s |
| DDR2 | HP | 2.0V | 800 | 800 | 800 | Mb/s |
| | HP | 1.8V | 800 | 800 | 800 | Mb/s |
| | HR | N/A | 800 | 800 | 800 | Mb/s |
| RLDRAM III | HP | 2.0V | 800 | 667 | 667 | MHz |
| | HP | 1.8V | 550 | 500 | 450 | MHz |
| | HR | N/A | N/A | | | |
| **2:1 Memory Controllers** | | | | | | |
| DDR3 | HP | 2.0V | 1066 | 1066 | 800 | Mb/s |
| | HP | 1.8V | 1066 | 1066 | 800 | Mb/s |
| | HR | N/A | 1066 | 1066 | 800 | Mb/s |
| DDR3L | HP | 2.0V | 1066 | 1066 | 800 | Mb/s |
| | HP | 1.8V | 1066 | 1066 | 800 | Mb/s |
| | HR | N/A | 800 | 800 | 667 | Mb/s |
| DDR2 | HP | 2.0V | 800 | 800 | 800 | Mb/s |
| | HP | 1.8V | | | | |
| | HR | N/A | | | | |
| QDR II+(3) | HP | 2.0V | 550 | 500 | 450 | MHz |
| | HP | 1.8V | | | | |
| | HR | N/A | 500 | 450 | 400 | MHz |
| RLDRAM II | HP | 2.0V | 533 | 500 | 450 | MHz |
| | HP | 1.8V | | | | |
| | HR | N/A | | | | |
| LPDDR2 | HP | 2.0V | 667 | 667 | 667 | Mb/s |
| | HP | 1.8V | 667 | 667 | 667 | Mb/s |
| | HR | N/A | 667 | 667 | 667 | Mb/s |

**Notes:**

1. $V_{REF}$ tracking is required. For more information, see UG586, *7 Series FPGAs Memory Interface Solutions User Guide*.
2. When using the internal $V_{REF}$, the maximum data rate is 800 Mb/s (400 MHz).
3. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

# PL Switching Characteristics

## IOB Pad Input/Output/3-State

Table 52 (3.3V high-range IOB (HR)) and Table 53 (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{IOPI}$ is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{IOOP}$ is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{IOTP}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than $T_{IOTP}$ when the DCITERMDISABLE pin is used. In HR I/O banks, the IN_TERM termination turn-on time is always faster than $T_{IOTP}$ when the INTERMDISABLE pin is used.

*Table 52:* **3.3V IOB High Range (HR) Switching Characteristics**

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -3 | -2 | -1 | -3 | -2 | -1 | -3 | -2 | -1 | |
| LVTTL_S4 | 1.31 | 1.42 | 1.64 | 3.77 | 3.90 | 4.00 | 4.53 | 4.76 | 4.99 | ns |
| LVTTL_S8 | 1.31 | 1.42 | 1.64 | 3.50 | 3.64 | 3.73 | 4.26 | 4.50 | 4.72 | ns |
| LVTTL_S12 | 1.31 | 1.42 | 1.64 | 3.49 | 3.62 | 3.72 | 4.25 | 4.48 | 4.71 | ns |
| LVTTL_S16 | 1.31 | 1.42 | 1.64 | 3.03 | 3.17 | 3.26 | 3.79 | 4.03 | 4.25 | ns |
| LVTTL_S24 | 1.31 | 1.42 | 1.64 | 3.25 | 3.39 | 3.48 | 4.01 | 4.25 | 4.47 | ns |
| LVTTL_F4 | 1.31 | 1.42 | 1.64 | 3.22 | 3.36 | 3.45 | 3.98 | 4.22 | 4.44 | ns |
| LVTTL_F8 | 1.31 | 1.42 | 1.64 | 2.71 | 2.84 | 2.93 | 3.47 | 3.70 | 3.92 | ns |
| LVTTL_F12 | 1.31 | 1.42 | 1.64 | 2.69 | 2.82 | 2.92 | 3.45 | 3.68 | 3.91 | ns |
| LVTTL_F16 | 1.31 | 1.42 | 1.64 | 2.57 | 2.85 | 3.15 | 3.33 | 3.71 | 4.14 | ns |
| LVTTL_F24 | 1.31 | 1.42 | 1.64 | 2.41 | 2.64 | 2.89 | 3.17 | 3.50 | 3.88 | ns |
| LVDS_25(1) | 0.64 | 0.68 | 0.80 | 1.36 | 1.47 | 1.55 | 2.12 | 2.33 | 2.54 | ns |
| MINI_LVDS_25 | 0.68 | 0.70 | 0.79 | 1.36 | 1.47 | 1.55 | 2.12 | 2.33 | 2.54 | ns |
| BLVDS_25(1) | 0.65 | 0.69 | 0.80 | 1.83 | 2.02 | 2.20 | 2.59 | 2.88 | 3.19 | ns |
| RSDS_25(1) | 0.63 | 0.68 | 0.79 | 1.36 | 1.48 | 1.55 | 2.12 | 2.34 | 2.54 | ns |
| PPDS_25(1) | 0.65 | 0.69 | 0.80 | 1.36 | 1.49 | 1.58 | 2.12 | 2.35 | 2.57 | ns |
| TMDS_33(1) | 0.72 | 0.76 | 0.86 | 1.43 | 1.54 | 1.60 | 2.19 | 2.40 | 2.59 | ns |
| PCI33_3(1) | 1.28 | 1.41 | 1.65 | 2.71 | 3.08 | 3.52 | 3.47 | 3.94 | 4.51 | ns |
| HSUL_12 | 0.63 | 0.64 | 0.71 | 1.77 | 1.90 | 2.00 | 2.53 | 2.76 | 2.99 | ns |
| DIFF_HSUL_12 | 0.58 | 0.61 | 0.70 | 1.55 | 1.68 | 1.78 | 2.31 | 2.54 | 2.77 | ns |
| HSTL_I_S | 0.61 | 0.64 | 0.73 | 1.55 | 1.69 | 1.80 | 2.31 | 2.55 | 2.79 | ns |
| HSTL_II_S | 0.61 | 0.64 | 0.73 | 1.21 | 1.34 | 1.43 | 1.97 | 2.20 | 2.42 | ns |
| HSTL_I_18_S | 0.64 | 0.67 | 0.76 | 1.28 | 1.39 | 1.45 | 2.04 | 2.25 | 2.44 | ns |
| HSTL_II_18_S | 0.64 | 0.67 | 0.76 | 1.18 | 1.31 | 1.40 | 1.94 | 2.17 | 2.39 | ns |
| DIFF_HSTL_I_S | 0.63 | 0.67 | 0.77 | 1.42 | 1.54 | 1.61 | 2.18 | 2.40 | 2.60 | ns |
| DIFF_HSTL_II_S | 0.63 | 0.67 | 0.77 | 1.15 | 1.24 | 1.27 | 1.91 | 2.10 | 2.26 | ns |
| DIFF_HSTL_I_18_S | 0.65 | 0.69 | 0.78 | 1.27 | 1.38 | 1.43 | 2.03 | 2.24 | 2.42 | ns |

*Table 52:* **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -3 | -2 | -1 | -3 | -2 | -1 | -3 | -2 | -1 | |
| LVCMOS15_S16 | 0.66 | 0.69 | 0.81 | 1.76 | 1.95 | 2.13 | 2.52 | 2.81 | 3.12 | ns |
| LVCMOS15_F4 | 0.66 | 0.69 | 0.81 | 1.63 | 1.76 | 1.86 | 2.39 | 2.62 | 2.85 | ns |
| LVCMOS15_F8 | 0.66 | 0.69 | 0.81 | 1.79 | 1.99 | 2.18 | 2.55 | 2.85 | 3.17 | ns |
| LVCMOS15_F12 | 0.66 | 0.69 | 0.81 | 1.40 | 1.54 | 1.65 | 2.16 | 2.40 | 2.64 | ns |
| LVCMOS15_F16 | 0.66 | 0.69 | 0.81 | 1.37 | 1.51 | 1.61 | 2.13 | 2.37 | 2.60 | ns |
| LVCMOS12_S4 | 0.88 | 0.91 | 1.00 | 2.53 | 2.67 | 2.76 | 3.29 | 3.53 | 3.75 | ns |
| LVCMOS12_S8 | 0.88 | 0.91 | 1.00 | 2.05 | 2.18 | 2.28 | 2.81 | 3.04 | 3.27 | ns |
| LVCMOS12_S12(1) | 0.88 | 0.91 | 1.00 | 1.75 | 1.89 | 1.98 | 2.51 | 2.75 | 2.97 | ns |
| LVCMOS12_F4 | 0.88 | 0.91 | 1.00 | 1.94 | 2.07 | 2.17 | 2.70 | 2.93 | 3.16 | ns |
| LVCMOS12_F8 | 0.88 | 0.91 | 1.00 | 1.50 | 1.64 | 1.73 | 2.26 | 2.50 | 2.72 | ns |
| LVCMOS12_F12(1) | 0.88 | 0.91 | 1.00 | 1.54 | 1.71 | 1.87 | 2.30 | 2.57 | 2.86 | ns |
| SSTL135_S | 0.61 | 0.64 | 0.73 | 1.27 | 1.40 | 1.50 | 2.03 | 2.26 | 2.49 | ns |
| SSTL15_S | 0.61 | 0.64 | 0.73 | 1.24 | 1.37 | 1.47 | 2.00 | 2.23 | 2.46 | ns |
| SSTL18_I_S | 0.64 | 0.67 | 0.76 | 1.59 | 1.74 | 1.85 | 2.35 | 2.60 | 2.84 | ns |
| SSTL18_II_S | 0.64 | 0.67 | 0.76 | 1.27 | 1.40 | 1.50 | 2.03 | 2.26 | 2.49 | ns |
| DIFF_SSTL135_S | 0.59 | 0.61 | 0.73 | 1.27 | 1.40 | 1.50 | 2.03 | 2.26 | 2.49 | ns |
| DIFF_SSTL15_S | 0.63 | 0.67 | 0.77 | 1.24 | 1.37 | 1.47 | 2.00 | 2.23 | 2.46 | ns |
| DIFF_SSTL18_I_S | 0.65 | 0.69 | 0.78 | 1.50 | 1.63 | 1.72 | 2.26 | 2.49 | 2.71 | ns |
| DIFF_SSTL18_II_S | 0.65 | 0.69 | 0.78 | 1.13 | 1.22 | 1.25 | 1.89 | 2.08 | 2.24 | ns |
| SSTL135_F | 0.61 | 0.64 | 0.73 | 1.04 | 1.17 | 1.26 | 1.80 | 2.03 | 2.25 | ns |
| SSTL15_F | 0.61 | 0.64 | 0.73 | 1.04 | 1.17 | 1.26 | 1.80 | 2.03 | 2.25 | ns |
| SSTL18_I_F | 0.64 | 0.67 | 0.76 | 1.12 | 1.22 | 1.26 | 1.88 | 2.08 | 2.25 | ns |
| SSTL18_II_F | 0.64 | 0.67 | 0.76 | 1.05 | 1.18 | 1.28 | 1.81 | 2.04 | 2.27 | ns |
| DIFF_SSTL135_F | 0.59 | 0.61 | 0.73 | 1.04 | 1.17 | 1.26 | 1.80 | 2.03 | 2.25 | ns |
| DIFF_SSTL15_F | 0.63 | 0.67 | 0.77 | 1.04 | 1.17 | 1.26 | 1.80 | 2.03 | 2.25 | ns |
| DIFF_SSTL18_I_F | 0.65 | 0.69 | 0.78 | 1.10 | 1.19 | 1.23 | 1.86 | 2.05 | 2.22 | ns |
| DIFF_SSTL18_II_F | 0.65 | 0.69 | 0.78 | 1.02 | 1.10 | 1.14 | 1.78 | 1.96 | 2.13 | ns |

**Notes:**

1. This I/O standard is only available in the 3.3V high-range (HR) banks.

*Table 56:* **OLOGIC Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1 | |
| **Setup/Hold** | | | | | |
| $T_{ODCK}/T_{OCKD}$ | D1/D2 pins setup/hold with respect to CLK | 0.45/–0.13 | 0.50/–0.13 | 0.58/–0.13 | ns |
| $T_{OOCECK}/T_{OCKOCE}$ | OCE pin setup/hold with respect to CLK | 0.28/0.03 | 0.29/0.03 | 0.45/0.03 | ns |
| $T_{OSRCK}/T_{OCKSR}$ | SR pin setup/hold with respect to CLK | 0.32/0.18 | 0.38/0.18 | 0.70/0.18 | ns |
| $T_{OTCK}/T_{OCKT}$ | T1/T2 pins setup/hold with respect to CLK | 0.49/–0.16 | 0.56/–0.16 | 0.68/–0.16 | ns |
| $T_{OTCECK}/T_{OCKTCE}$ | TCE pin setup/hold with respect to CLK | 0.28/0.01 | 0.30/0.01 | 0.45/0.01 | ns |
| **Combinatorial** | | | | | |
| $T_{ODQ}$ | D1 to OQ out or T1 to TQ out | 0.73 | 0.81 | 0.97 | ns |
| **Sequential Delays** | | | | | |
| $T_{OCKQ}$ | CLK to OQ/TQ out | 0.41 | 0.43 | 0.49 | ns |
| $T_{RQ\_OLOGICE2}$ | SR pin to OQ/TQ out (HP I/O banks only) | 0.63 | 0.70 | 0.83 | ns |
| $T_{GSRQ\_OLOGICE2}$ | Global set/reset to Q outputs (HP I/O banks only) | 7.60 | 7.60 | 10.51 | ns |
| $T_{RQ\_OLOGICE3}$ | SR pin to OQ/TQ out (HR I/O banks only) | 0.63 | 0.70 | 0.83 | ns |
| $T_{GSRQ\_OLOGICE3}$ | Global set/reset to Q outputs (HR I/O banks only) | 7.60 | 7.60 | 10.51 | ns |
| **Set/Reset** | | | | | |
| $T_{RPW\_OLOGICE2}$ | Minimum pulse width, SR inputs (HP I/O banks only) | 0.54 | 0.54 | 0.63 | ns, Min |
| $T_{RPW\_OLOGICE3}$ | Minimum pulse width, SR inputs (HR I/O banks only) | 0.54 | 0.54 | 0.63 | ns, Min |

## Input Serializer/Deserializer Switching Characteristics

*Table 57:* **ISERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1 | |
| **Setup/Hold for Control Lines** | | | | | |
| $T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$ | BITSLIP pin setup/hold with respect to CLKDIV | 0.01/0.12 | 0.02/0.13 | 0.02/0.15 | ns |
| $T_{ISCCK\_CE}$ / $T_{ISCKC\_CE}$(2) | CE pin setup/hold with respect to CLK (for CE1) | 0.39/–0.02 | 0.44/–0.02 | 0.63/–0.02 | ns |
| $T_{ISCCK\_CE2}$ / $T_{ISCKC\_CE2}$(2) | CE pin setup/hold with respect to CLKDIV (for CE2) | –0.12/0.29 | –0.12/0.31 | –0.12/0.35 | ns |
| **Setup/Hold for Data Lines** | | | | | |
| $T_{ISDCK\_D}$ /$T_{ISCKD\_D}$ | D pin setup/hold with respect to CLK | –0.02/0.11 | –0.02/0.12 | –0.02/0.15 | ns |
| $T_{ISDCK\_DDLY}$ /$T_{ISCKD\_DDLY}$ | DDLY pin setup/hold with respect to CLK (using IDELAY)(1) | –0.02/0.11 | –0.02/0.12 | –0.02/0.15 | ns |
| $T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$ | D pin setup/hold with respect to CLK at DDR mode | –0.02/0.11 | –0.02/0.12 | –0.02/0.15 | ns |
| $T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$ | D pin setup/hold with respect to CLK at DDR mode (using IDELAY)(1) | 0.11/0.11 | 0.12/0.12 | 0.15/0.15 | ns |
| **Sequential Delays** | | | | | |
| $T_{ISCKO\_Q}$ | CLKDIV to out at Q pin | 0.46 | 0.47 | 0.58 | ns |
| **Propagation Delays** | | | | | |
| $T_{ISDO\_DO}$ | D input to DO output pin | 0.09 | 0.10 | 0.12 | ns |

**Notes:**

1. Recorded at 0 tap value.
2. $T_{ISCCK\_CE2}$ and $T_{ISCKC\_CE2}$ are reported as $T_{ISCCK\_CE}$/$T_{ISCKC\_CE}$ in TRACE report.

## Output Serializer/Deserializer Switching Characteristics

*Table 58:* **OSERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1 | |
| **Setup/Hold** | | | | | |
| $T_{OSDCK\_D}$/$T_{OSCKD\_D}$ | D input setup/hold with respect to CLKDIV | 0.37/0.02 | 0.40/0.02 | 0.55/0.02 | ns |
| $T_{OSDCK\_T}$/$T_{OSCKD\_T}$(1) | T input setup/hold with respect to CLK | 0.49/–0.15 | 0.56/–0.15 | 0.68/–0.15 | ns |
| $T_{OSDCK\_T2}$/$T_{OSCKD\_T2}$(1) | T input setup/hold with respect to CLKDIV | 0.27/–0.15 | 0.30/–0.15 | 0.34/–0.15 | ns |
| $T_{OSCCK\_OCE}$/$T_{OSCKC\_OCE}$ | OCE input setup/hold with respect to CLK | 0.28/0.03 | 0.29/0.03 | 0.45/0.03 | ns |
| $T_{OSCCK\_S}$ | SR (reset) input setup with respect to CLKDIV | 0.41 | 0.46 | 0.75 | ns |
| $T_{OSCCK\_TCE}$/$T_{OSCKC\_TCE}$ | TCE input setup/hold with respect to CLK | 0.28/0.01 | 0.30/0.01 | 0.45/0.01 | ns |
| **Sequential Delays** | | | | | |
| $T_{OSCKO\_OQ}$ | Clock to out from CLK to OQ | 0.35 | 0.37 | 0.42 | ns |
| $T_{OSCKO\_TQ}$ | Clock to out from CLK to TQ | 0.41 | 0.43 | 0.49 | ns |
| **Combinatorial** | | | | | |
| $T_{OSDO\_TTQ}$ | T input to TQ out | 0.73 | 0.81 | 0.97 | ns |

**Notes:**

1. $T_{OSDCK\_T2}$ and $T_{OSCKD\_T2}$ are reported as $T_{OSDCK\_T}$/$T_{OSCKD\_T}$ in TRACE report.

*Table 60:* **IO_FIFO Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1 | |
| **IO_FIFO Clock to Out Delays** | | | | | |
| $T_{OFFCKO\_DO}$ | RDCLK to Q outputs | 0.51 | 0.56 | 0.63 | ns |
| $T_{CKO\_FLAGS}$ | Clock to IO_FIFO flags | 0.59 | 0.62 | 0.81 | ns |
| **Setup/Hold** | | | | | |
| $T_{CCK\_D}/T_{CKC\_D}$ | D inputs to WRCLK | 0.43/–0.01 | 0.47/–0.01 | 0.53/–0.01 | ns |
| $T_{IFFCCK\_WREN}/T_{IFFCKC\_WREN}$ | WREN to WRCLK | 0.39/–0.01 | 0.43/–0.01 | 0.50/–0.01 | ns |
| $T_{OFFCCK\_RDEN}/T_{OFFCKC\_RDEN}$ | RDEN to RDCLK | 0.49/0.01 | 0.53/0.02 | 0.61/0.02 | ns |
| **Minimum Pulse Width** | | | | | |
| $T_{PWH\_IO\_FIFO}$ | RESET, RDCLK, WRCLK | 0.81 | 0.92 | 1.08 | ns |
| $T_{PWL\_IO\_FIFO}$ | RESET, RDCLK, WRCLK | 0.81 | 0.92 | 1.08 | ns |
| **Maximum Frequency** | | | | | |
| $F_{MAX}$ | RDCLK and WRCLK | 533.05 | 470.37 | 400.00 | MHz |

## Block RAM and FIFO Switching Characteristics

*Table 64:* **Block RAM and FIFO Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1 | |
| **Block RAM and FIFO Clock-to-Out Delays** | | | | | |
| $T_{RCKO\_DO}$ and $T_{RCKO\_DO\_REG}$[1] | Clock CLK to DOUT output (without output register)[2][3] | 1.57 | 1.80 | 2.08 | ns, Max |
| | Clock CLK to DOUT output (with output register)[4][5] | 0.54 | 0.63 | 0.75 | ns, Max |
| $T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$ | Clock CLK to DOUT output with ECC (without output register)[2][3] | 2.35 | 2.58 | 3.26 | ns, Max |
| | Clock CLK to DOUT output with ECC (with output register)[4][5] | 0.62 | 0.69 | 0.80 | ns, Max |
| $T_{RCKO\_DO\_CASCOUT}$ and $T_{RCKO\_DO\_CASCOUT\_REG}$ | Clock CLK to DOUT output with Cascade (without output register)[2] | 2.21 | 2.45 | 2.80 | ns, Max |
| | Clock CLK to DOUT output with Cascade (with output register)[4] | 0.98 | 1.08 | 1.24 | ns, Max |
| $T_{RCKO\_FLAGS}$ | Clock CLK to FIFO flags outputs[6] | 0.65 | 0.74 | 0.89 | ns, Max |
| $T_{RCKO\_POINTERS}$ | Clock CLK to FIFO pointers outputs[7] | 0.79 | 0.87 | 0.98 | ns, Max |
| $T_{RCKO\_PARITY\_ECC}$ | Clock CLK to ECCPARITY in ECC encode only mode | 0.66 | 0.72 | 0.80 | ns, Max |
| $T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$ | Clock CLK to BITERR (without output register) | 2.17 | 2.38 | 3.01 | ns, Max |
| | Clock CLK to BITERR (with output register) | 0.57 | 0.65 | 0.76 | ns, Max |
| $T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$ | Clock CLK to RDADDR output with ECC (without output register) | 0.64 | 0.74 | 0.90 | ns, Max |
| | Clock CLK to RDADDR output with ECC (with output register) | 0.71 | 0.79 | 0.92 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | |
| $T_{RCCK\_ADDRA}/T_{RCKC\_ADDRA}$ | ADDR inputs[8] | 0.38/0.27 | 0.42/0.28 | 0.48/0.31 | ns, Min |
| $T_{RDCK\_DI\_WF\_NC}$/ $T_{RCKD\_DI\_WF\_NC}$ | Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode[9] | 0.49/0.51 | 0.55/0.53 | 0.63/0.57 | ns, Min |
| $T_{RDCK\_DI\_RF}/T_{RCKD\_DI\_RF}$ | Data input setup/hold time when block RAM is configured in READ_FIRST mode[9] | 0.17/0.25 | 0.19/0.29 | 0.21/0.35 | ns, Min |
| $T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$ | DIN inputs with block RAM ECC in standard mode[9] | 0.42/0.37 | 0.47/0.39 | 0.53/0.43 | ns, Min |
| $T_{RDCK\_DI\_ECCW}/T_{RCKD\_DI\_ECCW}$ | DIN inputs with block RAM ECC encode only[9] | 0.79/0.37 | 0.87/0.39 | 0.99/0.43 | ns, Min |
| $T_{RDCK\_DI\_ECC\_FIFO}$/ $T_{RCKD\_DI\_ECC\_FIFO}$ | DIN inputs with FIFO ECC in standard mode[9] | 0.89/0.47 | 0.98/0.50 | 1.12/0.54 | ns, Min |
| $T_{RCCK\_INJECTBITERR}$/ $T_{RCKC\_INJECTBITERR}$ | Inject single/double bit error in ECC mode | 0.49/0.30 | 0.55/0.31 | 0.63/0.34 | ns, Min |
| $T_{RCCK\_EN}/T_{RCKC\_EN}$ | Block RAM Enable (EN) input | 0.30/0.17 | 0.33/0.18 | 0.38/0.20 | ns, Min |
| $T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$ | CE input of output register | 0.21/0.13 | 0.25/0.13 | 0.31/0.14 | ns, Min |
| $T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$ | Synchronous RSTREG input | 0.25/0.06 | 0.27/0.06 | 0.29/0.06 | ns, Min |
| $T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$ | Synchronous RSTRAM input | 0.27/0.35 | 0.29/0.37 | 0.31/0.39 | ns, Min |
| $T_{RCCK\_WEA}/T_{RCKC\_WEA}$ | Write Enable (WE) input (Block RAM only) | 0.38/0.15 | 0.41/0.16 | 0.46/0.17 | ns, Min |
| $T_{RCCK\_WREN}/T_{RCKC\_WREN}$ | WREN FIFO inputs | 0.39/0.25 | 0.39/0.30 | 0.40/0.37 | ns, Min |
| $T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$ | RDEN FIFO inputs | 0.36/0.26 | 0.36/0.30 | 0.37/0.37 | ns, Min |

*Table 64:* **Block RAM and FIFO Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1 | |
| **Reset Delays** | | | | | |
| $T_{RCO\_FLAGS}$ | Reset RST to FIFO flags/pointers(10) | 0.76 | 0.83 | 0.93 | ns, Max |
| $T_{RREC\_RST}/T_{RREM\_RST}$ | FIFO reset recovery and removal timing(11) | 1.59/–0.68 | 1.76/–0.68 | 2.01/–0.68 | ns, Max |
| **Maximum Frequency** | | | | | |
| $F_{MAX\_BRAM\_WF\_NC}$ | Block RAM (Write first and No change modes)<br>When not in SDP RF mode | 601.32 | 543.77 | 458.09 | MHz |
| $F_{MAX\_BRAM\_RF\_PERFORMANCE}$ | Block RAM (Read first, Performance mode)<br>When in SDP RF mode but no address overlap between port A and port B | 601.32 | 543.77 | 458.09 | MHz |
| $F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$ | Block RAM (Read first, Delayed_write mode)<br>When in SDP RF mode and there is possibility of overlap between port A and port B addresses | 528.26 | 477.33 | 400.80 | MHz |
| $F_{MAX\_CAS\_WF\_NC}$ | Block RAM Cascade (Write first, No change mode)<br>When cascade but not in RF mode | 551.27 | 493.93 | 408.00 | MHz |
| $F_{MAX\_CAS\_RF\_PERFORMANCE}$ | Block RAM Cascade (Read first, Performance mode)<br>When in cascade with RF mode and no possibility of address overlap/one port is disabled | 551.27 | 493.93 | 408.00 | MHz |
| $F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$ | When in cascade RF mode and there is a possibility of address overlap between port A and port B | 478.24 | 427.35 | 350.88 | MHz |
| $F_{MAX\_FIFO}$ | FIFO in all modes without ECC | 601.32 | 543.77 | 458.09 | MHz |
| $F_{MAX\_ECC}$ | Block RAM and FIFO in ECC configuration | 484.26 | 430.85 | 351.12 | MHz |

**Notes:**

1. TRACE will report all of these parameters as $T_{RCKO\_DO}$.
2. $T_{RCKO\_DOR}$ includes $T_{RCKO\_DOW}$, $T_{RCKO\_DOPR}$, and $T_{RCKO\_DOPW}$ as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. $T_{RCKO\_DO}$ includes $T_{RCKO\_DOP}$ as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. $T_{RCKO\_FLAGS}$ includes the following parameters: $T_{RCKO\_AEMPTY}$, $T_{RCKO\_AFULL}$, $T_{RCKO\_EMPTY}$, $T_{RCKO\_FULL}$, $T_{RCKO\_RDERR}$, $T_{RCKO\_WRERR}$.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. $T_{RCO\_FLAGS}$ includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

## DSP48E1 Switching Characteristics

*Table 65:* **DSP48E1 Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1 | |
| **Setup and Hold Times of Data/Control Pins to the Input Register Clock** | | | | | |
| $T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$ | A input to A register CLK | 0.24/0.12 | 0.27/0.14 | 0.31/0.16 | ns |
| $T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$ | B input to B register CLK | 0.28/0.13 | 0.32/0.14 | 0.39/0.15 | ns |
| $T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$ | C input to C register CLK | 0.15/0.15 | 0.17/0.17 | 0.20/0.20 | ns |
| $T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$ | D input to D register CLK | 0.21/0.19 | 0.27/0.22 | 0.35/0.26 | ns |
| $T_{DSPDCK\_ACIN\_AREG}$/$T_{DSPCKD\_ACIN\_AREG}$ | ACIN input to A register CLK | 0.21/0.12 | 0.24/0.14 | 0.27/0.16 | ns |
| $T_{DSPDCK\_BCIN\_BREG}$/$T_{DSPCKD\_BCIN\_BREG}$ | BCIN input to B register CLK | 0.22/0.13 | 0.25/0.14 | 0.30/0.15 | ns |
| **Setup and Hold Times of Data Pins to the Pipeline Register Clock** | | | | | |
| $T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_B\_MREG\_MULT}$ | {A, B,} input to M register CLK using multiplier | 2.04/–0.01 | 2.34/–0.01 | 2.79/–0.01 | ns |
| $T_{DSPDCK\_\{A, B\}\_ADREG}$/ $T_{DSPCKD\_ D\_ADREG}$ | {A, D} input to AD register CLK | 1.09/–0.02 | 1.25/–0.02 | 1.49/–0.02 | ns |
| **Setup and Hold Times of Data/Control Pins to the Output Register Clock** | | | | | |
| $T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\} \_PREG\_MULT}$ | {A, B,} input to P register CLK using multiplier | 3.41/–0.24 | 3.90/–0.24 | 4.64/–0.24 | ns |
| $T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$ | D input to P register CLK using multiplier | 3.33/–0.62 | 3.81/–0.62 | 4.53/–0.62 | ns |
| $T_{DSPDCK\_\{A, B\} \_PREG}$/ $T_{DSPCKD\_\{A, B\} \_PREG}$ | A or B input to P register CLK not using multiplier | 1.47/–0.24 | 1.68/–0.24 | 2.00/–0.24 | ns |
| $T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$ | C input to P register CLK not using multiplier | 1.30/–0.22 | 1.49/–0.22 | 1.78/–0.22 | ns |
| $T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$ | PCIN input to P register CLK | 1.12/–0.13 | 1.28/–0.13 | 1.52/–0.13 | ns |
| **Setup and Hold Times of the CE Pins** | | | | | |
| $T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$ | {CEA; CEB} input to {A; B} register CLK | 0.30/0.05 | 0.36/0.06 | 0.44/0.09 | ns |
| $T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$ | CEC input to C register CLK | 0.24/0.08 | 0.29/0.09 | 0.36/0.11 | ns |
| $T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$ | CED input to D register CLK | 0.31/–0.02 | 0.36/–0.02 | 0.44/–0.02 | ns |
| $T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$ | CEM input to M register CLK | 0.26/0.15 | 0.29/0.17 | 0.33/0.20 | ns |
| $T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$ | CEP input to P register CLK | 0.31/0.01 | 0.36/0.01 | 0.45/0.01 | ns |
| **Setup and Hold Times of the RST Pins** | | | | | |
| $T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$ | {RSTA, RSTB} input to {A, B} register CLK | 0.34/0.10 | 0.39/0.11 | 0.47/0.13 | ns |
| $T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$ | RSTC input to C register CLK | 0.06/0.22 | 0.07/0.24 | 0.08/0.26 | ns |
| $T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$ | RSTD input to D register CLK | 0.37/0.06 | 0.42/0.06 | 0.50/0.07 | ns |
| $T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$ | RSTM input to M register CLK | 0.18/0.18 | 0.20/0.21 | 0.23/0.24 | ns |
| $T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$ | RSTP input to P register CLK | 0.24/0.01 | 0.26/0.01 | 0.30/0.01 | ns |
| **Combinatorial Delays from Input Pins to Output Pins** | | | | | |
| $T_{DSPDO\_A\_CARRYOUT\_MULT}$ | A input to CARRYOUT output using multiplier | 3.21 | 3.69 | 4.39 | ns |
| $T_{DSPDO\_D\_P\_MULT}$ | D input to P output using multiplier | 3.15 | 3.61 | 4.30 | ns |
| $T_{DSPDO\_A\_P}$ | A input to P output not using multiplier | 1.30 | 1.48 | 1.76 | ns |
| $T_{DSPDO\_C\_P}$ | C input to P output | 1.13 | 1.30 | 1.55 | ns |

*Table 70:* **Duty-Cycle Distortion and Clock-Tree Skew**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | |
| $T_{DCD\_CLK}$ | Global clock tree duty-cycle distortion(1) | All | 0.20 | 0.20 | 0.20 | ns |
| $T_{CKSKEW}$ | Global clock tree skew(2) | XC7Z030 | 0.29 | 0.36 | 0.37 | ns |
| | | XC7Z045 | 0.43 | 0.54 | 0.57 | ns |
| | | XC7Z100 | | | | ns |
| $T_{DCD\_BUFIO}$ | I/O clock tree duty-cycle distortion | All | 0.12 | 0.12 | 0.12 | ns |
| $T_{BUFIOSKEW}$ | I/O clock tree skew across one clock region | All | 0.02 | 0.02 | 0.02 | ns |
| $T_{DCD\_BUFR}$ | Regional clock tree duty-cycle distortion | All | 0.15 | 0.15 | 0.15 | ns |

**Notes:**

1. These parameters represent the worst-case duty-cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty-cycle distortion that might be caused by asymmetrical rise/fall times.
2. The $T_{CKSKEW}$value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate application specific clock skew.

## MMCM Switching Characteristics

*Table 71:* **MMCM Specification**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1 | |
| $MMCM\_F_{INMAX}$ | Maximum input clock frequency | 1066.00 | 933.00 | 800.00 | MHz |
| $MMCM\_F_{INMIN}$ | Minimum input clock frequency | 10.00 | 10.00 | 10.00 | MHz |
| $MMCM\_F_{INJITTER}$ | Maximum input clock period jitter | < 20% of clock input period or 1 ns Max | | | |
| $MMCM\_F_{INDUTY}$ | Allowable input duty cycle: 10—49 MHz | 25.00 | 25.00 | 25.00 | % |
| | Allowable input duty cycle: 50—199 MHz | 30.00 | 30.00 | 30.00 | % |
| | Allowable input duty cycle: 200—399 MHz | 35.00 | 35.00 | 35.00 | % |
| | Allowable input duty cycle: 400—499 MHz | 40.00 | 40.00 | 40.00 | % |
| | Allowable input duty cycle: >500 MHz | 45.00 | 45.00 | 45.00 | % |
| $MMCM\_F_{MIN\_PSCLK}$ | Minimum dynamic phase-shift clock frequency | 0.01 | 0.01 | 0.01 | MHz |
| $MMCM\_F_{MAX\_PSCLK}$ | Maximum dynamic phase-shift clock frequency | 550.00 | 500.00 | 450.00 | MHz |
| $MMCM\_F_{VCOMIN}$ | Minimum MMCM VCO frequency | 600.00 | 600.00 | 600.00 | MHz |
| $MMCM\_F_{VCOMAX}$ | Maximum MMCM VCO frequency | 1600.00 | 1440.00 | 1200.00 | MHz |
| $MMCM\_F_{BANDWIDTH}$ | Low MMCM bandwidth at typical(1) | 1.00 | 1.00 | 1.00 | MHz |
| | High MMCM bandwidth at typical(1) | 4.00 | 4.00 | 4.00 | MHz |
| $MMCM\_T_{STATPHAOFFSET}$ | Static phase offset of the MMCM outputs(2) | 0.12 | 0.12 | 0.12 | ns |
| $MMCM\_T_{OUTJITTER}$ | MMCM output jitter(3) | Note 1 | | | |
| $MMCM\_T_{OUTDUTY}$ | MMCM output clock duty-cycle precision(4) | 0.20 | 0.20 | 0.20 | ns |
| $MMCM\_T_{LOCKMAX}$ | MMCM maximum lock time | 100.00 | 100.00 | 100.00 | µs |
| $MMCM\_F_{OUTMAX}$ | MMCM maximum output frequency | 1066.00 | 933.00 | 800.00 | MHz |
| $MMCM\_F_{OUTMIN}$ | MMCM minimum output frequency(5)(6) | 4.69 | 4.69 | 4.69 | MHz |
| $MMCM\_T_{EXTFDVAR}$ | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | |
| $MMCM\_RST_{MINPULSE}$ | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | ns |
| $MMCM\_F_{PFDMAX}$ | Maximum frequency at the phase frequency detector | 550.00 | 500.00 | 450.00 | MHz |

*Table 71:* **MMCM Specification *(Cont'd)***

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1 | |
| MMCM_$F_{PFDMIN}$ | Minimum frequency at the phase frequency detector | 10.00 | 10.00 | 10.00 | MHz |
| MMCM_$T_{FBDELAY}$ | Maximum delay in the feedback path | 3 ns Max or one CLKIN cycle | | | |
| **MMCM Switching Characteristics Setup and Hold** | | | | | |
| $T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$ | Setup and hold of phase-shift enable | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$ | Setup and hold of phase-shift increment/decrement | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMCKO\_PSDONE}$ | Phase shift clock-to-out of PSDONE | 0.59 | 0.68 | 0.81 | ns |
| **Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK** | | | | | |
| $T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$ | Setup and hold of D address | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | ns, Min |
| $T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$ | Setup and hold of D input | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | ns, Min |
| $T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$ | Setup and hold of D enable | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | ns, Min |
| $T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$ | Setup and hold of D write enable | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | ns, Min |
| $T_{MMCMCKO\_DRDY}$ | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | ns, Max |
| $F_{DCK}$ | DCLK frequency | 200.00 | 200.00 | 200.00 | MHz, Max |

**Notes:**

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}$/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_$F_{OUTMIN}$ is 0.036 MHz.

*Table 81:* **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1 | |
| $T_{PSCS}/T_{PHCS}$ | Setup/hold of I/O clock for HR I/O banks | –0.36/1.36 | –0.36/1.50 | –0.36/1.70 | ns |
| | Setup/hold of I/O clock for HP I/O banks | –0.34/1.39 | –0.34/1.53 | –0.34/1.73 | ns |

*Table 82:* **Sample Window**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1 | |
| $T_{SAMP}$ | Sampling error at receiver pins(1) | 0.51 | 0.56 | 0.61 | ns |
| $T_{SAMP\_BUFIO}$ | Sampling error at receiver pins using BUFIO(2) | 0.30 | 0.35 | 0.40 | ns |

**Notes:**

1. This parameter indicates the total sampling error of the PL DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the PL DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

## Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for PL clock transmitter and receiver data-valid windows.

*Table 83:* **Package Skew**

| Symbol | Description | Device | Package | Value | Units |
|---|---|---|---|---|---|
| $T_{PKGSKEW}$ | Package skew(1) | XC7Z030 | FBG484 | 113 | ps |
| | | | FBG676 | 113 | ps |
| | | | FFG676 | 136 | ps |
| | | XC7Z045 | FBG676 | 159 | ps |
| | | | FFG676 | 158 | ps |
| | | | FFG900 | 191 | ps |
| | | XC7Z100 | FFG900 | | ps |
| | | | FFG1156 | | ps |

**Notes:**

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

# XADC Specifications

*Table 100:* **XADC Specifications**

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCADC}$ = 1.8V ± 5%, $V_{REFP}$ = 1.25V, $V_{REFN}$ = 0V, ADCCLK = 26 MHz, $T_j$ = –40°C to 100°C, Typical values at $T_j$=+40°C | | | | | | |
| **ADC Accuracy**(1) | | | | | | |
| Resolution | | | 12 | – | – | Bits |
| Integral Nonlinearity(2) | INL | | – | – | ±2 | LSBs |
| Differential Nonlinearity | DNL | No missing codes, guaranteed monotonic | – | – | ±1 | LSBs |
| Offset Error | | Unipolar operation | – | – | ±8 | LSBs |
| | | Bipolar operation | – | – | ±4 | LSBs |
| Gain Error | | | – | – | ±0.5 | % |
| Offset Matching | | | – | – | 4 | LSBs |
| Gain Matching | | | – | – | 0.3 | % |
| Sample Rate | | | 0.1 | – | 1 | MS/s |
| Signal to Noise Ratio(2) | SNR | $F_{SAMPLE}$ = 500KS/s, $F_{IN}$ = 20KHz | 60 | – | – | dB |
| RMS Code Noise | | External 1.25V reference | – | – | 2 | LSBs |
| | | On-chip reference | – | 3 | – | LSBs |
| Total Harmonic Distortion(2) | THD | $F_{SAMPLE}$ = 500KS/s, $F_{IN}$ = 20KHz | 70 | – | – | dB |
| **ADC Accuracy at Extended Temperatures (-55°C to 125°C)** | | | | | | |
| Resolution | | | 10 | – | – | Bits |
| Integral Nonlinearity(2) | INL | | – | – | ±1 | LSB (at 10 bits) |
| Differential Nonlinearity | DNL | No missing codes, guaranteed monotonic | – | – | ±1 | |
| **Analog Inputs**(3) | | | | | | |
| ADC Input Ranges | | Unipolar operation | 0 | – | 1 | V |
| | | Bipolar operation | –0.5 | – | +0.5 | V |
| | | Unipolar common mode range (FS input) | 0 | – | +0.5 | V |
| | | Bipolar common mode range (FS input) | +0.5 | – | +0.6 | V |
| Maximum External Channel Input Ranges | | Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels | –0.1 | – | $V_{CCADC}$ | V |
| Auxiliary Channel Full Resolution Bandwidth | FRBW | | 250 | – | – | KHz |
| **On-Chip Sensors** | | | | | | |
| Temperature Sensor Error | | $T_j$ = –40°C to 100°C. | – | – | ±4 | °C |
| | | $T_j$ = –55°C to +125°C | – | – | ±6 | °C |
| Supply Sensor Error | | Measurement range of $V_{CCAUX}$ 1.8V ±5% $T_j$ = –40°C to +100°C | – | – | ±1 | % |
| | | Measurement range of $V_{CCAUX}$ 1.8V ±5% $T_j$ = –55°C to +125°C | – | – | ±2 | % |
| **Conversion Rate**(4) | | | | | | |
| Conversion Time - Continuous | $t_{CONV}$ | Number of ADCCLK cycles | 26 | – | 32 | Cycles |
| Conversion Time - Event | $t_{CONV}$ | Number of CLK cycles | – | – | 21 | Cycles |
| DRP Clock Frequency | DCLK | DRP clock frequency | 8 | – | 250 | MHz |
| ADC Clock Frequency | ADCCLK | Derived from DCLK | 1 | – | 26 | MHz |