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7.3.2 Instruction TLB (ITLB) Configuration

The ITLB is used to translate a virtual address to a physical address in an instruction access. Information in the address translation table located in the UTLB is cached into the ITLB. Figure 7.8 shows the ITLB configuration. The ITLB consists of four fully-associative type entries.

Entry 0	ASID [7:0]	VPN [31:10]	V	PPN [28:10]	SZ [1:0]	SH	C	PR
Entry 1	ASID [7:0]	VPN [31:10]	V	PPN [28:10]	SZ [1:0]	SH	C	PR
Entry 2	ASID [7:0]	VPN [31:10]	V	PPN [28:10]	SZ [1:0]	SH	C	PR
Entry 3	ASID [7:0]	VPN [31:10]	V	PPN [28:10]	SZ [1:0]	SH	C	PR

Notes: 1. The D and WT bits are not supported.
2. There is only one PR bit, corresponding to the upper bit of the PR bits in the UTLB.

Figure 7.8 ITLB Configuration

- Interrupt mask register 2 (INTMSK2)

INTMSK2 settings are valid for particular IRL interrupt codes generated by the pattern of input signals on pins $\overline{IRL7}$ to $\overline{IRL4}$ or $\overline{IRL3}$ to $\overline{IRL0}$ and when all IRL interrupts from the corresponding set of pins are not masked by the setting in INTMSK1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IM015	IM014	IM013	IM012	IM011	IM010	IM009	IM008	IM007	IM006	IM005	IM004	IM003	IM002	IM001	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IM115	IM114	IM113	IM112	IM111	IM110	IM109	IM108	IM107	IM106	IM105	IM104	IM103	IM102	IM101	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit	Name	Initial Value	R/W	Description
31	IM015	0	R/W	Sets masking of interrupt-request generation by $\overline{IRL3}$ to $\overline{IRL0}$ = LLLL (H'0).
30	IM014	0	R/W	Sets masking of interrupt-request generation by $\overline{IRL3}$ to $\overline{IRL0}$ = LLLH (H'1).
29	IM013	0	R/W	Sets masking of interrupt-request generation by $\overline{IRL3}$ to $\overline{IRL0}$ = LLHL (H'2).
28	IM012	0	R/W	Sets masking of interrupt-request generation by $\overline{IRL3}$ to $\overline{IRL0}$ = LLHH (H'3).
27	IM011	0	R/W	Sets masking of interrupt-request generation by $\overline{IRL3}$ to $\overline{IRL0}$ = LHLL (H'4).
26	IM010	0	R/W	Sets masking of interrupt-request generation by $\overline{IRL3}$ to $\overline{IRL0}$ = LHLH (H'5).
25	IM009	0	R/W	Sets masking of interrupt-request generation by $\overline{IRL3}$ to $\overline{IRL0}$ = LHHL (H'6).
24	IM008	0	R/W	Sets masking of interrupt-request generation by $\overline{IRL3}$ to $\overline{IRL0}$ = LHHH (H'7).

[When reading]

0: The interrupt is acceptable.

1: The interrupt is masked.

[When writing]

0: No effect

1: Masks the interrupt

12.4.3 SDRAM Timing Register (STR)

STR specifies various timing parameters for the DDR-SDRAM.

Bit:	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	47
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	WR		RW	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRFC			SWR	SRRD	SRAS			SRC			SCL			SRCD	SRP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
63 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19, 18	WR	00	R/W	Minimum Number of Cycles from Write command to Read Commands These bits specify the minimum number of cycles required by the SDRAM from the issuing of a WRITE command to the issuing of a subsequent READ command. 00: 3 cycles 01: 4 cycles 10: 5 cycles 11: 6 cycles

(5) PCI Revision ID Register (PCIRID)

This register specifies a device specific revision identifier.

Bit:	7	6	5	4	3	2	1	0
	RID							
Initial value:	0	0	0	0	0	0	0	0
SH R/W:	R	R	R	R	R	R	R	R
PCI R/W:	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	RID	H'00	SH: R	Revision ID
			PCI: R	Indicates the PCIC revision.The initial value is H'00.RID value varies according to the logic version of the PCIC and it may be changed in the future.

(6) PCI Program Interface Register (PCIPIF)

This register is the programming interface for the IDE controller class code. For details of the class code, refer to “PCI Local Bus Specification Revision 2.2 Appendix D.”

Bit:	7	6	5	4	3	2	1	0
	MIDED	—	—	—	PIS	OMS	PIP	OMP
Initial value:	0	0	0	0	0	0	0	0
SH R/W:	R/W	R	R	R	R/W	R/W	R/W	R/W
PCI R/W:	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7	MIDED	0	SH: R/W	PCI Master IDE Device
			PCI: R	Specifies the PCI master IDE device.
				1: PCI master IDE device
				0: PCI slave IDE device
				When the CFINIT bit in PCICR is 0, this bit is writable. When the CFINIT bit in PCICR is 1, writing is ignored. This bit is readable.

(18) PCI Capability Pointer Register (PCICP)

This register is the expansion function pointer register of the PCI configuration register that is prescribed in the PCI power management specification.

Bit:	7	6	5	4	3	2	1	0
	CP							
Initial value:	0	1	0	0	0	0	0	0
SH R/W:	R	R	R	R	R	R	R	R
PCI R/W:	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	CP	H'40	SH: R	Capabilities pointer
			PCI: R	The offset address of the expansion function register.

(19) PCI Interrupt Line Register (PCIINTLINE)

Bit:	7	6	5	4	3	2	1	0
	INTLINE							
Initial value:	0	0	0	0	0	0	0	0
SH R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PCI R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	INTLINE	H'00	SH: R/W	PCI Interrupt Line
			PCI: R/W	PCI interrupt connected to the external interrupt of this LSI. Specify these bits by system software during initialization. The initial value is H'00. The setting value of this field does not affect the operation of this LSI.

Bit	Bit Name	Initial Value	R/W	Description
8 to 6	—	All 0	SH: R	Reserved
			PCI: R	These bits are always read as 0. The write value should always be 0.
5	DSI	0	SH: R	DSI
			PCI: R	Specifies whether or not the device requires the specific initialization.
				0: Does not require the specific initialization
4	—	0	SH: R	Reserved
			PCI: R	These bits are always read as 0. The write value should always be 0.
3	PMEC	1	SH: R/W	PCI PME clock
			PCI: R	Specifies whether or not the device requires the clock to support $\overline{\text{PME}}$ generation.
				1: Requires the clock to support $\overline{\text{PME}}$ generation
				Note: This LSI dose not have the $\overline{\text{PME}}$ pin.
2 to 0	PMV	010	SH: R/W	Version
			PCI: R	Specifies the version of the power management specifications.
				010: This LSI's power management specification is conformed to revision 1.1

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	SH: R	Reserved
			PCI: R	These bits are always read as 0. The write value should always be 0.
28 to 20	LSR	0 0000 0000	SH: R/W	Size of Local Address Space 0 (9 bits)
			PCI: R	Specify the size of local address space 0 (SuperHyway bus address space of this LSI) in units of Mbyte. The value set in these bits must be the size minus 1 Mbytes. Setting all the bits to 0 ensures 1-Mbyte space. 0 0000 0000: 1 Mbyte 0 0000 0001: 2 Mbytes 0 0000 0011: 4 Mbytes 0 0000 0111: 8 Mbytes 0 0000 1111: 16 Mbytes 0 0001 1111: 32 Mbytes 0 0011 1111: 64 Mbytes 0 0111 1111: 128 Mbytes 0 1111 1111: 256 Mbytes 1 1111 1111: 512 Mbytes Other than above: Setting prohibited
19 to 1	—	All 0	SH: R	Reserved
			PCI: R	These bits are always read as 0. The write value should always be 0.
0	MBARE	0	SH: R/W	PCI Memory Base Address Register 0 Enable
			PCI: R	The local address space 0 can be accessed by setting this bit to 1. 0: PCIMBAR0 disabled 1: PCIMBAR0 enabled

(20) PCI Memory Bank Register 2 (PCIMBR2)

This register specifies the upper 14-bit address of the PCI memory space 2 (address bits 31 to 18).

Refer to Section 13.4.3 (2), Accessing PCI Memory Space.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PMSBA2														—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SH R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R
PCI R/W:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SH R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
PCI R/W:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	PMSBA2	All 0	SH: R/W PCI: —	PCI Memory Space 2 Bank Address Specify the bank address in PCI memory space 2 for a master access.
17 to 0	—	All 0	SH: R PCI: —	Reserved These bits are always read as 0. The write value should always be 0.

The PCIC can store the error information on the PCI bus. If an error occurs, the error address is stored in the PCI error address information register (PCIAIR), the types of transfer and command information are stored in the PCI error command information register. And then if the PCIC operates host bus bridge mode, the bus master information is stored in the PCI error bus master information register.

Error information is stored only one information. This causes only to store the first occurred error information, and not to store after second error information. The error information is initialized by a power-on reset.

13.4.6 Normal mode

When operating in normal mode, the PCI bus arbitration function in the PCIC is disabled and PCI bus arbitration is performed according to the specifications of the externally connected PCI bus arbiter.

In normal mode, the master performs bus parking is decided by the grant signal that asserted from the external bus arbiter. If the master that performing bus parking is different from the next transaction master, the bus will be high-impedance state for minimum one clock cycle before the address phase.

In normal mode, the $\overline{\text{GNT0}}$/$\overline{\text{GNTIN}}$ pin is used for the grant input signal to the PCIC, and the $\overline{\text{REQ0}}$/$\overline{\text{REQOUT}}$ pin is used for the request output signal from the PCIC.

13.4.7 Power Management

The PCIC supports PCI power management revision 1.1. Supported features are shown below.

- Support for the PCI power management control configuration register.
- Support for the power-down/restore request interrupts from hosts on the PCI bus.

There are seven configuration registers for PCI power management control. PCI capabilities pointer register shows the address offset of the configuration registers for power management. In the PCIC, this offset is fixed at CP = H'40. PCI capability ID (PCICID), next item pointer (PCINIP), power management capability (PCIPMC), power management control/status (PCIPMCSR), PMCSR bridge support extension (PCIPMCSRBSE) and power consumption/dissipation (PCIPCDD) are power management registers. They support four states: power state D0 (normal) power state D1 (bus idle) power state D2 (clock stop) and power state D3 (power down mode).

Figure 13.16 shows the PCI local bus power down state transition.

20.2 Input/Output Pins

Table 20.1 shows the RTC pins.

Table 20.1 RTC Pins

Pin Name	Function	I/O	Description
EXTAL2	RTC oscillator crystal pin	Input	Connects crystal to RTC oscillator
XTAL2	RTC oscillator crystal pin	Output	Connects crystal to RTC oscillator
TCLK*[1]	TMU clock input/RTC clock output	I/O	TMU external clock input pin/input capture control input pin/RTC output pin (shared with TMU)
VDD-RTC	Dedicated RTC power supply	—	RTC oscillator power supply pin*[2]
VSS-RTC	Dedicated RTC GND pin	—	RTC oscillator GND pin*[2]

Notes: 1. This pin is multiplexed with the LBSC and GPIO pins.
2. Power must be supplied to the RTC power supply pins even when the RTC is not used.

Bit	Bit Name	Initial Value	R/W	Description
3	STOP	0	R/W	Stop Bit Length In asynchronous mode, selects 1 or 2 bits as the stop bit length. The stop bit setting is valid only in asynchronous mode. Since the stop bit is not added in clocked synchronous mode, the STOP bit setting is invalid. 0: 1 stop bit*[1] 1: 2 stop bits*[2] In reception, only the first stop bit is checked, regardless of the STOP bit setting. If the second stop bit is 1, it is treated as a stop bit; if it is 0, it is treated as the start bit of the next transmit character. Note: 1. In transmission, a single 1-bit (stop bit) is added to the end of a transmit character before it is sent. 2. In transmission, two 1-bits (stop bits) are added to the end of a transmit character before it is sent.
2	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
1	CKS1	0	R/W	Clock Select 1 and 0
0	CKS0	0	R/W	These bits select the clock source for the on-chip baud rate generator. The clock source can be selected from Pck, Pck/4, Pck/16, and Pck/64, according to the setting of bits CKS1 and CKS0. For details of the relationship between clock sources, bit rate register settings, and baud rate, see section21.3.8, Bit Rate Register n (SCBRR). 00: Pck clock 01: Pck/4 clock 10: Pck/16 clock 11: Pck/64 clock Note: Pck = Peripheral Clock

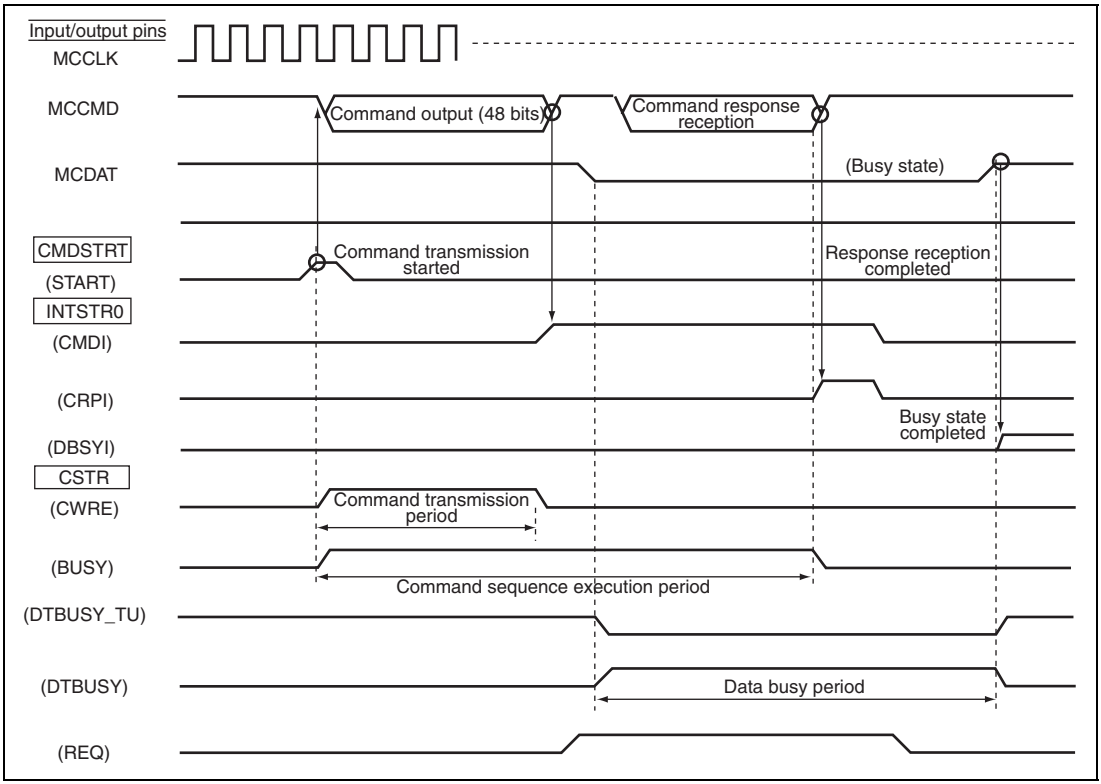

Figure 24.6 Example of Command Sequence for Commands without Data Transfer (with Data Busy State)

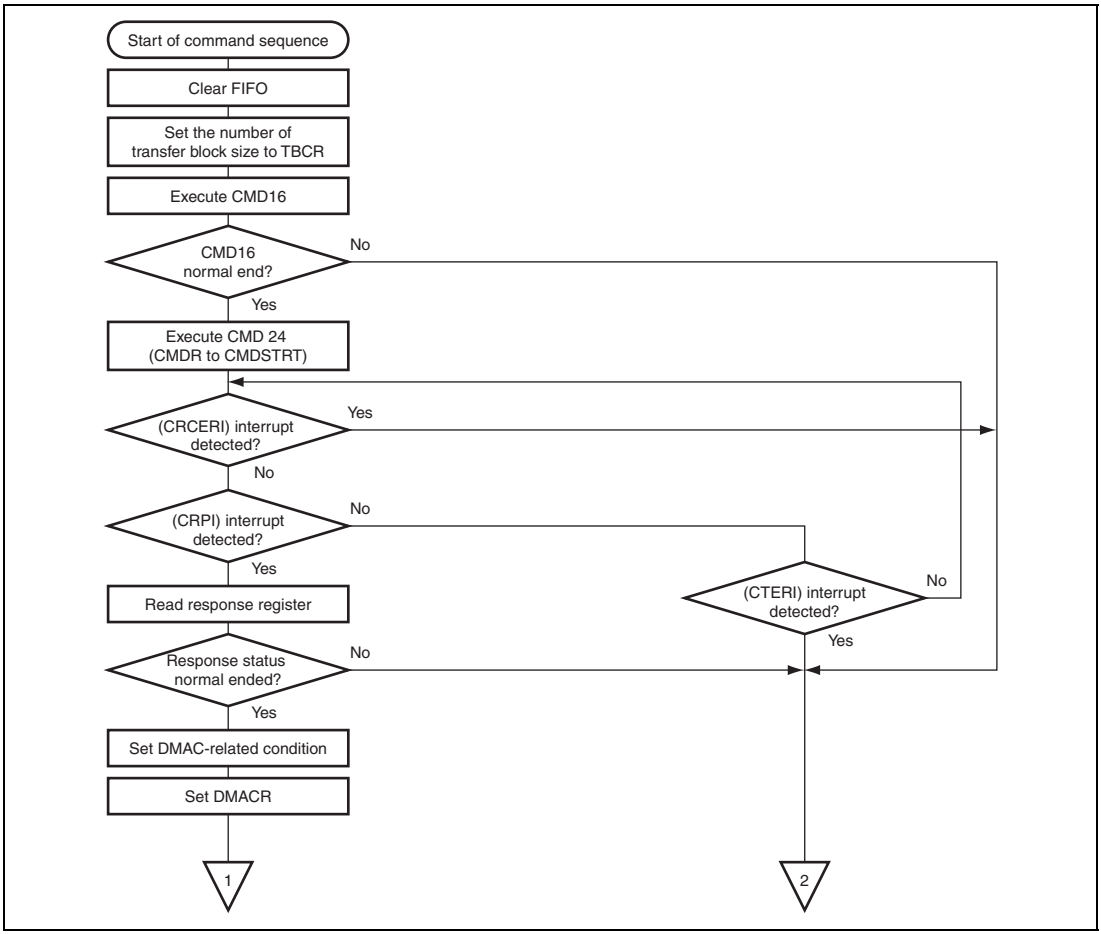

Figure 24.26 Example of Write Sequence Flow (1) (Single Block Transfer)

Data Error:

- When a program error or erase error occurs, the error is reflected on the error source flags. Interrupts for each source can be specified.
- When an ECC error is detected by software, perform an error correction, specify another sector to be replaced, and copy the contents of the block to another sector as required.

Data Transfer FIFO:

- The 224-byte FLDTFIFO is incorporated for data transfer of flash memory.
- The 32-byte FLECFIFO is incorporated for data transfer of a control code.
- Flag bit for detecting overrun/underrun during access from the CPU or DMA

DMA Transfer:

- By individually specifying the destinations of data and control code of flash memory to the DMA controller, data and control code can be sent to different areas.

Access Size:

- Registers can be accessed in 32 bits or 8 bits. Registers must be accessed in the specified access size.
- FIFOs are accessed in 32 bits (4 bytes). Set the byte number for read to a multiple of four, and the byte number for write to a multiple of four.

Access Time:

- The operating frequency of the FLCTL pins can be specified by the FCKSEL bit and the QTSEL bit in the common control register (FLCMNCR), regardless of the operating frequency of the peripheral bus.
- The operating clock FCLK on the pins for the NAND-type flash memory is generated by dividing a peripheral clock (Pck).
- In NAND-type flash memory, the $\overline{\text{FRE}}$ and $\overline{\text{FWE}}$ pins operate with the frequency (FCLK) on the pins which common control register (FLCMNCR) designated. To ensure the setup time, this operating frequencies must be specified within the maximum operating frequency of memory to be connected.

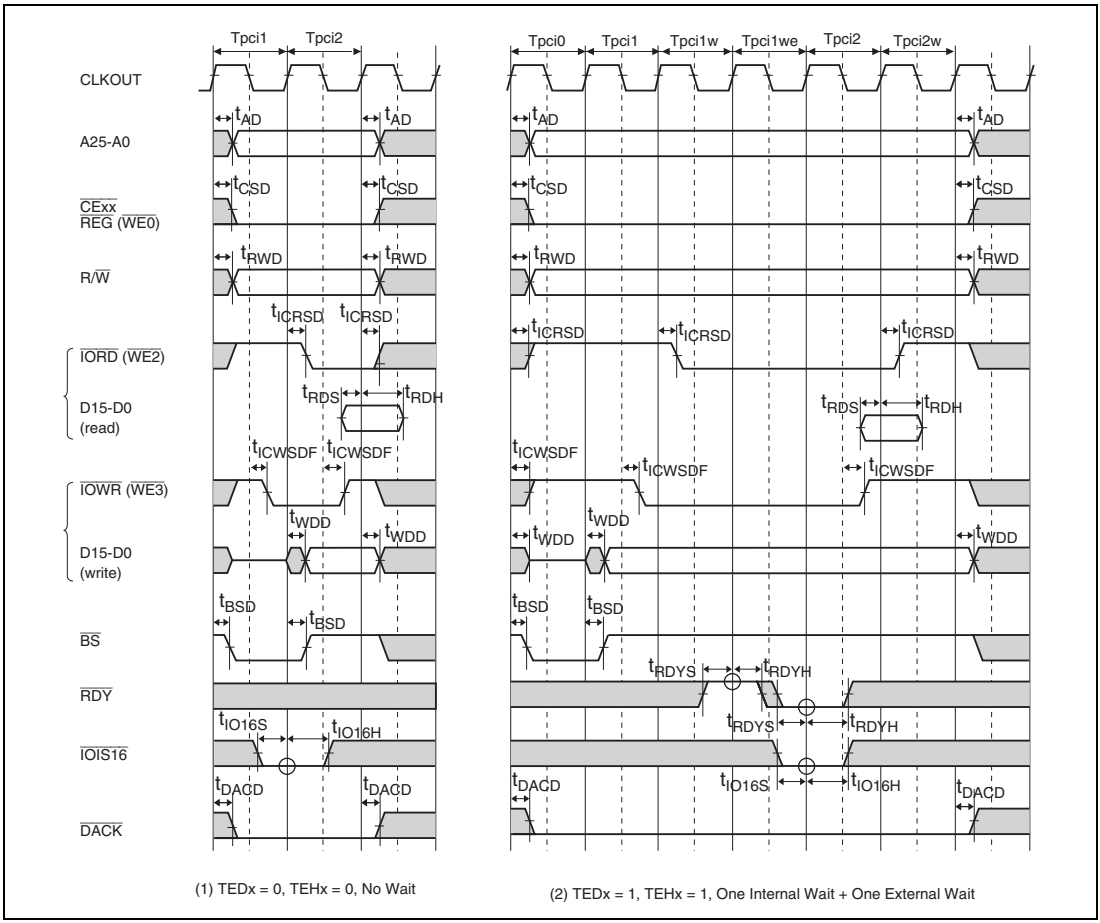

Figure 31.17 PCMCIA I/O Bus Cycle

Physical Address	Register Name	Abbreviation	Initial Value	R/W	Access Size	Module
H'FC81 8088	DMA transfer count register 11	TCR11	H'xxxx xxxx	R/W	32	DMAC
H'FC81 808C	DMA channel control register 11	CHCR11	H'4000 0000	R/W	32	DMAC
H'FC81 8090 to H'FC81 80FF	Reserved (112 bytes)	—	—	—	—	—

DDRIF (H'FE80 0000-H'FEFF FFFF; 8M bytes)

Physical Address	Register Name	Abbreviation	Initial Value	R/W	Access Size	Module
H'FE80 0000 to H'FE80 0007	Reserved (8 bytes)	—	—	—	—	—
H'FE80 0008	Memory interface mode register	MIM (1)	H'0000 0000	R/W	32	DDRIF
H'FE80 000C	Memory interface mode register	MIM (2)	H'0C34 x100	R/W	32	DDRIF
H'FE80 0010	DDR-SDRAM control register	SCR (1)	H'0000 0000	R/W	32	DDRIF
H'FE80 0014	DDR-SDRAM control register	SCR (2)	H'0000 0000	R/W	32	DDRIF
H'FE80 0018	DDR-SDRAM timing register	STR (1)	H'0000 0000	R/W	32	DDRIF
H'FE80 001C	DDR-SDRAM timing register	STR (2)	H'0000 0000	R/W	32	DDRIF
H'FE80 0030	DDR-SDRAM row attribute register	SDR (1)	H'0000 0000	R/W	32	DDRIF
H'FE80 0034	DDR-SDRAM row attribute register	SDR (2)	H'0000 0000	R/W	32	DDRIF
H'FE80 0038 to H'FE80 03FF	Reserved (968 bytes)	—	—	—	—	—

Physical Address	Register Name	Abbreviation	Initial Value	R/W	Access Size	Module
H'FE80 0400	DDR-SDRAM back-up register	DBK (1)	H'0000 0000	R	32	DDRIF
H'FE80 0408	DDR-SDRAM back-up register	DBK (2)	H'0000 000x	R	32	DDRIF
H'FE80 040C to H'FEBF FFFF	Reserved (4,193,268 bytes)	—	—	—	—	—
H'FECx xxxx*	DDR-SDRAM mode register	SDMR	—	W	32	DDRIF

Note: * The DDR-SDRAM mode register is placed in the DDR-SDRAM. The setting value is written to the DDR-SDRAM register by accessing this address. For details, refer to section 12, DDR-SDRAM Interface (DDRIF).