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Understanding Embedded - Microprocessors

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	SH-4A
Number of Cores/Bus Width	-
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-20°C ~ 75°C (TA)
Security Features	-
Package / Case	449-FBGA
Supplier Device Package	449-FBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r8a77800bnbgv

Section 2 Programming Model

The programming model of this LSI is explained in this section. This LSI has registers and data formats as shown below.

2.1 Data Formats

The data formats supported in this LSI are shown in figure 2.1.

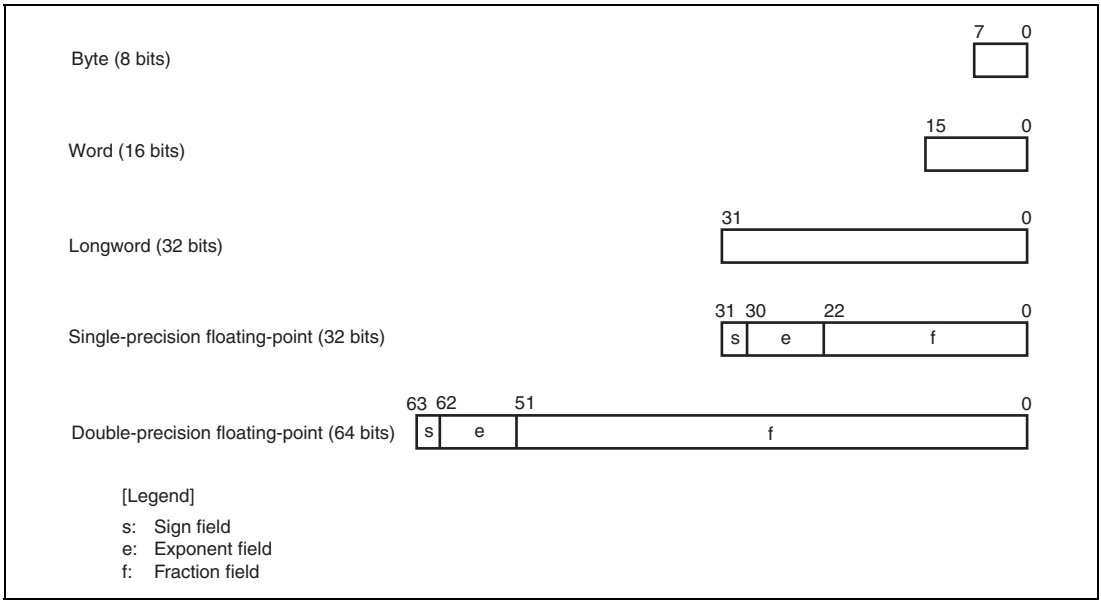


Figure 2.1 Data Formats

Exception Category	Execution Mode	Exception	Priority Level*2	Priority Order*2	Exception Transition Direction*3		Exception Code*4
					Vector Address	Offset	
General exception	Completion type	Unconditional trap (TRAPA)	2	4	(VBR)	H'100	H'160
		User break after instruction execution*1	2	10	(VBR/DBR)	H'100/—	H'1E0
Interrupt	Completion type	Nonmaskable interrupt	3	—	(VBR)	H'600	H'1C0
		General interrupt request	4	—	(VBR)	H'600	—

Notes: 1. When UBDE in CBCR = 1, PC = DBR. In other cases, PC = VBR + H'100.
2. Priority is first assigned by priority level, then by priority order within each level (the lowest number represents the highest priority).
3. Control passes to H'A000 0000 in a reset, and to [VBR + offset] in other cases.
4. Stored in EXPEVT for a reset or general exception, and in INTEVT for an interrupt.

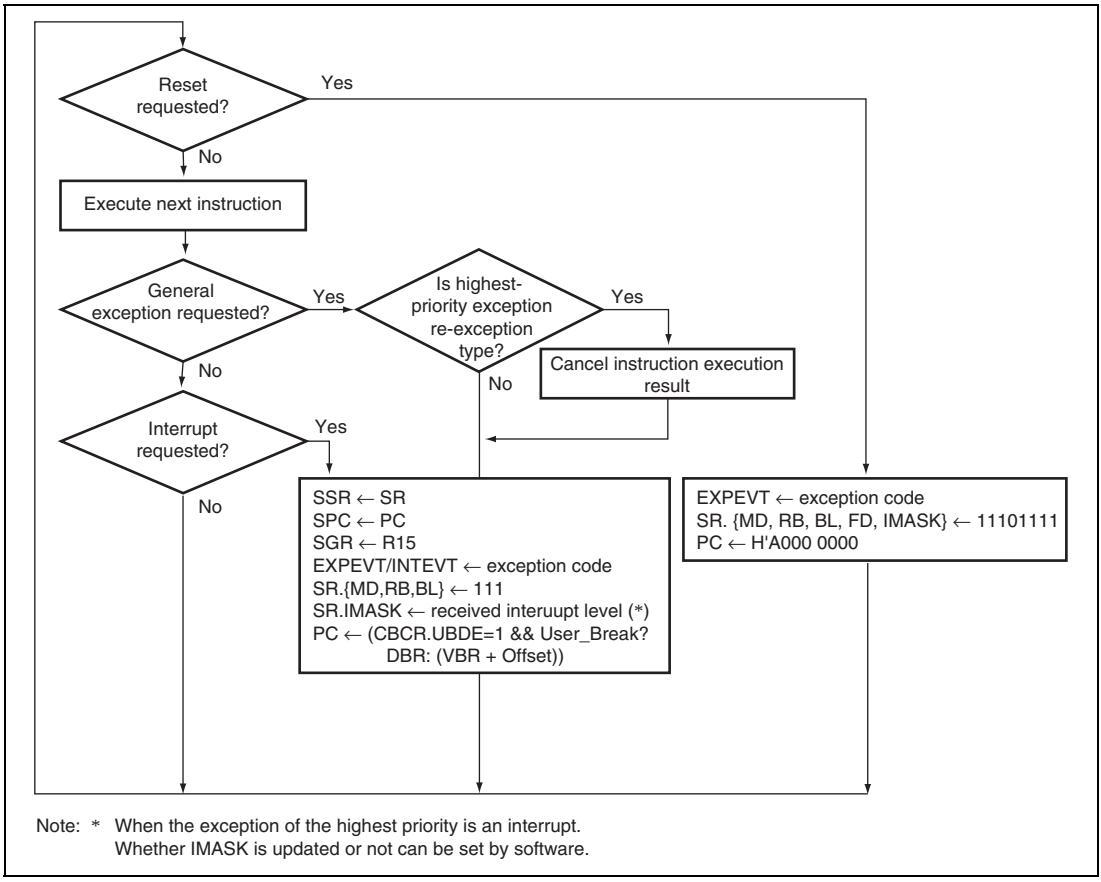


Figure 5.1 Instruction Execution and Exception Handling

4. Note that the V bit is mapped to both address array and data array in PMB registration. That is, first write 0 to the V bit in one of arrays and then write 1 to the V bit in another array.

INT2B3: Indicates detailed interrupt sources for the DMAC.

Module	Bit	Name	Detailed Source	Description
DMAC	31 to 14	—	(Reserved) These bits are always read as 0. Writing to these bits is invalid.	Indicates DMAC interrupt sources. This register indicates DMAC interrupt sources even if a mask setting for DMAC interrupts has been made in the interrupt mask register.
	13	DMAE1	DMA channels 6 to 11 address error interrupt	
	12	DMAE0	DMA channels 0 to 5 address error interrupt	
	11	DMINT11	Channel 11 DMA transfer end or half-end interrupt	
	10	DMINT10	Channel 10 DMA transfer end or half-end interrupt	
	9	DMINT9	Channel 9 DMA transfer end or half-end interrupt	
	8	DMINT8	Channel 8 DMA transfer end or half-end interrupt	
	7	DMINT7	Channel 7 DMA transfer end or half-end interrupt	
	6	DMINT6	Channel 6 DMA transfer end or half-end interrupt	
	5	DMINT5	Channel 5 DMA transfer end or half-end interrupt	
	4	DMINT4	Channel 4 DMA transfer end or half-end interrupt	
	3	DMINT3	Channel 3 DMA transfer end or half-end interrupt	
	2	DMINT2	Channel 2 DMA transfer end or half-end interrupt	
	1	DMINT1	Channel 1 DMA transfer end or half-end interrupt	
	0	DMINT0	Channel 0 DMA transfer end or half-end interrupt	

Note: The DMA transfer end or half-end interrupt means the transfer has finished or half finished with the condition of specified to the corresponding TCR.

INT2B5: Indicates detailed interrupt sources for the MMC.

Module	Bit	Name	Detailed Source	Description
MMCIF	31 to 4	—	(Reserved) These bits are always read as 0. Writing to these bits is invalid.	Indicates MMC interrupt sources. This register indicates MMC interrupt sources even if the mask setting for MMC interrupts has been made in the interrupt mask register.
	3	FRDY	FIFO ready interrupt	
	2	ERR	CRC error interrupt, data timeout error interrupt, or command timeout error interrupt	
	1	TRAN	Data response interrupt, data transfer end interrupt, command response receive end interrupt, command transmit end interrupt, or data busy end interrupt	
	0	FSTAT	MMC FIFO empty interrupt or FIFO full interrupt	

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	SH: R	Reserved
			PCI: R	These bits are always read as 0. The write value should always be 0.
28 to 20	LSR	0 0000 0000	SH: R/W	Size of Local Address Space 0 (9 bits)
			PCI: R	Specify the size of local address space 0 (SuperHyway bus address space of this LSI) in units of Mbyte. The value set in these bits must be the size minus 1 Mbytes. Setting all the bits to 0 ensures 1-Mbyte space. 0 0000 0000: 1 Mbyte 0 0000 0001: 2 Mbytes 0 0000 0011: 4 Mbytes 0 0000 0111: 8 Mbytes 0 0000 1111: 16 Mbytes 0 0001 1111: 32 Mbytes 0 0011 1111: 64 Mbytes 0 0111 1111: 128 Mbytes 0 1111 1111: 256 Mbytes 1 1111 1111: 512 Mbytes Other than above: Setting prohibited
19 to 1	—	All 0	SH: R	Reserved
			PCI: R	These bits are always read as 0. The write value should always be 0.
0	MBARE	0	SH: R/W	PCI Memory Base Address Register 0 Enable
			PCI: R	The local address space 0 can be accessed by setting this bit to 1. 0: PCIMBAR0 disabled 1: PCIMBAR0 enabled

(16) PCI Memory Bank Register 0 (PCIMBR0)

This register specifies the upper 14-bit address of the PCI memory space 0 (address bits 31 to 18).

Refer to Section 13.4.3 (2), Accessing PCI Memory Space.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PMSBA0														—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SH R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R
PCI R/W:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SH R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
PCI R/W:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	PMSBA0	H'0000	SH: R/W PCI: —	PCI Memory Space 0 Bank Address Specify the bank address in PCI memory space 0 for a master access.
17 to 0	—	All 0	SH: R PCI: —	Reserved These bits are always read as 0. The write value should always be 0.

(2) Target Read/Write Cycle Timing

The PCIC responds to target memory burst read accesses from an external master by retries until 8 longword (32-bit) data are prepared in the PCIC's internal FIFO. That is, it always responds to the first target burst read with a retry. For a single read access, the PCIC reaponds as soon as the data is prepared.

Also, when a target memory write access is made, the content of the data is guaranteed until the write data is completely written to the local memory if reading the target write data immediately after write access.

Only single transfers are supported in the case of target accesses of the configuration space and I/O space. If there is a burst access request, the external master is disconnected on completion of the first transfer. Note that the $\overline{\text{DEVSEL}}$ response speed is fixed at 2 clocks (Medium) in the case of target access to the PCIC.

Figure 13.21 shows an example target single read cycle in normal mode. Figure 13.22 shows an example target single write cycle in normal mode. Figure 13.23 is an example of a target burst read cycle in host bus bridge mode. And figure 13.24 is an example of a target burst write cycle in host bus bridge mode.

```
Manual_reset()
{
    EXPEVT = H'0000 0020;
    VBR = H'0000 0000;
    SR.MD = 1;
    SR.RB = 1;
    SR.BL = 1;
    SR.(I0-I3) = B'1111;
    SR.FD = 0;
    Initialize_CPU();
    Initialize_Module(Manual);
    PC = H'A000 0000;
}
```

16.4.2 Using watchdog timer mode

1. Set the WDTCNT overflow interval value in WDTST.
2. Set the WT/IT bit in WDTCSR to 1, select the type of reset with the RSTS bit.
3. When the TME bit in WTCSR is set to 1, the WDT count starts.
4. During operation in watchdog timer mode, clear to the WDTCNT or WDTBCNT periodically so that WDTCNT does not overflow. See section 16.4.5, Clearing WDT Counter for WDT counter clear method.
5. When the WDTCNT overflows, the WDT sets the WOVF flag in WDTCSR to 1, and generates a reset of the type specified by the RSTS bit. After reset operation, the WDTCNT and WDTBCNT continues counting again.

16.4.3 Using Interval timer mode

When the WDT is operating in interval timer mode, an interval timer interrupt is generated each time the counter overflows. This enables interrupts to be generated at fixed intervals.

1. Set the WDTCNT overflow time in WDTST.
2. Clear the WT/IT bit in WDTCSR to 0.
3. When the TME bit in WDTCSR is set to 1, the WDT count starts.
4. When the WDTCNT overflows, the WDT sets the IOVF flag in WDTCSR to 1, and sends an interval timer interrupt (ITI) request to INTC. The counter continues counting.

20.3.7 Month Counter (RMONCNT)

RMONCNT is an 8-bit readable/writable register used as a counter for setting and counting the BCD-coded month value in the RTC. It counts on the carry generated once per month by the day counter.

The setting range is decimal 01 to 12. The RTC will not operate normally if any other value is set. Write processing should be performed after stopping the count with the START bit in RCR2, or by using the carry flag.

RMONCNT is not initialized by a power-on or manual reset.

Bits 7 to 5 are always read as 0. A write to these bits is invalid, but the write value should always be 0.

Bit:	7	6	5	4	3	2	1	0
	—	—	—	10-month unit	1-month units			
Initial value:	0	0	0	—	—	—	—	—
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W

20.3.8 Year Counter (RYRCNT)

RYRCNT is a 16-bit readable/writable register used as a counter for setting and counting the BCD-coded year value in the RTC. It counts on the carry generated once per year by the month counter.

The setting range is decimal 0000 to 9999. The RTC will not operate normally if any other value is set. Write processing should be performed after stopping the count with the START bit in RCR2, or by using the carry flag.

RYRCNT is not initialized by a power-on or manual reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1000-year units				100-year units				10-year units				1-year units			
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
0	DR	0	R/W*	Receive Data Ready In asynchronous mode, indicates that there are fewer than the receive trigger set number of data bytes in SCFRDR, and no further data has arrived for at least 15 etu after the stop bit of the last data received. This is not set when using clocked synchronous mode. 0: Reception is in progress or has ended normally and there is no receive data left in SCFRDR [Clearing conditions] • Power-on reset or manual reset • When all the receive data in SCFRDR has been read after reading DR = 1, and 0 is written to DR • When all the receive data in SCFRDR has been read by the DMAC 1: No further receive data has arrived [Setting condition] • When SCFRDR contains fewer than the receive trigger set number of receive data bytes, and no further data has arrived for at least 15 etu after the stop bit of the last data received* [Legend] etu: Elementary time unit (time for transfer of 1 bit) Note: Equivalent to 1.5 frames with an 8-bit, 1-stop-bit format.

Note: * Only 0 can be written, to clear the flag.

Bit	Bit Name	Initial Value	R/W	Description
2	TFCL	0	R/W	Transmit FIFO Data Count Register Clear Clears the transmit FIFO data count register to 0. 0: Clear operation disabled 1: Clear operation enabled Note: A reset operation is performed in the event of a power-on reset or manual reset.
1	RFCL	0	R/W	Receive FIFO Data Count Register Clear Clears the transmit FIFO data count register to 0. 0: Clear operation disabled 1: Clear operation enabled Note: A reset operation is performed in the event of a power-on reset or manual reset.
0	LOOP	0	R/W	Loopback Test Internally connects the transmit output pin (SCIF_TXD) and receive input pin (SCIF_RXD), and the $\overline{\text{SCIF0\_RTS}}$ pin and $\overline{\text{SCIF0\_CTS}}$ pin (for channel 0), enabling loopback testing. 0: Loopback test disabled 1: Loopback test enabled

Note: * Only channel 0. Reserved bit in channel 1.

Register Name	Abbrev.	R/W	P4 Address	Area 7 Address	Size	Sync Clock
Response register 5	RSPR5	R/W	H'FFE6 0025	H'1FE6 0025	8	Pck
Response register 6	RSPR6	R/W	H'FFE6 0026	H'1FE6 0026	8	Pck
Response register 7	RSPR7	R/W	H'FFE6 0027	H'1FE6 0027	8	Pck
Response register 8	RSPR8	R/W	H'FFE6 0028	H'1FE6 0028	8	Pck
Response register 9	RSPR9	R/W	H'FFE6 0029	H'1FE6 0029	8	Pck
Response register 10	RSPR10	R/W	H'FFE6 002A	H'1FE6 002A	8	Pck
Response register 11	RSPR11	R/W	H'FFE6 002B	H'1FE6 002B	8	Pck
Response register 12	RSPR12	R/W	H'FFE6 002C	H'1FE6 002C	8	Pck
Response register 13	RSPR13	R/W	H'FFE6 002D	H'1FE6 002D	8	Pck
Response register 14	RSPR14	R/W	H'FFE6 002E	H'1FE6 002E	8	Pck
Response register 15	RSPR15	R/W	H'FFE6 002F	H'1FE6 002F	8	Pck
Response register 16	RSPR16	R/W	H'FFE6 0030	H'1FE6 0030	8	Pck
CRC status register	RSPRD	R/W	H'FFE6 0031	H'1FE6 0031	8	Pck
Data timeout register	DTOUTR	R/W	H'FFE6 0032	H'1FE6 0032	16	Pck
Data register	DR	R/W	H'FFE6 0040	H'1FE6 0040	16	Pck
FIFO pointer clear register	FIFOCLR	W	H'FFE6 0042	H'1FE6 0042	8	Pck
DMA control register	DMACR	R/W	H'FFE6 0044	H'1FE6 0044	8	Pck
Interrupt control register 2	INTCR2	R/W	H'FFE6 0046	H'1FE6 0046	8	Pck
Interrupt status register 2	INTSTR2	R/W	H'FFE6 0048	H'1FE6 0048	8	Pck

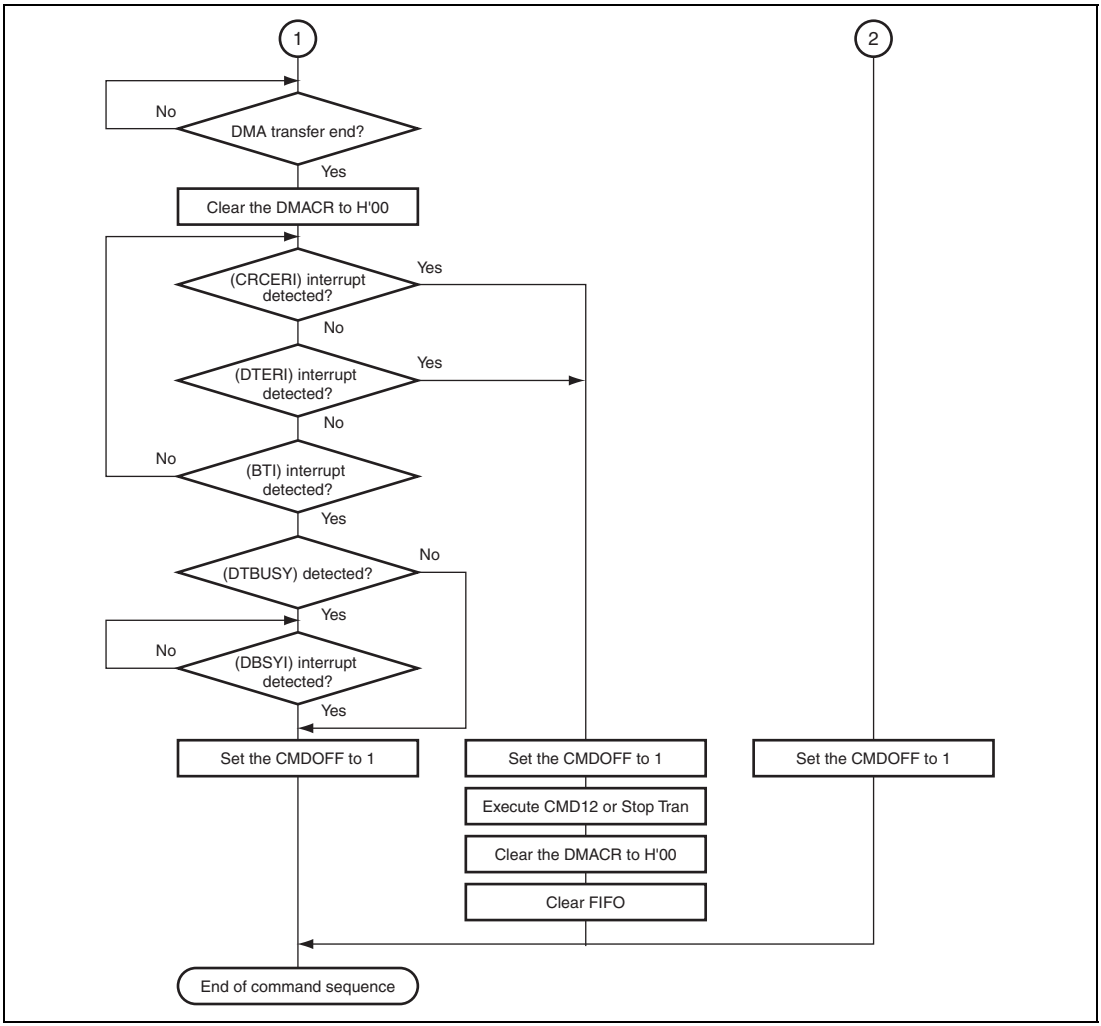


Figure 24.29 Example of Operational Flow for Auto-mode Pre-defined Multiple Block Write Transfer (2)

5. Padding Bits First, Followed by Serial Data, without Delay

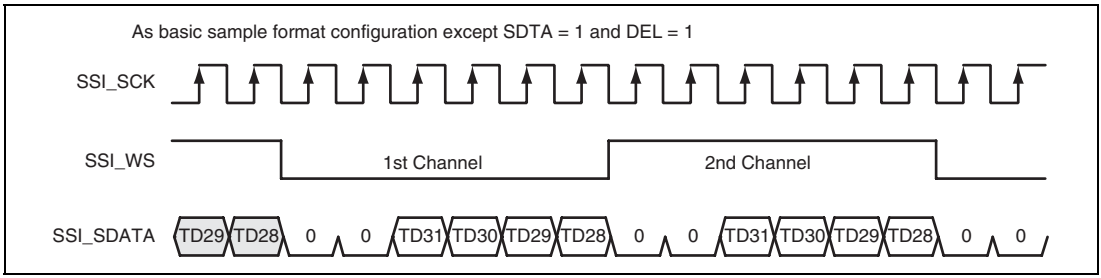


Figure 26.14 Padding Bits First, Followed by Serial Data, without Delay

6. Serial Data First, Followed by Padding Bits, without Delay

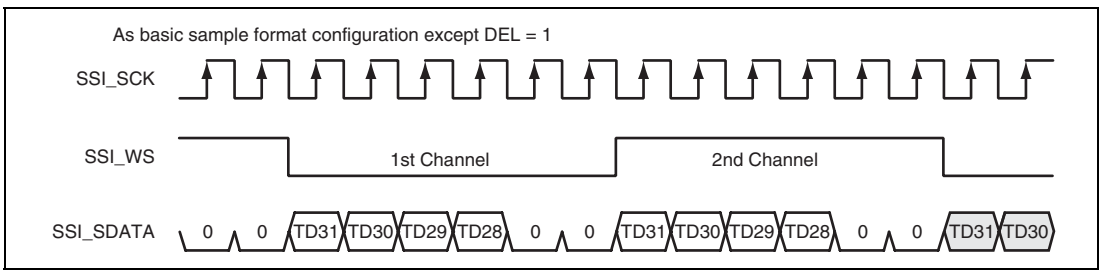


Figure 26.15 Serial Data First, Followed by Padding Bits, without Delay

7. Parallel Right Aligned with Delay

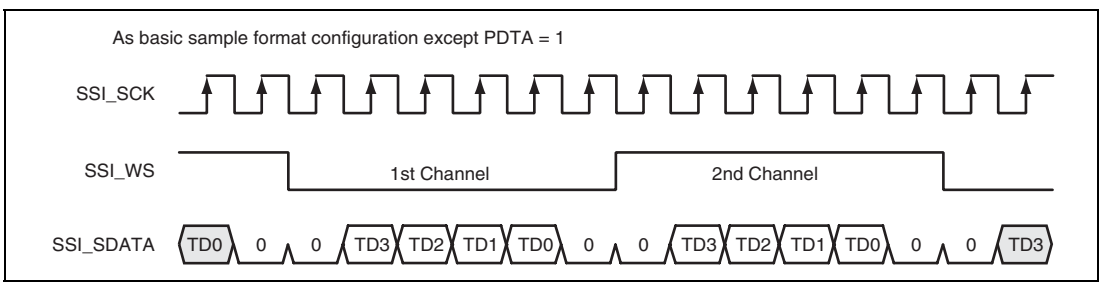


Figure 26.16 Parallel Right Aligned with Delay

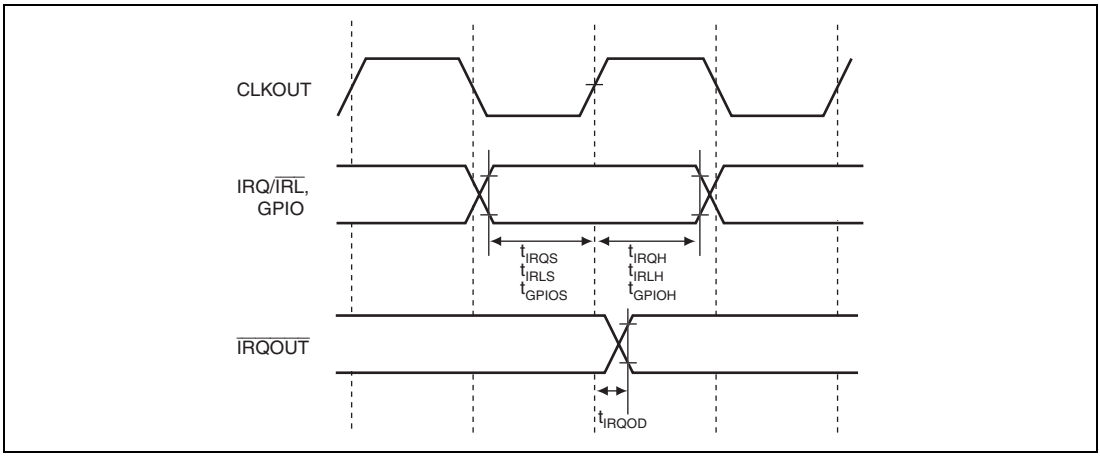


Figure 31.29 IRQ/IRL, GPIO Interrupt Input and IRQOUT Output Timing

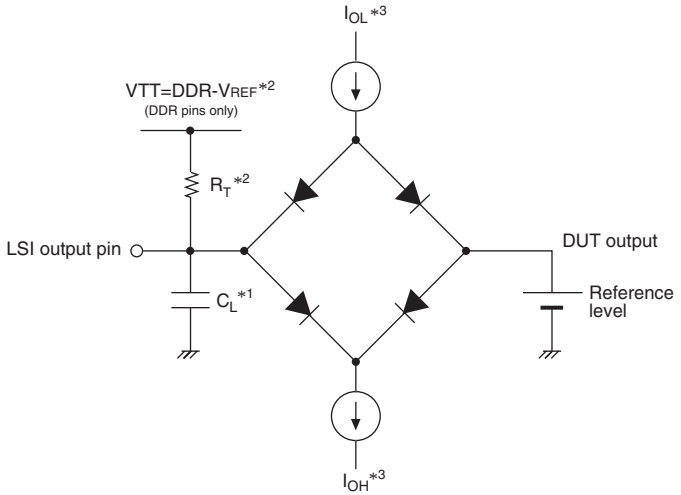
31.4 AC Characteristic Test Conditions

The AC characteristic test conditions are as follows :

- Input/output signal reference level: V*/2
- Input pulse level: V_{SSQ} to V*
- Input rise/fall time: 1 ns

Note: V*: V_{DDQ}, $V_{CCQ-DDR}$ (V_{DDQ} = 3.0 to 3.6V, $V_{CCQ-DDR}$ = 2.3 to 2.7V)

The output load circuit is shown in figure 31.67



Notes: 1. C_L = 30pF (All pins). C_L is the total value that includes the capacitance of measurement instruments.
The capacitance of each pin is set to 30 pF.
2. R_T = 50Ω, V_{TT} = DRR - V_{REF} (DDR pins only)
3. I_{OL} = 7.6 mA (DDR pins),
4 mA (PCI pins),
2 mA (Other output pins)
I_{OH} = –7.6 mA (DDR pins),
–4 mA (PCI pins),
–2 mA (Other output pins)

Figure 31.67 Output Load Circuit

Physical Address	Register Name	Abbreviation	Initial Value	R/W	Access Size	Module
H'FFE6 0027	Response register 7	RSPR7	H'00	R/W	8	MMCIF
H'FFE6 0028	Response register 8	RSPR8	H'00	R/W	8	MMCIF
H'FFE6 0029	Response register 9	RSPR9	H'00	R/W	8	MMCIF
H'FFE6 002A	Response register 10	RSPR10	H'00	R/W	8	MMCIF
H'FFE6 002B	Response register 11	RSPR11	H'00	R/W	8	MMCIF
H'FFE6 002C	Response register 12	RSPR12	H'00	R/W	8	MMCIF
H'FFE6 002D	Response register 13	RSPR13	H'00	R/W	8	MMCIF
H'FFE6 002E	Response register 14	RSPR14	H'00	R/W	8	MMCIF
H'FFE6 002F	Response register 15	RSPR15	H'00	R/W	8	MMCIF
H'FFE6 0030	Response register 16	RSPR16	H'00	R/W	8	MMCIF
H'FFE6 0031	CRC status register	RSPRD	H'00	R/W	8	MMCIF
H'FFE6 0032	Data timeout register	DTOUTR	H'FFFF	R/W	16	MMCIF
H'FFE6 0034 to H'FFE6 003F	Reserved (12 bytes)	—	—	—	—	—
H'FFE6 0040	Data register	DR	H'xxxx	R/W	16	MMCIF
H'FFE6 0042	FIFO pointer clear register	FIFOCLR	H'00	W	8	MMCIF
H'FFE6 0044	DMA control register	DMACR	H'00	R/W	8	MMCIF
H'FFE6 0046	Interrupt control register 2	INTCR2	H'00	R/W	8	MMCIF
H'FFE6 0048	Interrupt status register 2	INTSTR2	H'0x	R/W	8	MMCIF
H'FFE6 0049 to H'FFE6 FFFF	Reserved (65,463 bytes)	—	—	—	—	—

Physical Address	Register Name	Abbreviation	Initial Value	R/W	Access Size	Module
H'FFE7 0000	Control register	SSICR	H'0000 0000	R/W	32	SSI
H'FFE7 0004	Status register	SSISR	H'0200 0003	R/W	32	SSI
H'FFE7 0008	Transmit data register	SSITDR	H'0000 0000	R/W	32	SSI
H'FFE7 000C	Receive data register	SSIRDR	H'0000 0000	R	32	SSI
H'FFE7 0010 to H'FFE7 FFFF	Reserved (65,520 bytes)	—	—	—	—	—

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